

## FULLY INTEGRATED 8-CHANNEL DC/DC CONVERTER FOR DIGITAL STILL CAMERAS

### FEATURES

- 8-Channel DC/DC Converters and LDO
- Integrated Power MOSFET Switch Except CH8
  - Boost (CH5/7)
  - Buck (CH1/3)
  - Buck-Boost (CH2/4)
  - Invert (CH6)
- Low-Power Suspend Mode (Sleep Mode)
- Power ON/OFF Sequence (CH1/2/3 and CH5/6)
- LED-Back Light Brightness Control (CH7)
- Fixed Switching Frequency (CH1–4: 1.5 MHz, CH5–8: 750 kHz)
- Fixed Max Duty Cycle Internally
- Soft Start
- Undervoltage Lockout (UVLO)
- Protection
  - Thermal Shutdown (TSD)
  - Overvoltage Protection (OVP)
  - Overcurrent Protection (OCP) Except CH8
- Supply Voltage Range: 1.5 V to 5.5 V
- Operating Temperature Range: –25°C to 85°C
- 6 × 6 mm, 0.4-mm Pitch, 48-Pin QFN Package

### APPLICATIONS

- Digital Still Cameras (DSCs)
- Portable Electronics Equipment

### DESCRIPTION/ ORDERING INFORMATION

The TPS65530 is highly integrated 8-channel switching dc/dc converter, and seven channels have integrated power FET.

CH2/4 are configured for H bridge for buck-boost topology and single inductor supports. These channels achieve higher efficiency in spite of input/output voltage conditions.

CH7 has a brightness control and drives white LED by constant current. Also, CH7 supports overvoltage protection for open load.

CH1/2/3 has power ON/OFF sequence suitable for a digital still camera (DSC) system. CH5/6 has a power ON/OFF sequence, depending on the CCD. Power ON/OFF for CCD block (CH5/6) is selectable by the input voltage level at the SEQ56 pin. CH4 and CH7 have individual ON/OFF sequences.

The TPS65530 high switching frequency is achieved by an integrated power MOSFET switch. It reduces external parts dynamically. Shutdown current consumption is less than 1  $\mu$ A as a typical value.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–25°C to 85°C	QFN	Reel of 250	TPS65530RSLT
		Reel of 2500	TPS65530RSLR
			TPS65530

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



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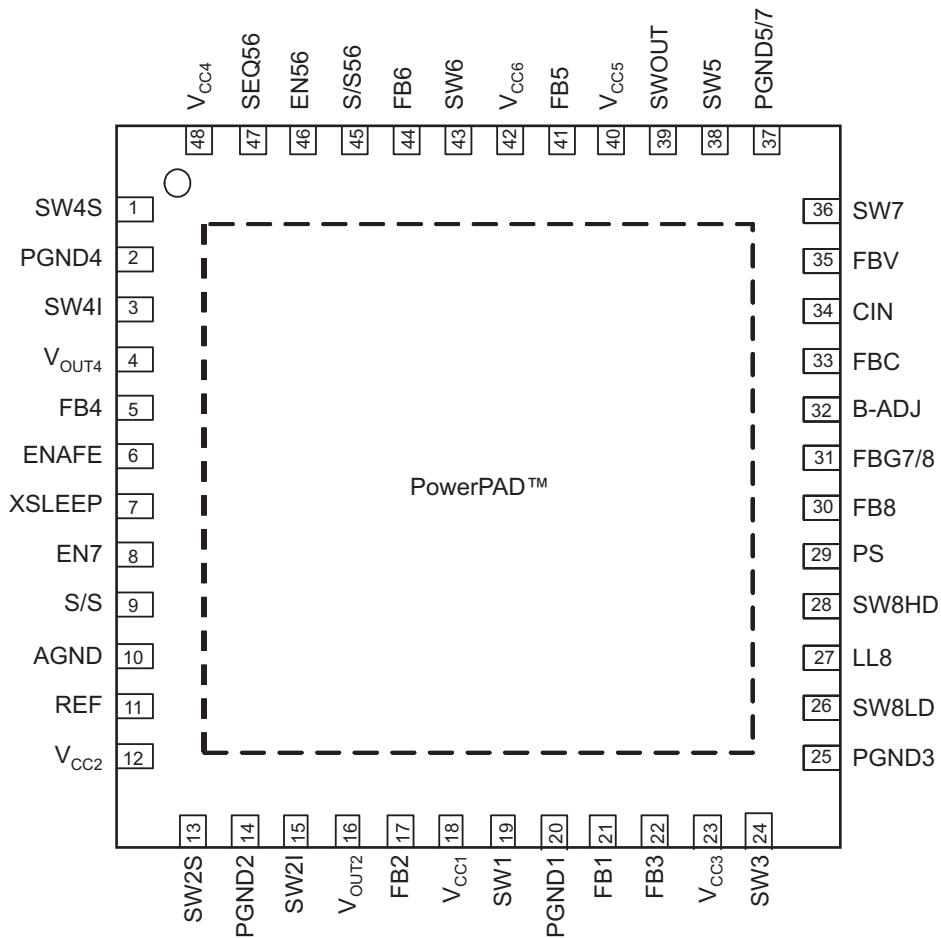


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### CHANNEL CONFIGURATION

CHANNEL	OPERATION MODE	RECTIFY MODE	CONTROL METHOD	OUTPUT VOLTAGE (V)	APPLICATION	MAXIMUM SUPPLY CURRENT (mA)
CH1	Buck SW	Synchronous	Voltage	0.9 to 2.5	Engine core	600
CH2	Buck-boost SW	Synchronous	Average current	2.5 to 3.6	Engine I/O (DSP I/F)	600
CH3	Buck SW	Synchronous	Voltage	0.9 to 2.5	External memory	300
CH4	Buck-boost SW	Synchronous	Average current	2.2 to 3.6	AFE	300
CH5	Boost SW	Non-Synchronous	Peak current	Up to 18.0	CCD+	50
CH6	Invert SW	Non-Synchronous	Voltage	-10.0 to -5.0	CCD-	100
CH7	Boost SW	Non-Synchronous	Voltage	3.0 to 20.0	Backlight LED	25
CH8	Boost SW	Synchronous	Voltage	3.3 to 5.5	Motor controller and IC drive supply	-
REF	Low dropout voltage	-	-	2.8	Internal supply for logic	15

QFN PACKAGE  
(TOP VIEW)



**TERMINAL FUNCTIONS**

TERMINAL		I/O <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
SW4S	1	O	Buck-side terminal of coil for CH4
PGND4	2	G	GND for CH4 low-side FET
SW4I	3	I	Boost-side terminal of coil for CH4
V <sub>OUT4</sub>	4	O	Output of CH4
FB4	5	I	Output voltage feedback for CH4. The external resistors should be connected as close as possible to the terminal.
ENAFE	6	I	Enable for CH4 (L: Disable, H: Enable)
XSLEEP	7	I	Control for sleep mode/normal operation (L: Sleep mode, H: Normal operation)
EN7	8	I	Enable for CH7 (L: Disable, H: Enable)
S/S	9	I/O	Soft start time adjustment. The time is programmable by an external capacitor. Please see the soft start description.
AGND	10	G	Analog ground
REF	11	O	Output of LDO. From 2.2 $\mu$ F to 4.7 $\mu$ F, capacitor should be connected to AGND.
V <sub>CC2</sub>	12	P	Power supply at CH2 buck-side FET from battery
SW2S	13	O	Buck-side terminal of coil for CH2
PGND2	14	G	GND for CH2 low-side FET
SW2I	15	I	Boost-side terminal of coil for CH2
V <sub>OUT2</sub>	16	O	Output of CH2
FB2	17	O	Output voltage feedback for CH2. The external resistors should be connected as close as possible to the terminal.
V <sub>CC1</sub>	18	P	Power supply at CH1 high-side FET from battery
SW1	19	O	Output of CH1. The terminal should be connected to the external inductor.
PGND1	20	G	GND for CH1 low-side FET
FB1	21	I	Output voltage feedback for CH1. The external resistors should be connected as close as possible to the terminal.
FB3	22	I	Output voltage feedback for CH3. The external resistors should be connected as close as possible to the terminal.
V <sub>CC3</sub>	23	P	Power supply at CH3 high-side FET from battery
SW3	24	O	Output of CH3. The terminal should be connected to the external inductor.
PGND3	25	G	GND for CH3 low-side FET
SW8LD	26	O	Output for CH8 external low-side FET drive. The terminal is connected to the gate of the low-side external FET.
LL8	27	O	Switching output for CH8 at wake mode. The terminal is switched when the output voltage of CH8 is less than 2.5 V.
SW8HD	28	O	Output for CH8 external high-side FET drive. The terminal is connected to the gate of the high-side external FET.
PS	29	I	Power input for IC inside. The terminal should be connected to CH8 output voltage.
FB8	30	I	Output voltage feedback for CH8. The external resistors should be connected as close as possible to the terminal.
FBG7/8	31	I	GND for CH7 and CH8 feedback resistors
B-ADJ	32	I	Brightness adjustment for W-LED
FBC	33	I	Output current feedback for CH7
CIN	34	I	Input current at CH7 load switch
FBV	35	I	Output voltage feedback for CH7. The external resistors should be connected as close as possible to the terminal.
SW7	36	O	Output of CH7. The terminal should be connected to the external inductor.
PGND5/7	37	G	Power GND for CH5/7. The terminal should be connected by power ground layer at PCB via a through hole.
SW5	38	O	Low-side terminal of coil for CH5

(1) I = input, O = output, I/O = input/output, P = power supply, G = GND

**TERMINAL FUNCTIONS (continued)**

TERMINAL		I/O <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
SWOUT	39	O	High-side terminal of coil for CH5
V <sub>CC5</sub>	40	P	Power supply at CH5 high-side FET from battery
FB5	41	I	Output voltage feedback for CH5. The external resistors should be connected as close as possible to the terminal.
V <sub>CC6</sub>	42	P	Power supply at CH6 load switch from battery
SW6	43	O	Output of CH6. The terminal should be connected to the external inductor.
FB6	44	I	Output voltage feedback for CH6. The external resistors should be connected as close as possible to the terminal.
S/S56	45	I/O	Soft start-time adjustment terminal for CH5 and CH6. The time is programmable by external capacitor. See the soft-start description.
EN56	46	I	Enable for CH5 and CH6 (L: Disable, H: Enable)
SEQ56	47	I	Sequence select for CH5 and CH6. See the power sequence description.
V <sub>CC4</sub>	48	P	Power supply at CH4 high-side FET from battery
PowerPAD™	Back side	G	Must be soldered to achieve appropriate power dissipation. Should be connected to PGND to use a $\Phi 0.3\text{mm}$ through hole. See the recommended foot pattern description.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			UNIT
Input voltage	V <sub>CC1</sub> , V <sub>CC2</sub> , V <sub>CC3</sub> , V <sub>CC4</sub> , V <sub>CC5</sub> , V <sub>CC6</sub> , SWOUT, FB2, FB4, FB5, FB8, FBC, FBV, PS, XSLEEP, ENAFE, SEQ56, EN56, EN7, SW4S, SW4I, V <sub>OUT4</sub> , SW2S, SW2I, V <sub>OUT2</sub> , SW1, SW3, SW8LD, SW8HD, FBG78 (based on PGND or AGND)	-0.3 to 6	V
	BADJ, SS, FB1, FB3, FB6, SS56	-0.3 to 3	
	LL8	-0.3 to 7	
	REF	-0.3 to 3.6	
	SW5	-0.3 to 22	
	SW7, CIN	-0.3 to 27	
	SW6 (based on V <sub>CC6</sub> )	-20	
	PGND1, PGND2, PGND3, PGND4, PGND57, AGND	-0.3 to 0.3	
Switching current	CIN	0.05	A
	SW2S, SW2I	3.3	
	SW4S, SW4I	1.65	
	SW1	1.9	
	SW3	1.0	
	SW5	1.6	
	SW6	-1.35	
	SW7	1.2	
	LL8	1.0	
	SW8LD, SW8HD	0.6	
T <sub>J</sub>	Maximum junction temperature range	-30 to 150	°C
T <sub>stg</sub>	Storage temperature range	-40 to 150	°C
ESD rating, Human-Body Model (HBM)	JEDEC JESD22A-A114	2	kV
ESD rating, Changed-Device Model (CDM)	JEDEC JESD22A-C101	500	V

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## DISSIPATION RATINGS

PACKAGE	R <sub>θJA</sub> <sup>(1)</sup>	POWER RATINGS T <sub>A</sub> < 25°C	POWER RATINGS RATE T <sub>A</sub> > 25°C
48-pin QFN	27°C/W	2.9 W	0.029°C/W

- (1) The thermal resistance, R<sub>θJA</sub>, is based on a soldered PowerPAD package on a 2S2P JEDEC board (3-in × 3-in, four layers) using thermal vias (0.3 mm diameter × 12 vias)

## RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage	V <sub>CC1</sub> , V <sub>CC2</sub> , V <sub>CC4</sub> , V <sub>CC5</sub>	1.5	5.5	V
	V <sub>CC3</sub> , V <sub>CC6</sub>	2.5	5.5	
High-level input voltage	XSLEEP/ENAFE/EN56/EN7	1.4		V
Low-level input voltage	XSLEEP/ENAFE/EN56/EN7		0.4	V
High-level input voltage	SEQ56	1.4	REF	V
Low-level input voltage	SEQ56		0.4	V
Operating temperature		-25	85	°C

**ELECTRICAL CHARACTERISTICS**

0°C ≤ T<sub>j</sub> ≤ 125°C, 1.8 V ≤ V<sub>CC2</sub> ≤ 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>For All Circuits</b>						
I <sub>CC_Iq</sub>	Consumption current at PS (pin 29)	V <sub>CC2</sub> = VPS = 3.6 V, XSLEEP = AGND		1	10	μA
I <sub>CC_sleep</sub>		V <sub>CC2</sub> = 3.6 V, VPS = 5 V, XSLEEP = AGND, ENAFE = V <sub>CC2</sub>		40	70	
I <sub>CC_PWM</sub>		V <sub>CC2</sub> = 3.6 V, VPS = 5 V, XSLEEP = V <sub>CC2</sub> , ENAFE = V <sub>CC2</sub> , EN56 = V <sub>CC2</sub> , EN7 = V <sub>CC2</sub>		20	30	
I <sub>CC_Iq2</sub>	Consumption current at V <sub>CC2</sub> (pin 12)	V <sub>CC2</sub> = VPS = 3.6 V, XSLEEP = AGND		1	10	μA
I <sub>CC_sleep2</sub>		V <sub>CC2</sub> = 3.6 V, VPS = 5 V, XSLEEP = AGND, ENAFE = V <sub>CC2</sub>		12	30	
I <sub>CC_PWM2</sub>		V <sub>CC2</sub> = 3.6 V, VPS = 5 V, XSLEEP = V <sub>CC2</sub> , ENAFE = V <sub>CC2</sub> , EN56 = V <sub>CC2</sub> , EN7 = V <sub>CC2</sub>		0.3	1.0	
TSD	Thermal shutdown temperature <sup>(2)</sup>			150		°C
V <sub>(UV_ON)</sub>	UVLO detect level	V <sub>CC2</sub> from 0 V to 5.5 V, XSLEEP = V <sub>CC2</sub>	1.25	1.4	1.55	V
V <sub>(UV_OFF)</sub>	UVLO hysteresis	V <sub>CC2</sub> from 5.5 V to 0 V	50	100	150	mV
OSC	Internal OSC frequency	V <sub>CC2</sub> = 3.6 V	1.35	1.5	1.65	MHz
O <sub>SC_SUB</sub>	CH5/6/7/8 switching frequency	OSC = 1.5 MHz, VPS = 5 V		750		KHz
	REF output voltage	XSLEEP = V <sub>CC2</sub>	2.72	2.8	3.03	V
I <sub>SS</sub>	SS source current	S/S=AGND	6	10	14	μA
	Pulldown resistance at XSLEEP, ENAFE, EN56, EN7, SEQ56	XSLEEP = ENAFE = EN56 = EN7 = SEQ56 = 3 V		200		kΩ
<b>CH1</b>						
V <sub>CC1</sub>	Supply voltage		1.5		5.5	V
V <sub>OUT1</sub>	Output voltage <sup>(2)</sup>		0.9		2.5	V
I <sub>OUT1</sub>	Output current <sup>(2)</sup>	V <sub>CC1</sub> > 2.4 V, V <sub>OUT1</sub> = 1.2 V, Feedback resistance: R1 = 330 kΩ, R2 = 330 kΩ			600	mA
V <sub>FB1</sub>	FB1 reference voltage	No load	0.59	0.6	0.61	V
	Overcurrent protection threshold			0.9	1.9	A
	Overvoltage protection threshold (sensing at FB1 pin)		0.67	0.75	0.83	V
	High-side Nch FET ON resistance <sup>(3)</sup>	VPS = 5 V		320	500	mΩ
	Low-side Nch FET ON resistance <sup>(3)</sup>	VPS = 5 V		200	250	mΩ
	Trigger voltage to start CH3			0.48		V
	Trigger voltage to power off LDO			0.25		V
<b>CH2</b>						
V <sub>CC2</sub>	Supply voltage		1.5		5.5	V
V <sub>OUT2</sub>	Output voltage <sup>(2)</sup>		2.5		3.6	V
I <sub>OUT2</sub>	Output current <sup>(2)</sup>	V <sub>CC2</sub> > 2.4 V, V <sub>OUT2</sub> = 3.3 V, Feedback resistance: R1 = 180 kΩ, R2 = 820 kΩ			600	mA
V <sub>FB2</sub>	FB2 reference voltage	No load	0.595	0.605	0.615	V
	Overcurrent protection threshold			2.6	3.3	A
	Overvoltage protection threshold (sensing at FB2 pin)		0.67	0.75	0.83	V
Buck side <sup>(3)</sup>	High-side FET ON resistance	VPS = 5 V		100	210	mΩ
	Low-side FET ON resistance	VPS = 5 V		450	600	

(1) T<sub>A</sub> = 25°C

(2) Specified by design

(3) The value of FET On resistance includes the resistance of bonding wire.

**ELECTRICAL CHARACTERISTICS (continued)**
 $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ,  $1.8\text{ V} \leq V_{CC2} \leq 5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
Boost side <sup>(3)</sup>	High-side FET ON resistance	VPS = 5 V		130	240	mΩ
	Low-side FET ON resistance	VPS = 5 V		80	140	
Trigger voltage to power off CH3		V <sub>OUT2</sub> = 0.5 V		0.5		V
V <sub>OUT2</sub> leakage current		V <sub>OUT2</sub> = 0.5 V			1	μA
Nch FET ON resistance for discharge		XSLEEP = AGND, ENAFE = AGND		1	2	kΩ
<b>CH3</b>						
V <sub>CC3</sub>	Supply voltage		2.5		5.5	V
V <sub>OUT3</sub>	Output voltage <sup>(2)</sup>		0.9		2.5	V
I <sub>OUT3</sub>	Output current <sup>(2)</sup>	V <sub>CC3</sub> > 2.5 V, V <sub>OUT3</sub> = 1.8 V, Feedback resistance: R1 = 220 kΩ, R2 = 470 kΩ			300	mA
V <sub>FB3</sub>	FB3 reference voltage	No load	0.59	0.6	0.61	V
Overcurrent protection threshold				0.6	1.0	A
Overvoltage protection threshold (sensing at FB3 pin)			0.67	0.75	0.83	V
High-side Nch FET ON resistance <sup>(4)</sup>		VPS = 5 V		370	750	mΩ
Low-side Nch FET ON resistance <sup>(4)</sup>		VPS = 5 V		300	600	mΩ
Nch FET ON resistance for discharge		XSLEEP = AGND, ENAFE = AGND		1	2	kΩ
Trigger voltage to start CH2				0.48		V
Trigger voltage to power off CH1				0.2		V
<b>CH4</b>						
V <sub>CC4</sub>	Supply voltage		1.5		5.5	V
V <sub>OUT4</sub>	Output voltage <sup>(5)</sup>		2.2		3.6	V
I <sub>OUT4</sub>	Output current <sup>(5)</sup>	V <sub>CC4</sub> > 2.4 V, V <sub>OUT4</sub> = 3.3 V, Feedback resistance: R1 = 82 kΩ, R2 = 330 kΩ		100	300	mA
V <sub>FB4</sub>	FB4 reference voltage	No load	0.595	0.605	0.615	V
Overcurrent protection threshold				1.4	1.65	A
Overvoltage protection threshold (sensing at FB4 pin)			0.67	0.75	0.83	V
Buck side <sup>(4)</sup>	High-side FET ON resistance	VPS = 5 V		130	310	mΩ
	Low-side FET ON resistance	VPS = 5 V		600	730	
Boost side <sup>(4)</sup>	High-side FET ON resistance	VPS = 5 V		170	270	mΩ
	Low-side FET ON resistance	VPS = 5 V		130	250	
V <sub>OUT4</sub> leakage current		V <sub>OUT4</sub> = 0.5 V			1	μA
Nch FET ON resistance for discharge		XSLEEP = AGND, ENAFE = AGND		1	2	kΩ
<b>CH5</b>						
V <sub>CC5</sub>	Supply voltage		1.5		5.5	V
V <sub>OUT5</sub>	Output voltage <sup>(5)</sup>		V <sub>CC5</sub>		18	V
V <sub>FB5</sub>	FB5 reference voltage	No load	0.98	1	1.02	V
I <sub>OUT5</sub>	Output current <sup>(5)</sup>	V <sub>CC5</sub> > 2.4 V, V <sub>OUT5</sub> = 15 V, Feedback resistance: R1 = 40 kΩ, R2 = 560 kΩ			50	mA

(4) The value of FET On resistance includes the resistance of bonding wire.

(5) Specified by design

**ELECTRICAL CHARACTERISTICS (continued)**

0°C ≤ T<sub>J</sub> ≤ 125°C, 1.8 V ≤ V<sub>CC2</sub> ≤ 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
Overcurrent protection threshold				1.3	1.6	A
Overvoltage protection threshold (sensing at FB5 pin)			1.09	1.25	1.38	V
Nch FET ON resistance <sup>(4)</sup>		VPS = 5 V		610	900	mΩ
Load switch ON resistance (between V <sub>CC5</sub> and SW5)		1.5 V < V <sub>CC5</sub> < 5.5 V		100	470	mΩ
Load switch ramp-up time (between V <sub>CC5</sub> and SW5) <sup>(5)</sup>		1.5 V < V <sub>CC5</sub> < 5.5 V, SWOUT capacitance = 4.7 μF		200		μS
Load switch leakage current (between V <sub>CC5</sub> and SW5)					1	μA
MAX DUTY cycle			96	98		%
Trigger voltage to start up CH6		SEQ56 = AGND		0.8		V
<b>CH6</b>						
V <sub>CC6</sub>	Supply voltage		2.5		5.5	V
V <sub>OUT6</sub>	Output voltage <sup>(5)</sup>		-10		-5	V
I <sub>OUT6</sub>	Output current <sup>(5)</sup>	V <sub>CC6</sub> > 2.8 V, V <sub>OUT6</sub> = -7.5 V, Feedback resistance: R1 = 136 kΩ, R2 = 820 kΩ			100	mA
V <sub>FB6</sub>	FB6 reference voltage	No load	-0.02	0	0.02	V
Overcurrent protection threshold		V <sub>CC6</sub> > 2.8 V		1.1	1.35	A
Overvoltage protection threshold (sensing at FB6 pin)			-0.3	-0.2	-0.1	V
Pch FET ON resistance <sup>(6)</sup>		V <sub>CC6</sub> = 3.6 V		640	1100	mΩ
Max duty cycle			84	91	98	%
Trigger voltage to power off CH6		SEQ56 = AGND	0.5	0.53	0.56	V
V <sub>S/S56</sub>	S/S56 pin voltage		1.22	1.25	1.28	V
I <sub>S/S56</sub>	S/S56 pin source current	S/S56 = AGND	170	200	230	μA
<b>CH7</b>						
V <sub>CC7</sub>	Supply voltage <sup>(7)</sup>		1.5		5.5	V
V <sub>OUT7</sub>	Output voltage <sup>(8)</sup>	V <sub>CC7</sub> < V <sub>OUT7</sub>	3		20	V
I <sub>OUT7_L</sub>	Lower output current <sup>(7)</sup>	V <sub>CC7</sub> > 2.4 V, V <sub>OUT7</sub> = 15 V, Feedback resistance: R1 = 47 kΩ, R2 = 680 kΩ, R <sub>sense</sub> = 10 Ω, B_ADJ pin voltage = 0 V	3.7	5	6.3	mA
I <sub>OUT7_H</sub>	Higher output current <sup>(7)</sup>	V <sub>CC7</sub> > 2.4 V, V <sub>OUT7</sub> = 15 V, Feedback resistance: R1 = 47 kΩ, R2 = 680 kΩ, R <sub>sense</sub> = 10 Ω, B_ADJ pin voltage = 1 V	23.7	25	26.3	mA
V <sub>FBV</sub>	FBV reference voltage	No load	0.97	1	1.03	V
Overvoltage protection threshold (sensing at FBV pin)			1.15	1.25	1.35	V
Overcurrent protection threshold				0.8	1.2	A
Nch FET ON resistance <sup>(6)</sup>				700	1200	mΩ
Max duty cycle			86	91	99	%
Load switch ON resistance				2	4	Ω
Load switch leakage current (between C-IN and FBC)					1	μA
R <sub>B-ADJ</sub>	B-ADJ pin input impedance			1		MΩ

(6) The value of FET On resistance includes the resistance of bonding wire.

(7) Specified by design

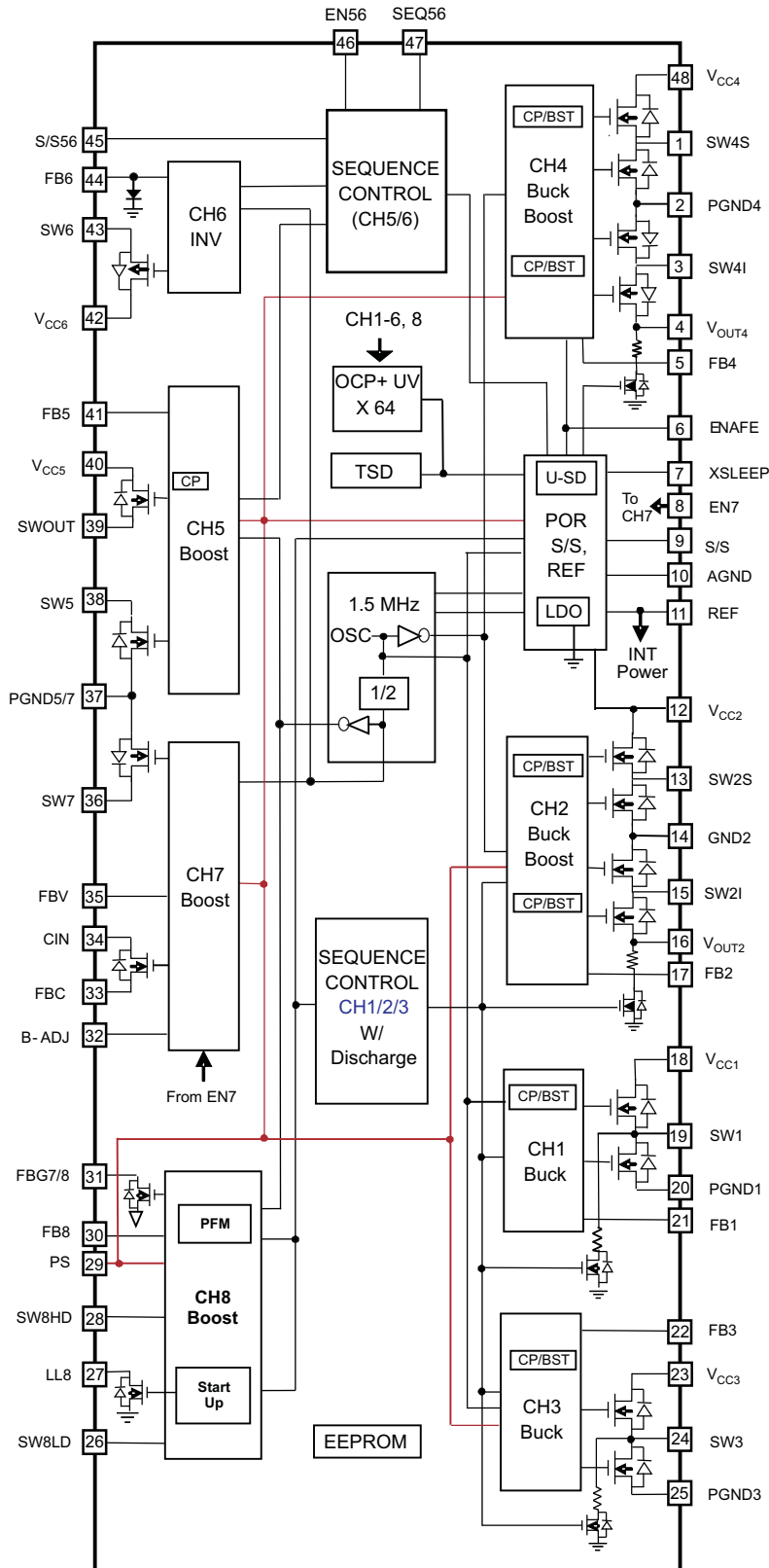
(8) Due to constant current control for CH7, the operating condition is that Input voltage is less than LED supply voltage (Output voltage).



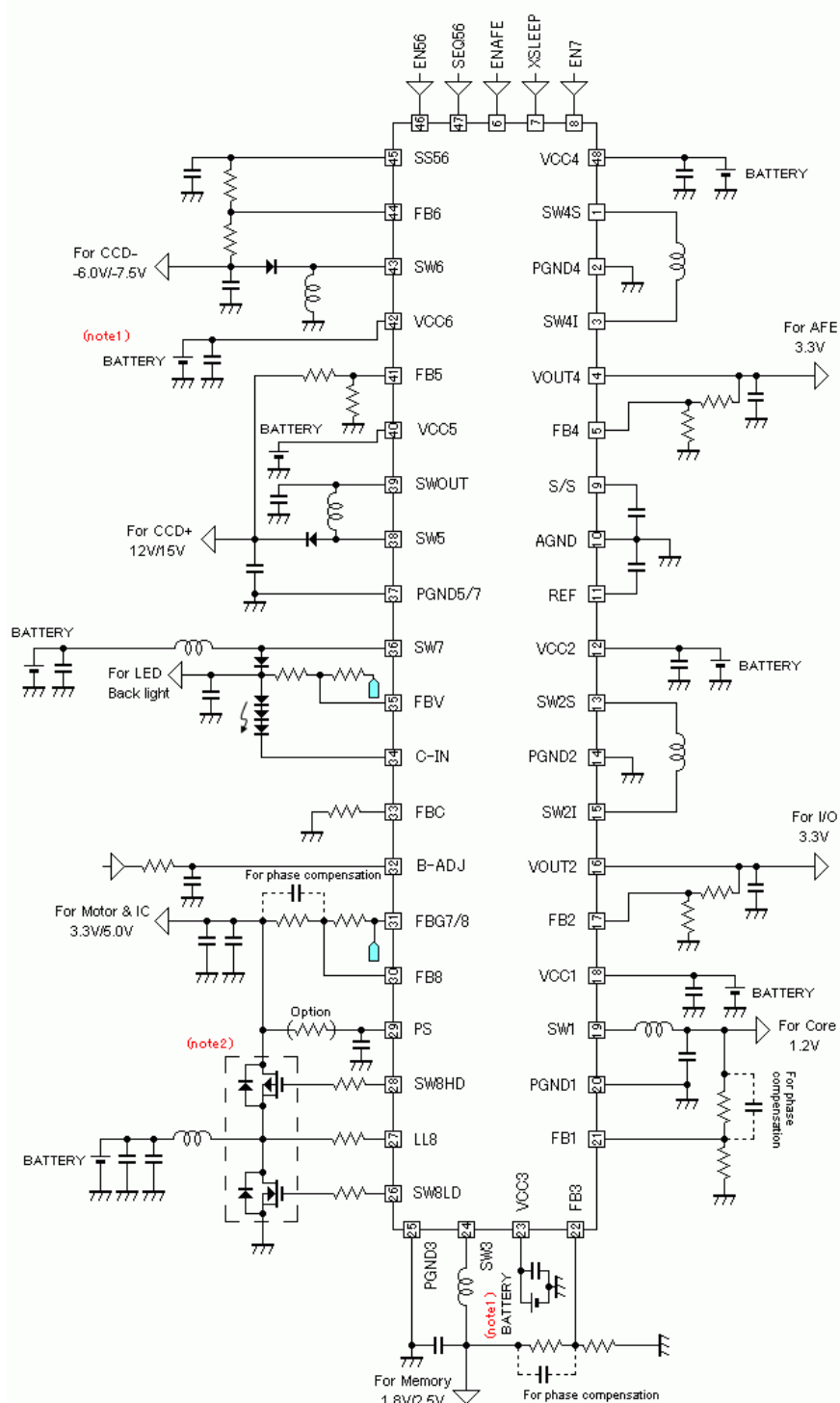
**ELECTRICAL CHARACTERISTICS (continued)**
 $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ,  $1.8\text{ V} \leq V_{CC2} \leq 5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>CH8</b>						
Supply voltage <sup>(7)</sup>		$T_A = 25^{\circ}\text{C}$ , Start up (XSLEEP from AGND to $V_{CC2}$ )	1.8		5.5	V
		XSLEEP = $V_{CC2}$	1.5		5.5	
VPS	Output voltage <sup>(7)</sup>		3.3		5.5	V
$V_{FB8}$	FB8 reference voltage	XSLEEP = H, ENAFE = AGND, No load	1.23	1.25	1.27	V
		CH8 operation mode: PFM mode, No load	1.2	1.25	1.35	V
Fixed ON time at PFM mode		$V_{CC2} = 3.6\text{ V}$		250		ns
Max duty cycle			76	85	92	%
SW8LD driver	Source impedance	VPS = 5 V, ISW = 100 mA		5	7.5	$\Omega$
	Sink impedance	VPS = 5 V, ISW = -100 mA		1	1.5	
SW8HD driver	Source impedance	VPS = 5 V, ISW = 100 mA		10	15	$\Omega$
	Sink impedance	VPS = 5 V, ISW = -100 mA		5	7.5	
Overvoltage protection threshold (sensing at FB8 pin)			1.30	1.56	1.80	V
FBG7/8 FET ON resistance		VPS = 5 V, XSLEEP = $V_{CC2}$		0.6		k $\Omega$
FBG7/8 leakage current		XSLEEP = AGND, ENAFE = AGND			1	$\mu\text{A}$

BLOCK DIAGRAM



**APPLICATION INFORMATION**



- When output voltage is higher than input voltage at 2AA battery models,  $V_{CC1}$  and  $V_{CC3}$  should be connected to the CH8 output. When the 2AA battery is connected,  $V_{CC6}$  should be connected to the CH8 output.
- The external FET for CH8 is dependent on the load. When the motor is connected to CH8, the external FET is large.

## FUNCTIONAL DESCRIPTION

### Logic True Table

The enable/disable of each channel is controlled by logic input signals level at XSLEEP (pin 7 for all channels), ENAFE (pin 6 for CH4), EN56 (pin 46 for CH5 and CH6) and EN7 (pin 8 for CH7). Table 1 is the summary of the enable/disable mode.

Table 1. Control Pin vs Enable/Disable

NO. OF STATE	XSLEEP	ENAFE	EN56	EN7	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8 <sup>(1)</sup>	LDO
1	L	L	-	-	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
2	H	L	L	L	ON	ON	ON	OFF	OFF	OFF	OFF	PWM	ON
3	H	L	L	H	ON	ON	ON	OFF	OFF	OFF	ON	PWM	ON
4	H	L	H	L	ON	ON	ON	OFF	ON	ON	OFF	PWM	ON
5	H	L	H	H	ON	ON	ON	OFF	ON	ON	ON	PWM	ON
6	H	H	L	L	ON	ON	ON	ON	OFF	OFF	OFF	PWM	ON
7	H	H	L	H	ON	ON	ON	ON	OFF	OFF	ON	PWM	ON
8	H	H	H	L	ON	ON	ON	ON	ON	ON	OFF	PWM	ON
9	H	H	H	H	ON	ON	ON	ON	ON	ON	ON	PWM	ON
10 <sup>(2)</sup>	L	H	-	-	OFF	OFF	OFF	OFF	OFF	OFF	OFF	PFM	OFF

- (1) PWM = pulse width modulation, PFM = pulse frequency modulation
- (2) State 10 (CH8: PFM mode) must go through State 2.

### Power ON/OFF Sequence

This device has the power ON/OFF sequence of CH1/2/3/8/REF and CH5/6 for DSC application. The CH1/2/3/8/REF sequence is shown in Figure 1. The CH5/6 sequence is shown in Figure 2. CH4 and CH7 have individual sequences but CH4/5/6 has the subordinate relationship with CH1/2/3 because the slope of soft start is the same and puts high priority of CH1/2/3 to avoid the functional conflict (see the Soft Start description). Due to this, CH4/5/6 should not be ON before CH1/2/3 is ON. When XSLEEP is forced low, all channels turn OFF with the power OFF sequence.

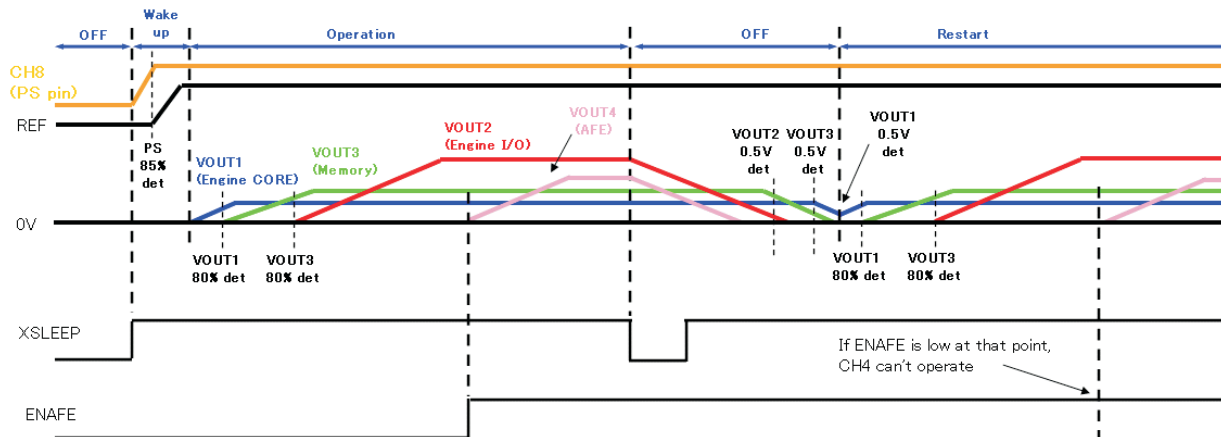
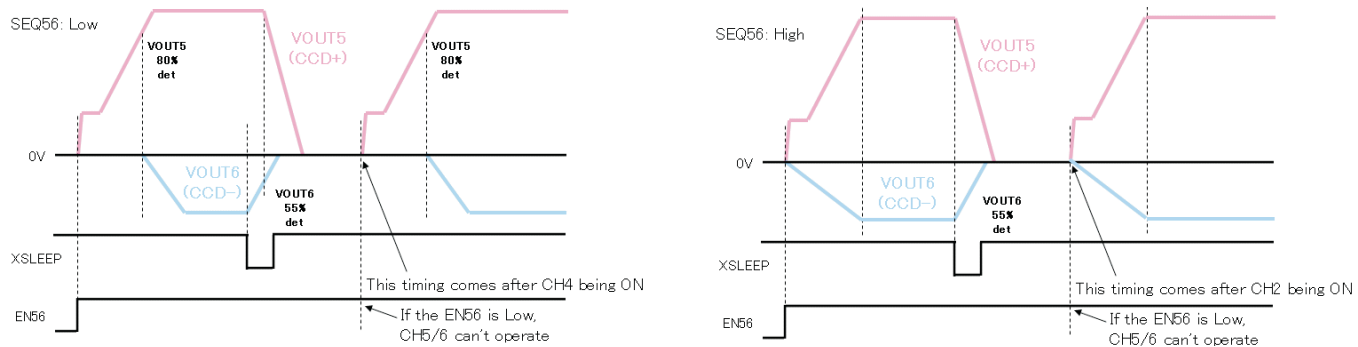


Figure 1. CH1/CH2/CH3/CH8/REF Power ON/OFF Sequence



**Figure 2. CH5/CH6 Power ON/OFF Sequence**

## Soft Start

This function reduces the rush current from the battery at start-up. This device has two slopes, defined by S/S (pin 9) and S/S56 (pin 45). The slopes of CH1/2/3/4 are defined by S/S (pin 9); the slope of CH5/6 depends on SEQ56 (pin 47) signal level. When SEQ 56 (pin 47) is low, the slope of CH5 is defined by S/S (pin 9), the slope of CH6 is defined by S/S56 (pin 45). When SEQ 56 (pin 47) is high, the slopes of CH5 and CH6 are defined by S/S56 (pin 45). The soft-start time is calculated by [Equation 1](#) and [Equation 2](#).

$$T_{S/S} = C_{S/S} \times 60 \quad (1)$$

$$T_{S/S56} = C_{S/S56} \times 6.25 \quad (2)$$

$C_{S/S}$ : Capacitance at S/S pin [ $\mu\text{F}$ ],  $T_{S/S}$ : soft start duration defined by S/S pin [ms]

$C_{S/S56}$ : Capacitance at S/S56 pin [ $\mu\text{F}$ ],  $T_{S/S56}$ : soft start duration defined by S/S56 pin [ms]

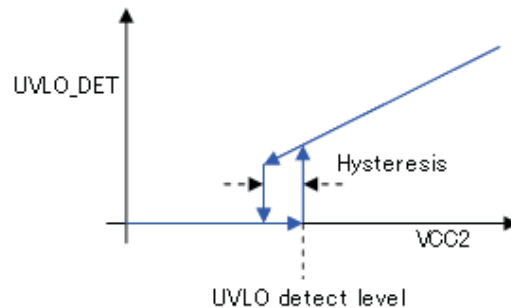
The recommended capacitances are:

$$C_{S/S}: 0.1 \text{ } [\mu\text{F}], \text{ or } T_{S/S}: 6.0 \text{ } [\text{ms}] \quad (3)$$

$$C_{S/S56}: 1.0 [\mu\text{F}], \text{ or } T_{S/S56}: 6.25 \text{ } [\text{ms}] \quad (4)$$

## Undervoltage Lockout (UVLO)

This device monitors the battery voltage level at  $V_{CC2}$  (pin 12). When XSLEEP is high and  $V_{CC2}$  (pin 12) is less than the threshold (defined in *Electrical Characteristics* as UVLO detect level), the operation shuts down immediately without the power OFF sequence. UVLO has a hysteresis as shown in [Figure 3](#). This factor is defined in *Electrical Characteristics* as UVLO hysteresis.



**Figure 3. UVLO Hysteresis**

## Protections

The TPS65530 has protections: overcurrent protection (OCP), overvoltage protection (OVP), and thermal shutdown (TSD) (see [Table 2](#)).

**Table 2. Protection Conditions**

PROTECTION		CH1–CH6	CH7	CH8	REF (LDO)
OCP	Change mode	All CH shutdown (latch-off) (without power OFF sequence)	Forced OFF at MOSFET	All CH shutdown (latch-off) (without power OFF sequence)	All CH shutdown (latch-off) (without power OFF sequence)
	Detect condition	Current over the threshold, $V_{OUT}$ less than 80% to compare the target, and count 64 cycle $\times$ 1.5 MHz	Current over the threshold	$V_{OUT}$ less than 70% to compare the target	$V_{OUT}$ less than 80% to compare the target
	Comeback condition	XSLEEP: Change level from Low to High ENAFE: Change level from Low to High (for CH4) EN56: Change level from Low to High (for CH5/6) or $V_{CC2}$ : Apply more than UVLO threshold (1.4 V) after removing $V_{CC2}$	Current less than the threshold (automatic restoration) or $V_{CC2}$ : Apply more than UVLO threshold (1.4 V) after removing $V_{CC2}$	XSLEEP: Change level from Low to High ENAFE: Change level from Low to High or $V_{CC2}$ : Apply more than UVLO threshold (1.4 V) after removing $V_{CC2}$	XSLEEP: Change level from Low to High ENAFE: Change level from Low to High or $V_{CC2}$ : Apply more than UVLO threshold (1.4 V) after removing $V_{CC2}$
OVP	Change mode	Forced OFF at applicable CH MOSFET	Forced OFF at MOSFET, load switch turns ON	Forced OFF at MOSFET	No OVP function
	Detect condition	Voltage over the threshold at feedback	Voltage over the threshold at feedback	Voltage over the threshold at feedback	
	Comeback condition	Voltage less than the threshold at feedback (auto-recovery)	EN7: Change level from low to high	Voltage less than the threshold at feedback (auto-recovery)	
TSD	Change mode	All CH shutdown (without power OFF sequence)			
	Detect condition	The junction temperature is more than the threshold.			
	Comeback condition	XSLEEP: Change level from Low to High, ENAFE: Change level from Low to High (for CH4), EN56: Change level from Low to High (for CH5/6), or $V_{CC2}$ : More than 1.4 V			

## CHANNEL DESCRIPTIONS

### CH1/3 Description

Both CH1 and CH3 are the same topology. CH1/3 is the voltage-mode-controlled synchronous buck converter for engine core (CH1) or external memory (CH3). Both high-side and low-side switches are integrated into the device and consist of NMOS-FET only. The gate of the high-side switch is driven by bootstrap circuit. The capacitance of the bootstrap is included in the device. These channels are able to operate up to 100% duty cycle.

This device has a discharge path to use the switch (Q\_Discharge1/3) for CH1/3 output capacitor via the inductor. The switch is activated after the power OFF sequence has started. Typical resistance at the discharge circuit is 1 k $\Omega$ . When the device detects the threshold at FB1/3 after the power OFF sequence has started, the MOSFET turns OFF and the output is fixed with high impedance.

It is acceptable to connect the battery to  $V_{CC1}$  (pin 18)/ $V_{CC3}$  (pin 23) directly when the battery voltage is more than 2.5 V. When the battery voltage is less than 2.5 V, the CH8 output should be connected to  $V_{CC1}$  (pin 18)/ $V_{CC3}$  (pin 23).

The output voltage is programmed from 0.9 V to 2.5 V (both CH1 and CH3) to use the feedback loop sensed by the external resistances. The output voltage is calculated by Equation 5. The block diagram is shown in Figure 4.

$$V_{OUT} = (1 + R2/R1) \times 0.6 \text{ [V]} \quad (5)$$

$V_{OUT}$ : Output voltage [V]  
R1, R2: Feedback resistance (see Figure 4)

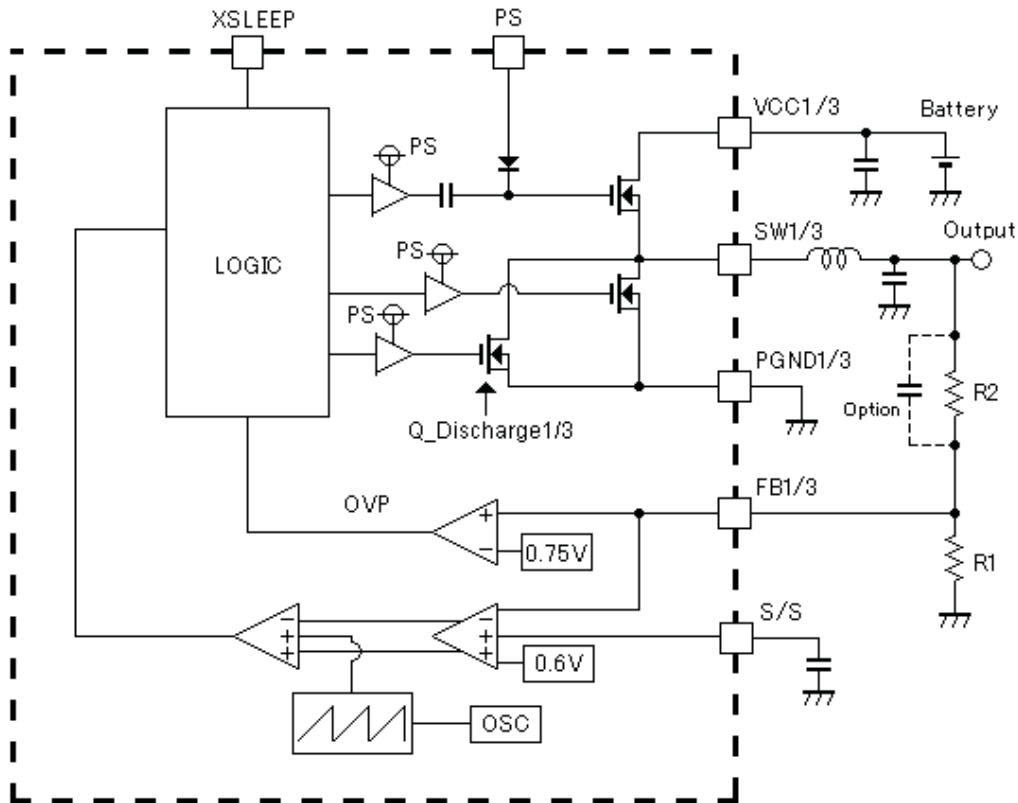


Figure 4. CH1/3 Block Diagram

CH1/3 Recommended Parts

Table 3. Recommended Parts for Inductor (CH1 and CH3)

VENDOR	TYPE NUMBER	INDUCTANCE (μH)	DCR (mΩ)	SIZE (mm)
TOKO	DE2812C-1098AS-4R7M	4.7	130	2.8 × 3.0 × 1.2

Table 4. Recommended Parts for Capacitor (Input, CH1 and CH3)

VENDOR	TYPE NUMBER	CAPACITANCE (μF)	TOLERANCE (%)	SIZE (mm)
Murata	GRM21BB30J226ME38	22.0	20	2.0 × 1.25 × 1.25 (EIA code: 0805)

Table 5. Recommended Parts for Capacitor (Output, CH1 and CH3)

VENDOR	TYPE NUMBER	CAPACITANCE (μF)	TOLERANCE (%)	SIZE (mm)
TDK	C2012X5R0J106M	10.0	20	2.0 × 1.25 × 1.25 (EIA code: 0805)

CH2/4 Description

Both CH2 and CH4 are the same topology. CH2/4 is the average current-mode-controlled synchronous back-boost converter for engine I/O (CH2) or AFE (CH4). This converter is an adapted H-bridge circuit to use four switches. These switches are integrated into the device and consist of NMOS-FET only. The gate of the high-side switch is controlled by the bootstrap circuit. The capacitance of the bootstrap is included in the device.

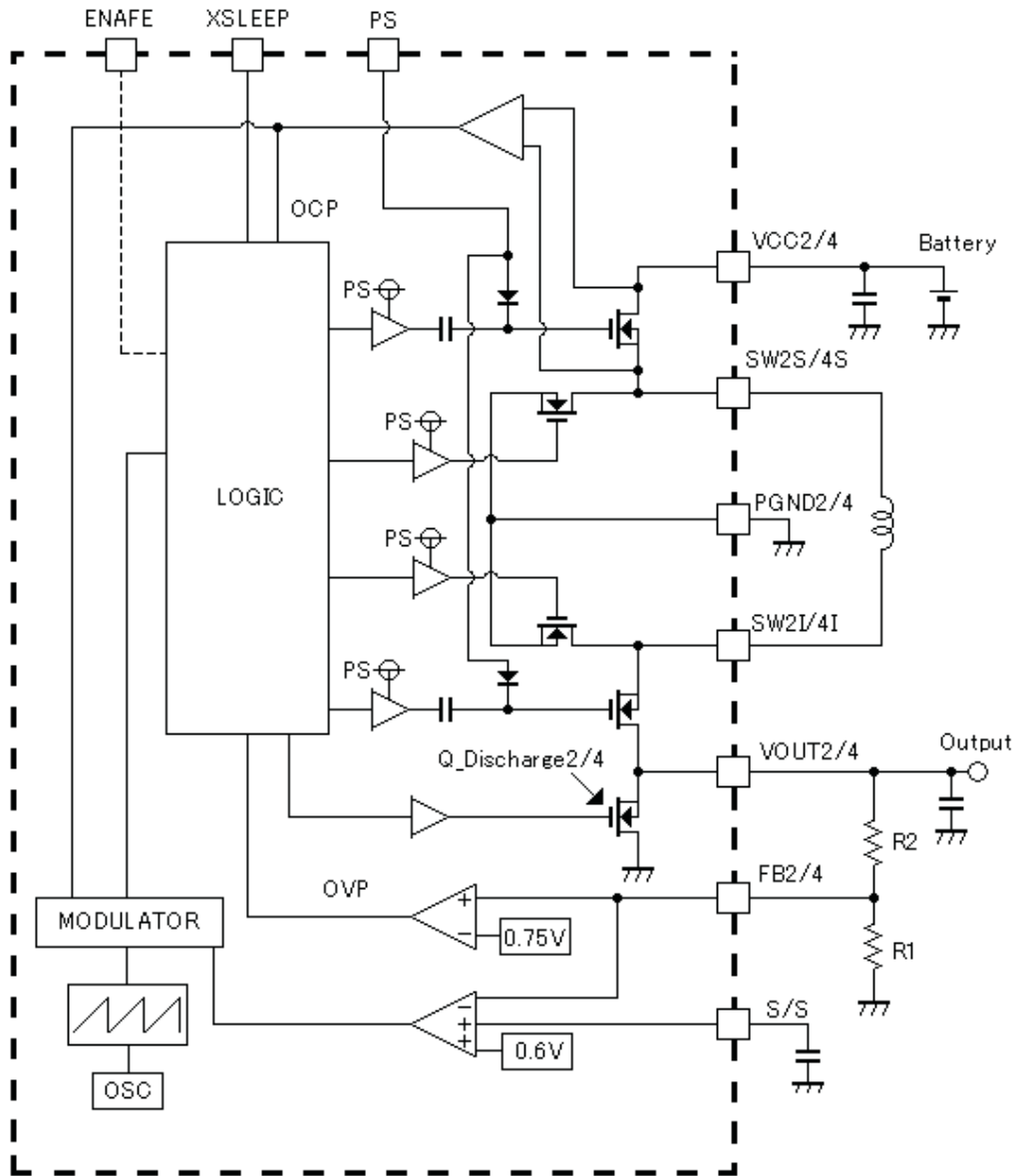
The device automatically switches from buck operation to boost operation or from boost operation to buck operation as required by the configuration. It always uses one active switch, one rectifying switch, one switch permanently on, and one switch permanently off. Therefore, it operates as a buck converter when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all four switches are permanently switching.



This device has a discharge switch (Q\_Discharge2/4) for the CH2/4 output capacitor. The typical ON resistance at the discharge switch is 1 kΩ. The discharge switch is activated when XSLEEP turns low. For CH4 only, the switch is also activated when ENAFE turns low. After output voltage reaches approximately 0.5 V, the discharge switch turns OFF and VOUT2/4 is changed into high impedance. The output voltage is programmable from 2.5 V to 3.6 V (for CH2) or from 2.2 V to 3.6 V (for CH4) to use the feedback loop sensed by the external resistances. The output voltage is calculated by Equation 6. The block diagram is shown in Figure 5.

$$V_{OUT} = (1 + R2/R1) \times 0.6 \text{ [V]} \tag{6}$$

$V_{OUT}$ : Output voltage [V]  
 $R1, R2$ : Feedback resistance (see Figure 5)



**Figure 5. CH2/4 Block Diagram**

**CH2/4 Recommended Parts****Table 6. Recommended Parts for Inductor (CH2)**

VENDOR	TYPE NUMBER	INDUCTANCE (μH)	DCR (mΩ)	SIZE (mm)
TOKO	DE2812C-1098AS-2R7M	2.7	72	2.8 × 3.0 × 1.2

**Table 7. Recommended Parts for Inductor (CH4)**

VENDOR	TYPE NUMBER	INDUCTANCE (μH)	DCR (mΩ)	SIZE (mm)
TOKO	DE2812C-1098AS-4R7M	4.7	130	2.8 × 3.0 × 1.2

**Table 8. Recommended Parts for Capacitor (Input, CH2 and CH4)**

VENDOR	TYPE NUMBER	CAPACITANCE (μF)	TOLERANCE (%)	SIZE (mm)
Murata	GRM21BB30J226ME38	22.0	20	2.0 × 1.25 × 1.25 (EIA code: 0805)

**Table 9. Recommended Parts for Capacitor (Output, CH2 and CH4)**

VENDOR	TYPE NUMBER	CAPACITANCE (μF)	TOLERANCE (%)	SIZE (mm)
TAIYO YUDEN	JMK212BJ476MG-T	47.0	20	2.0 × 1.25 × 1.25 (EIA code: 0805)

**CH5 Description**

CH5 is the peak current-mode-controlled nonsynchronous boost converter for CCD+. The switch between inductor and power GND is integrated into the device and consists of NMOS-FET. Also, this device has a load switch between the battery and inductor and consists of NMOS-FET. The gate of the switch is controlled by a charge-pump circuit. The output voltage is programmable up to 18 V to use the feedback loop sensed by the external resistances. The output voltage is calculated by [Equation 7](#). The block diagram is shown in [Figure 6](#).

$$V_{OUT5} = (1 + R2/R1) \times 1.0 \text{ [V]} \quad (7)$$

$V_{OUT5}$ : Output voltage of CH5 [V]  
 R1, R2: Feedback resistance (see [Figure 6](#))

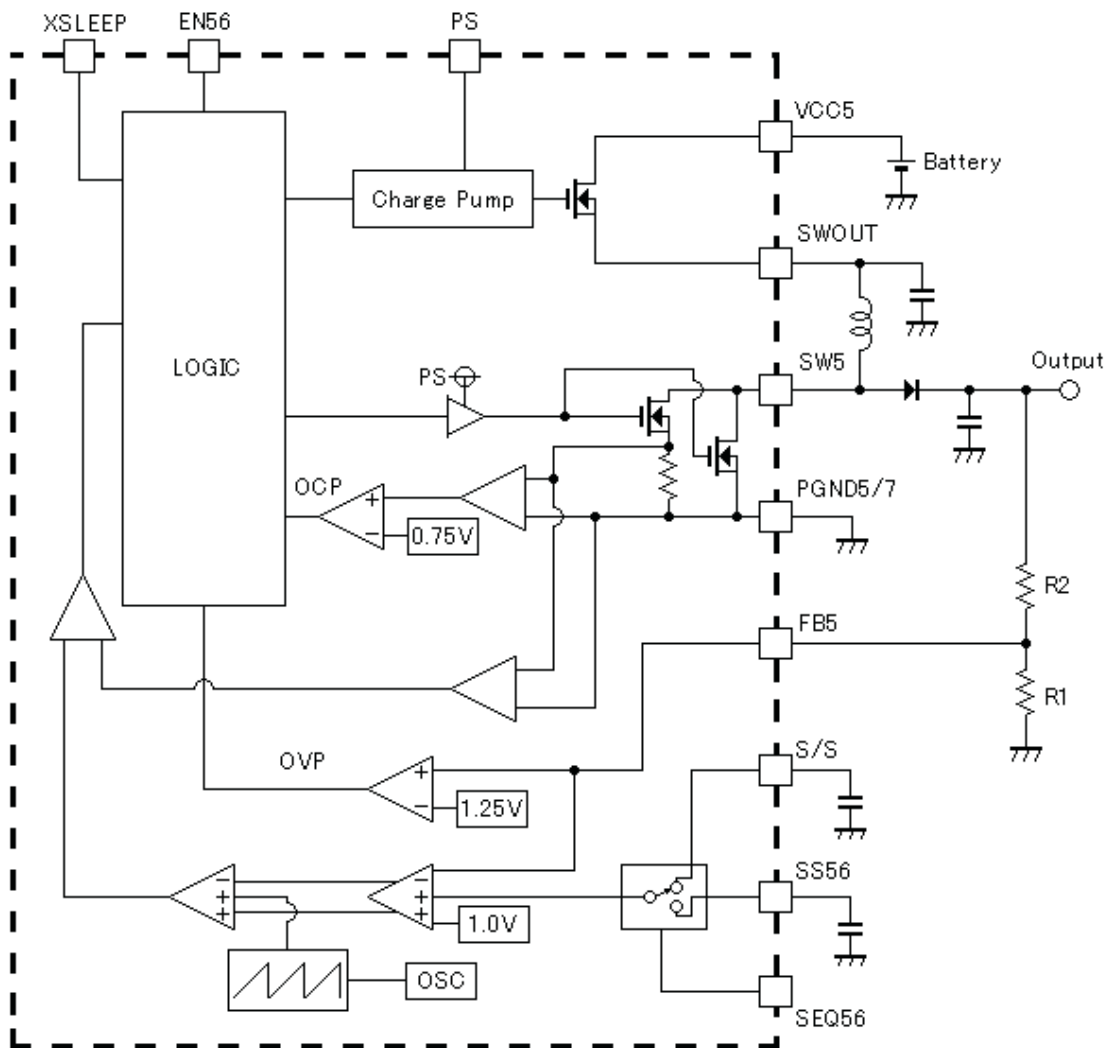


Figure 6. CH5 Block Diagram

### CH5 Recommended Parts

Table 10. Recommended Parts for Inductor (CH5)

VENDOR	TYPE NUMBER	INDUCTANCE ( $\mu\text{H}$ )	DCR ( $\text{m}\Omega$ )	SIZE (mm)
TOKO	DE2812C-1098AS-120M	12.0	340	2.8 × 3.0 × 1.2

Table 11. Recommended Parts for Capacitor (Output, CH5)

VENDOR	TYPE NUMBER	CAPACITANCE ( $\mu\text{F}$ )	TOLERANCE (%)	SIZE (mm)
Murata	GRM31CB31E106KA75	10.0	10	3.2 × 1.6 × 1.6 (EIA code: 1206)

Table 12. Recommended Parts for Capacitor (SWOUT, CH5)

VENDOR	TYPE NUMBER	CAPACITANCE ( $\mu\text{F}$ )	TOLERANCE (%)	SIZE (mm)
TDK	C2012X5R1A335M	3.3	20	2.0 × 1.25 × 1.25 (EIA code: 0805)

**Table 13. Recommended Parts for Diode (CH5)**

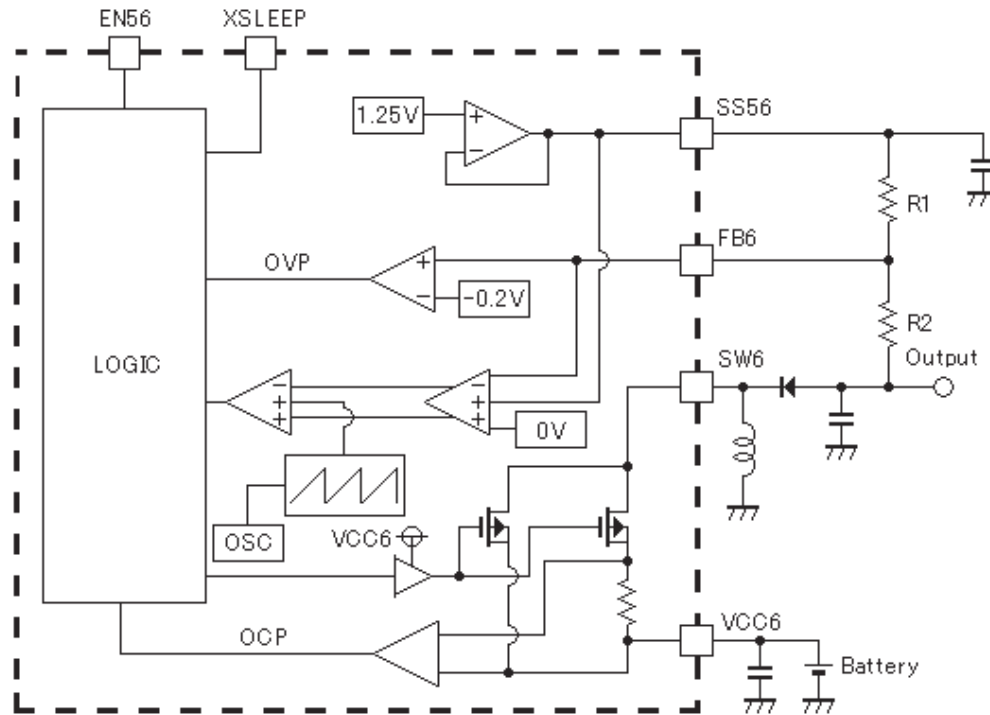
VENDOR	TAPE NUMBER	VR (V)	IF (mA)	VF (V)	CAPACITANCE (pF)	SIZE (mm)
SANYO	SB0503EJ	30	500	0.55/0.5	16.5	1.6 × 0.8 × 0.6

**CH6 Description**

CH6 is the voltage-mode-controlled nonsynchronous inverting converter for CCD-. The switch between the input voltage and inductor is integrated into the device and consists of PMOS-FET. It is acceptable to connect the battery to V<sub>CC6</sub> (pin 42) directly when the battery voltage is more than 2.5 V. When the battery voltage is less than 2.5 V, the CH8 output should be connected to V<sub>CC6</sub> (pin 42). The output voltage is programmable from -10 V to -5 V to use the feedback loop sensed by the external resistances. The output voltage is calculated by Equation 8. The block diagram is shown in Figure 7.

$$V_{OUT6} = 1.25 - (1 + R2/R1) \times 1.25 \text{ [V]} \tag{8}$$

V<sub>OUT6</sub> : Output voltage of CH6 [V]  
 R1, R2: Feedback resistance (see Figure 7)



**Figure 7. CH6 Block Diagram**

**CH6 Recommended Parts**

**Table 14. Recommended Parts for Inductor (CH6)**

VENDOR	TYPE NUMBER	INDUCTANCE (μH)	DCR (mΩ)	SIZE (mm)
TOKO	DE2815C-1071AS-120M	12.0	240	2.8 × 3.0 × 1.2

**Table 15. Recommended Parts for Capacitor (Input, CH6)**

VENDOR	TYPE NUMBER	CAPACITANCE (μF)	TOLERANCE (%)	SIZE (mm)
Murata	GRM21BB31A106KE18	10.0	10	2.0 × 1.25 × 1.25 (EIA code: 0805)

**Table 16. Recommended Parts for Capacitor (Output, CH6)**

VENDOR	TYPE NUMBER	CAPACITANCE (μF)	TOLERANCE (%)	SIZE (mm)
Murata	GRM31CB31E106KA75	10.0	10	3.2 × 1.6 × 1.6 (EIA code: 1206)

**Table 17. Recommended Parts for Diode (CH6)**

VENDOR	TAPE NUMBER	VR (V)	IF (mA)	VF (V)	CAPACITANCE (pF)	SIZE (mm)
SANYO	SB0503EJ	30	500	0.55/0.5	16.5	1.6 × 0.8 × 0.6

## CH7 Description

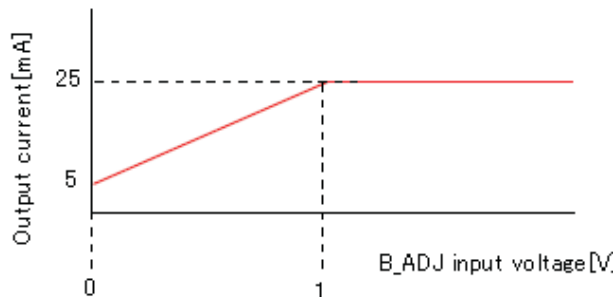
CH7 is the voltage-mode-controlled nonsynchronous boost converter for the back-light LED. The switch between the inductor and power GND is integrated into the device and consists of NMOS-FET. Also, this device has a load switch to control the output current and consists of NMOS-FET. The output current is constant and is calculated by Equation 9. It is controlled by the B\_ADJ (pin 32) input voltage as shown in Figure 8. The B\_ADJ input voltage is required as an analog input. When it is required to input PWM signal for B\_ADJ (pin 32), the RC filter is needed.

$$I_{LED} = \frac{0.2}{R_{SENSE}} \cdot V_{BADJ} + \frac{0.05}{R_{SENSE}} \quad (9)$$

$I_{LED}$ : Output current of CH7 [A]

$R_{SENSE}$ : Sense resistor between FBC and PGND5/7 [Ω]

$V_{BADJ}$ : B\_ADJ input voltage ( $0 < V_{BADJ} < 1$ ) [V]



**Figure 8. Output Current vs B\_ADJ Input Voltage (RSENSE = 10 Ω)**

The principle of the operation is to adjust the duty cycle of the MOSFET. When the B\_ADJ (pin 32) input voltage is changed, the level of “A” point shown in Figure 9 is changed to get the desired duty cycle compared to the sense current.

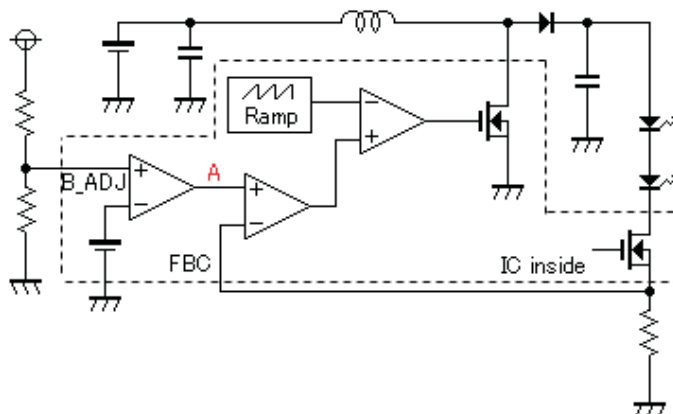


Figure 9. LED Brightness Control Block Diagram

At first, CH7 operates as pulse frequency modulation (PFM) mode at start-up. After reaching the target output voltage, CH7 operation is changed from PFM mode to pulse width modulation (PWM) mode automatically. The output voltage is programmable up to 20 V to use the feedback loop sensed by the external resistances. The maximum output voltage is calculated by Equation 10. The block diagram is shown in Figure 10.

$$V_{OUT7\ MAX} = 1 + (R2/R1) \times 1.25 \text{ [V]} \tag{10}$$

$V_{OUT7\ MAX}$ : Maximum output voltage of CH7 [V]  
 R1, R2: Feedback resistance (see Figure 10)

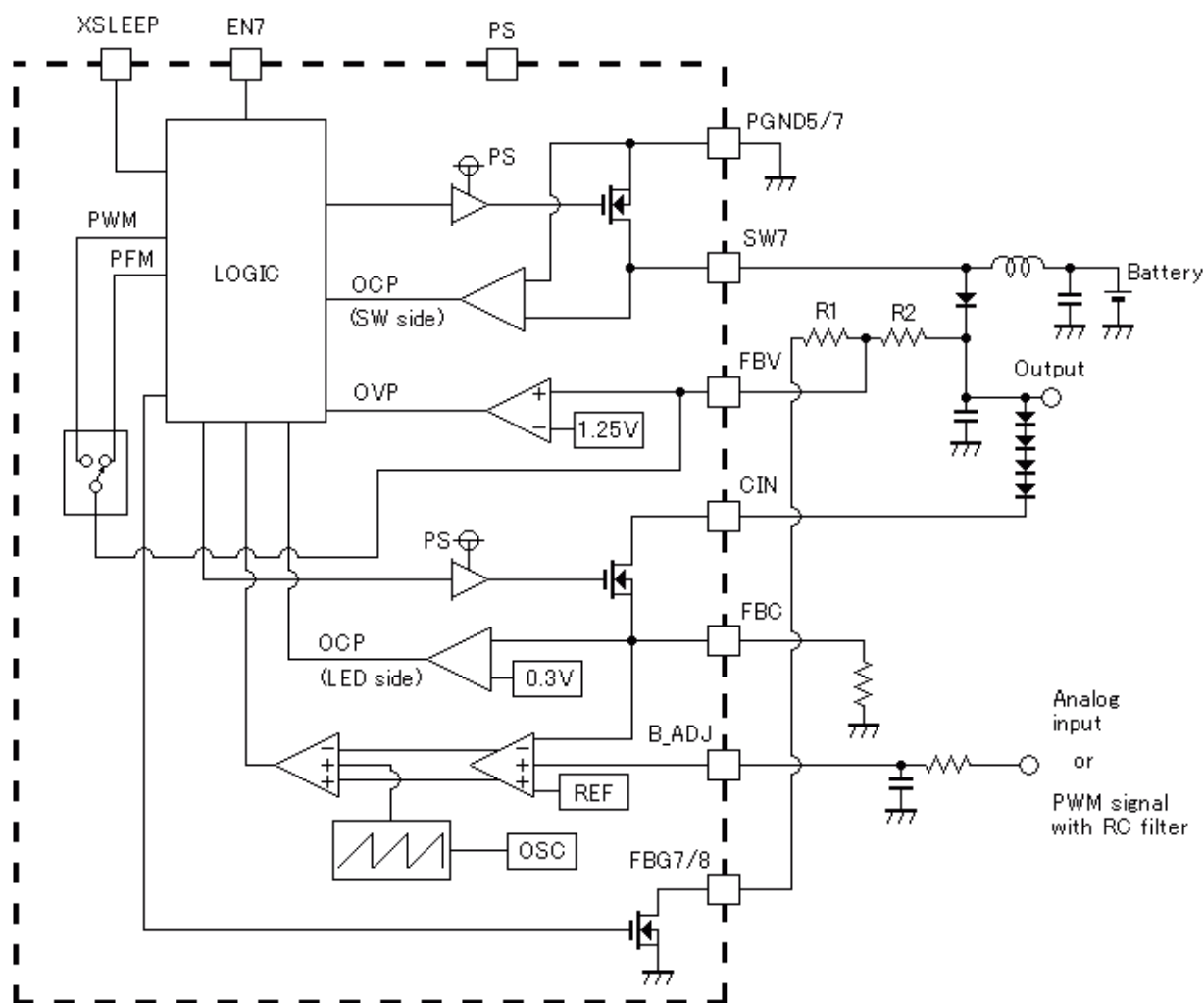


Figure 10. CH7 Block Diagram

## CH7 Recommended Parts

Table 18. Recommended Parts for Inductor (CH7)

VENDOR	TYPE NUMBER	INDUCTANCE ( $\mu\text{H}$ )	DCR ( $\text{m}\Omega$ )	SIZE (mm)
TOKO	DE2815C-1071AS-120M	12.0	240	2.8 × 3.0 × 1.2

Table 19. Recommended Parts for Capacitor (Input, CH7)

VENDOR	TYPE NUMBER	CAPACITANCE ( $\mu\text{F}$ )	TOLERANCE (%)	SIZE (mm)
Murata	GRM21BB31A106KE18	10.0	10	2.0 × 1.25 × 1.25 (EIA code: 0805)

Table 20. Recommended Parts for Diode (CH7)

VENDOR	TAPE NUMBER	VR[V]	IF[mA]	VF[V]/IF[A]	CAPACITANCE ( $\mu\text{F}$ )	SIZE (mm)
SANYO	SB0503EJ	30	500	0.55/0.5	16.5	1.6 × 0.8 × 0.6

**Table 21. Recommended Parts for Capacitor (Output, CH7)**

VENDOR	TYPE NUMBER	CAPACITANCE (μF)	TOLERANCE (%)	SIZE (mm)
Murata	GRM31CB31E106KA75	10.0	10	3.2 × 1.6 × 1.6 (EIA code: 1206)

## CH8 Description

CH8 uses an external FET. It is based on voltage-mode-controlled synchronous boost converter topology used for motor control and an IC inside driver. CH8 output should connect to PS (pin 29) because PS (pin 29) is the path to supply the power for the driver of each channel. This channel has two operation modes – PWM and PFM. The operation depends on the XSELLP (pin 7) and ENAFE (pin 6) signal level.

When XSLEEP turns high, CH8 operates as PWM mode. The ENAFE (pin 6) signal level does not matter. For start-up (less than 2.5 V at CH8 output), CH8 operates as WAKE mode to use the internal MOSFET switch connected to LL8 (pin 27). The duty cycle of WAKE mode is fixed. After PS (pin 29) voltage reaches 2.5 V, CH8 operation is changed from WAKE mode to PFM mode automatically. PFM mode is driven by the external MOSFET switch. When PS (pin 29) voltage reaches 90% of the target voltage, the operation mode is changed from PFM mode to PWM mode automatically. To operate CH8 in PFM mode only, XSLEEP (pin 7) must be high at first. After that, XSLEEP (pin 7) goes low and ENAFE (pin 6) is high for PFM mode. PFM operation is recommended for the IC drive only from an efficiency point of view.

CH8 has the reversed current protection to monitor the different voltage between LL8 (pin 27) and PS (pin 29). The protection monitors the difference between both PFM mode and PWM mode. When LL8 (pin 27) voltage is larger than PS (pin 29) voltage, the function is activated. When the function is activated, SW8HD (pin 28) level is changed from high to low; SW8LD (pin 26) level stays low. This means that LL8 voltage converges the battery voltage naturally.

The recovery condition is dependent on the operation mode. When CH8 operates as PFM mode, the condition is that FB8 (pin 30) voltage is less than 1.25 V. When CH8 operates as PWM mode, the condition is that LL8 (pin 27) voltage is smaller than PS (pin 29) voltage at the rising edge of the internal clock.

The output voltage is programmable from 3.3 V to 5.5 V to use the feedback loop sensed by the external resistances. The output voltage is calculated by [Equation 11](#). The block diagram is shown in [Figure 11](#).

$$V_{OUT8} = (1 + R1/R2) \times 1.25 \text{ [V]} \quad (11)$$

$V_{OUT8}$ : Output voltage of CH8 [V]  
R1, R2: Feedback resistance (see [Figure 11](#))



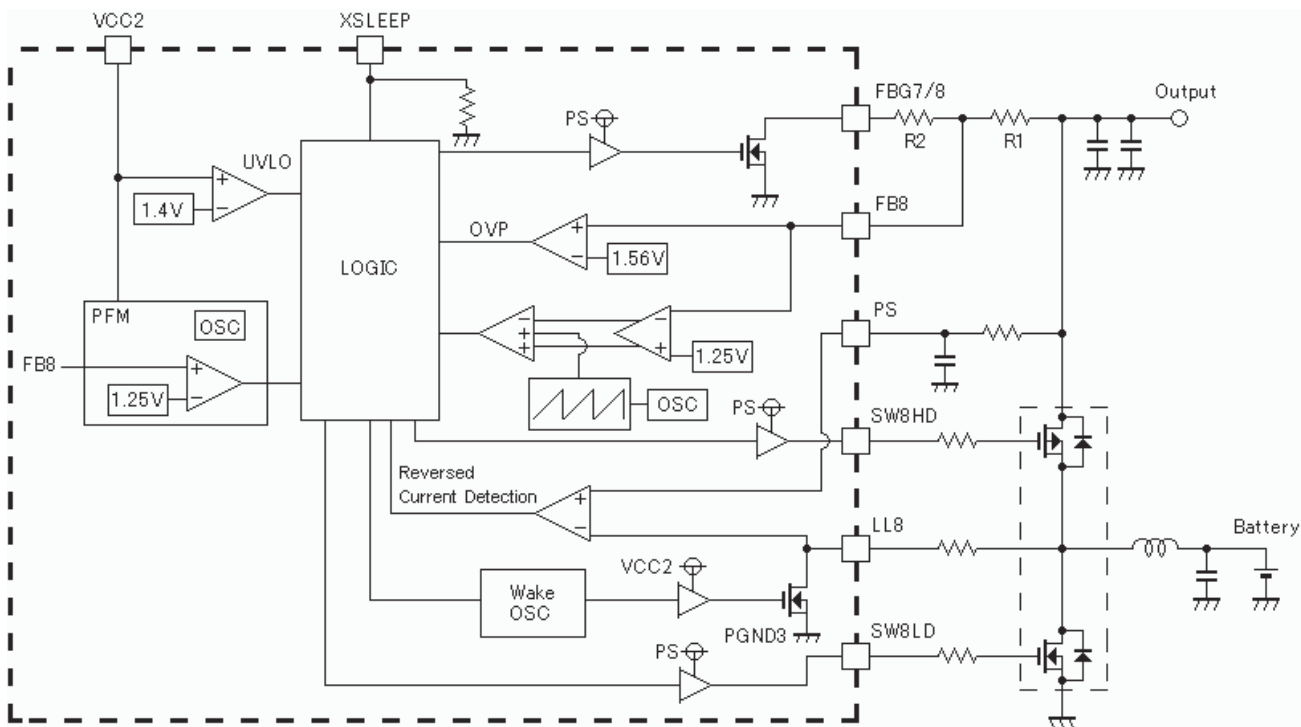


Figure 11. CH8 Block Diagram

## CH8 Recommended Parts

### For Motor Control and IC Inside Driver

Table 22. Recommended Parts for Inductor (CH8)

VENDOR	TYPE NUMBER	INDUCTANCE ( $\mu\text{H}$ )	DCR ( $\text{m}\Omega$ )	SIZE (mm)
TOKO	DE4518-1124-4R3M	4.3	54	4.5 × 4.7 × 1.8

Table 23. Recommended Parts for Capacitor (Input, CH8)

VENDOR	TYPE NUMBER	CAPACITANCE ( $\mu\text{F}$ )	TOLERANCE (%)	SIZE (mm)
TDK	C3216X5R0J226M	22.0 × 2pcs	20	3.2 × 1.6 × 0.85 (EIA code: 1206)

Table 24. Recommended Parts for Capacitor (Output, CH8)

VENDOR	TYPE NUMBER	CAPACITANCE ( $\mu\text{F}$ )	TOLERANCE (%)	SIZE (mm)
Murata	GRM31MB31A106KE18	10.0 × 2pcs	10	3.2 × 1.6 × 1.15 (EIA code: 1206)

Table 25. Recommended Parts for FET(CH8)

VENDOR	TYPE NUMBER	ID (DC) (N-ch) (A)	ID (DC) (P-ch) (A)	Rds(on) (N-ch) ( $\Omega$ )	Rds(on) (P-ch) ( $\Omega$ )	QG (N-ch) (nC)	QG (P-ch) (nC)
Sanyo	VEC2607	4.5	-4.0	0.032 / 4V	0.037/-4.5V	7.6	11.0
	VEC2611	3.0	-2.6	0.053 / 4V	0.080/-4.5V	8.8	6.5

**For IC Inside Driver Only****Table 26. Recommended Parts for Inductor (CH8)**

VENDOR	TYPE NUMBER	INDUCTANCE ( $\mu$ H)	DCR (m $\Omega$ )	SIZE (mm)
Yuden	LB2518T330	33	700	1.8 × 2.5 × 1.8

**Table 27. Recommended Parts for Capacitor (Input, CH8)**

VENDOR	TYPE NUMBER	CAPACITANCE ( $\mu$ F)	TOLERANCE (%)	SIZE (mm)
TDK	C3216X5R0J226M	22	20	3.2 × 1.6 × 0.85 (EIA code: 1206)

**Table 28. Recommended Parts for Capacitor (Output, CH8)**

VENDOR	TYPE NUMBER	CAPACITANCE ( $\mu$ F)	TOLERANCE (%)	SIZE (mm)
TDK	C1608X5R0J475M	4.7	20	1.6 × 0.8 × 0.8 (EIA code: 0603)

**Table 29. Recommended Parts for FET (CH8)**

VENDOR	TYPE NUMBER	ID (DC) (N-ch) (A)	ID (DC) (P-ch) (A)	Rds(on) (N-ch) ( $\Omega$ )	Rds(on) (P-ch) ( $\Omega$ )	QG (N-ch) (nQ)	QG (P-ch) (nQ)
ON-SEMI	NTZD3155C	0.54	–0.43	0.4 / 4.5V	0.5 / –4.5V	1.5	1.7
Sanyo	SCH2615	1.2	–0.9	0.28 / 4V	0.47 / –4.5V	1.15	1.43

**Layout Consideration**

To avoid ground shift problems due to the high currents in the switches, separate AGND (pin 10) from PGND1 (pin 20), PGND2 (pin 14), PGND3 (pin 25), PGND4 (pin 2), and PGND5/7 (pin 37). The reference GND for all control signals, such as XSLEEP, is AGND (pin 10). The power switches inside the IC are connected to PGND1 (pin 20), PGND2 (pin 14), PGND3 (pin 25), PGND4 (pin 2), and PGND5/7 (pin 37). Both grounds must be connected on the PCB (ideally at only one point).

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS65530RSLR	ACTIVE	QFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65530RSLT	ACTIVE	QFN	RSL	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

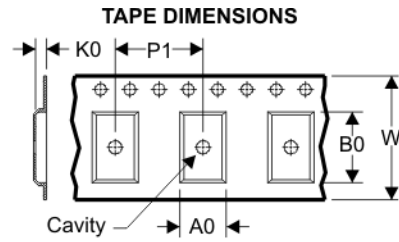
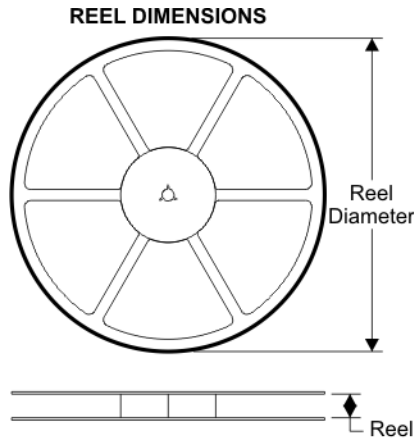
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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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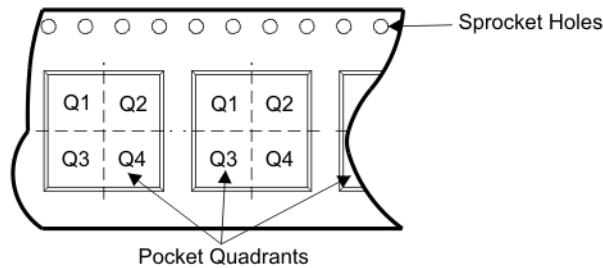
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**TAPE AND REEL BOX INFORMATION**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65530RSLR	RSL	48	SITE 41	330	16	6.3	6.3	1.5	12	16	Q2
TPS65530RSLT	RSL	48	SITE 41	180	16	6.3	6.3	1.5	12	16	Q2

**TAPE AND REEL BOX DIMENSIONS**



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS65530RSLR	RSL	48	SITE 41	346.0	346.0	33.0
TPS65530RSLT	RSL	48	SITE 41	190.0	212.7	31.75

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