Programmable High-Frequency Crystal Oscillator (XO)

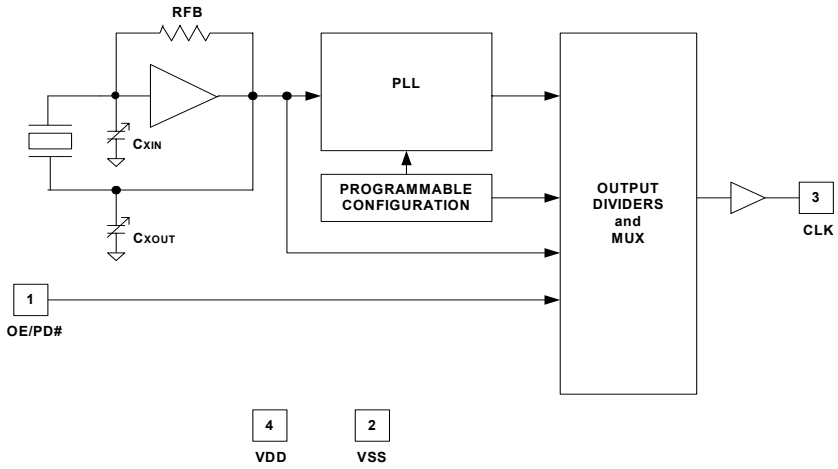
Features

- Programmable High-frequency Crystal Oscillator (XO)
- Wide output (CLK) range from:
  - 1.0 to 125 MHz (V_{DD} = 5.0V)
  - 1.0 to 90 MHz (V_{DD} = 3.3V)
- Integrated phase-locked loop (PLL)
- Low cycle-to-cycle Jitter
- 3.3/5.0V operation
- Output Enable function
- Power-down function
- Refer to CY25701 for SSCG function
- Lead-free package

Benefits

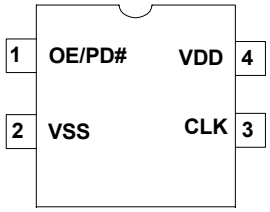
- Eliminates the need for external crystal oscillator.
- Internal PLL to generate up to 125-MHz output.
- Suitable for most PC, consumer and networking applications.
- Application compatibility in standard and low-power systems.
- CY25701 can be used as a direct replacement in 3.3V applications if Spread Spectrum Clock (SSC) is required for EMI reduction without any PCB modification.
- In-house programming of samples and prototype quantities is available using the CY3672 programming kit and CY36xx socket adapter. Sample and production quantities are available through Cypress's value-added distribution partners.

Logic Block Diagram



Pin Configuration

CY25702
4-pin Plastic SMD



Pin Definition

Pin	Name	Description
1	OE/PD#	**Output Enable pin**: **Active HIGH**. If OE = 1, CLK is enabled. **Power Down pin**: **Active LOW**. If PD# = 0, Power Down is enabled.
2	VSS	**Power supply ground**.
3	CLK	**Clock output**.
4	VDD	**3.3V or 5.0V power supply**.

Table 1. Programming Data Requirement

Pin Function	Output Frequency	Output Enable/Power Down	Power Supply
Pin Name	CLK	OE/PD#	VDD
Pin#	3	1	4
Units	MHz	N/A	V
Program Value	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**

Functional Description

The CY25702 is a Crystal Oscillator (XO).

The device uses a Cypress proprietary PLL to synthesize the frequency of the embedded input crystal.

The CY25702 uses a programmable configuration memory array to synthesize output frequency.

The frequency CLK output can be programmed from 10–125 MHz.

The CY25702 is available in a 4-pin plastic SMD packages with operating temperature range of –20 to 70°C.

Programming Description

Field/Factory-Programmable CY25702

Field/Factory programming is available for samples and manufacturing by Cypress and its distributors. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. Once the request has been processed, you will receive a new part number, samples, and data sheet with the programmed values. This part number will be used for additional sample requests and production orders.

Additional information on the CY25702 can be obtained from the Cypress web site at www.cypress.com.

Output Frequency, CLK Output (CLK, pin 3)

The frequency at the CLK output is produced by synthesizing the embedded crystal oscillator frequency input. The range of synthesized clock is from 1–125 MHz when V_{DD} = 5V and 1–90 MHz when V_{DD} = 3.3V.

Output Enable or Power Down (OE/PD#, pin 1)

Pin 1 can be programmed as either output enable (OE) or Power Down (PD#).

Absolute Maximum Rating

Supply Voltage (V_{DD}).....–0.5V to +7.0V

DC Input Voltage ..... –0.5V to V_{DD} + 0.5V

Storage Temperature (Non-condensing) .... –55°C to +100°C

Junction Temperature..... –40°C to +125°C

Data Retention @ Tj = 125°C.....> 10 years

Package Power Dissipation..... 350 mW

Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD1}	Supply Voltage Range	3.00	3.30	3.60	V
V_{DD2}	Supply Voltage Range	4.50	5.00	5.50	V
T_A	Ambient Temperature	–20	–	70	°C
C_{LOAD}	Max. Load Capacitance @ pin 3	–	–	15	pF
F_{CLK1}	CLK output frequency, C_{LOAD} = 15 pF, V_{DD} = 5.0V	1.0	–	125	MHz
F_{CLK2}	CLK output frequency, C_{LOAD} = 15 pF, V_{DD} = 3.3V	1.0	–	90	MHz
T_{PU}	Power-up time for VDD to reach minimum specified voltage (power ramp must be monotonic)	0.05	–	500	ms

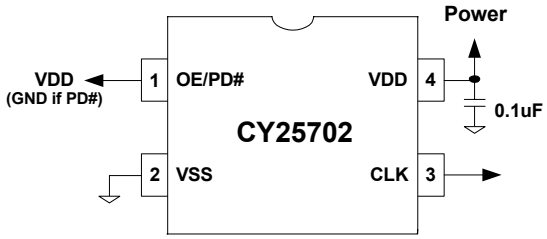
DC Electrical Characteristics

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{OH1}	High Output Voltage	V_{DD} = 5.0V, I_{OH} = –16 mA	V_{DD} – 0.4	–	–	V
V_{OL1}	Low Output Voltage	V_{DD}= 5.0V, I_{OL}= 16 mA	–	–	0.4	V
V_{OH2}	High Output Voltage	V_{DD} = 3.3V, I_{OH} = –8 mA	V_{DD} – 0.4	–	–	V
V_{OL2}	Low Output Voltage	V_{DD}= 3.3V, I_{OL} = 8 mA	–	–	0.4	V
V_{IH1}	Input High Voltage (pin 1)	V_{DD} = 5.0V	2.0	–	–	V
V_{IL1}	Input Low Voltage (pin 1)	V_{DD} = 5.0V	–	–	0.8	V
V_{IH2}	Input High Voltage (pin 1)	V_{DD} = 3.3V	0.7V_{DD}	–	–	V
V_{IL2}	Input Low Voltage (pin 1)	V_{DD} = 3.3V	–	–	0.2V_{DD}	V
I_{IH}	Input High Current (pin 1)	V_{in} = V_{DD}	–	–	10	µA
I_{IL}	Input Low Current (pin 1)	V_{in} = V_{SS}	–	–	10	µA
I_{OZ}	Output Leakage Current (pin 3)	Three-state output, OE = 0	–10	–	10	µA
C_{IN}	Input Capacitance (pin 1)	Pin 1, OE or PD#	–	5	7	pF
I_{VDD1}	Supply Current	V_{DD} = 3.3V, CLK = 1 to 90 MHz, C_{LOAD} = 0, OE = V_{DD}	–	–	28	mA
I_{VDD2}	Supply Current	V_{DD} = 3.3V, CLK = 1 to 90 MHz, C_{LOAD} = 0, OE = GND	–	–	16	mA
I_{VDD3}	Supply Current	V_{DD} = 5.0V, CLK = 1 to 125 MHz, C_{LOAD} = 0, OE = V_{DD}	–	–	45	mA
I_{VDD4}	Supply Current	V_{DD} = 5.0V, CLK = 1 to 125 MHz, C_{LOAD} = 0, OE = GND	–	–	30	mA
$I_{PD\#}$	Power Down Current	PD# = GND	–	–	50	µA
FS	Frequency Stability	–20 to +70°C	–50	–	50	ppm
AG	Aging	Ta = 25°C, First Year	–5	–	5	ppm
SR	Shock Resistance	Three drops on a hard board from 750 mm or excitation test with 29.400m/s^2 x 0.3ms x 1/2 sinewave in three directions	–20	–	20	ppm

AC Electrical Characteristics

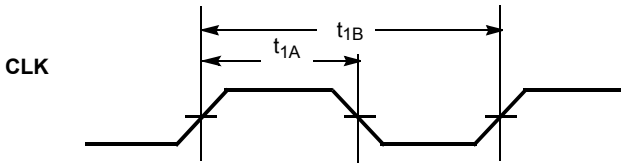
Parameter	Description	Condition	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	CLK, Measured at V_{DD}/2	40	50	60	%
t_R	Output Rise Time	20%–80% of V_{DD}, C_L = 15 pF	–	–	4.0	ns
t_F	Output Fall Time	20%–80% of V_{DD}, C_L = 15 pF	–	–	4.0	ns
T_{OE1}	Output Disable Time (pin1 = OE)	Time from falling edge on OE to stopped outputs (Asynchronous)	–	150	350	ns
T_{OE2}	Output Enable Time (pin1 = OE)	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	150	350	ns
T_{LOCK}	PLL Lock Time	Time for CLK to reach valid frequency	–	–	10	ms
T_{SU}	Start-up time out of Power Down	PD# pin Low to High	–	–	5	ms
T_{PDD}	Power Down Delay Time	PD# pin Low to CLK Low (Asynchronous)	–	–	25	ns
t_{J1}	Cycle-to-cycle jitter V_{DD} = 3.3V	1.0 MHz ≤ fo ≤ 125 MHz, C_L = 15 pF	–	–	200	ps
t_{J2}	Cycle-to-cycle jitter V_{DD} = 5.0V	33 MHz ≤ fo ≤ 125 MHz, C_L = 15 pF	–	–	150	ps
		1.0 MHz ≤ fo ≤ 33 MHz, C_L = 15 pF	–	–	200	ps

Application Circuit

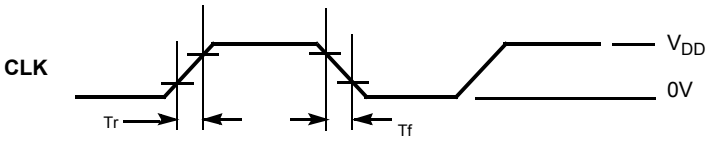


Switching Waveforms

Duty Cycle Timing (DC = t_{1A}/t_{1B})

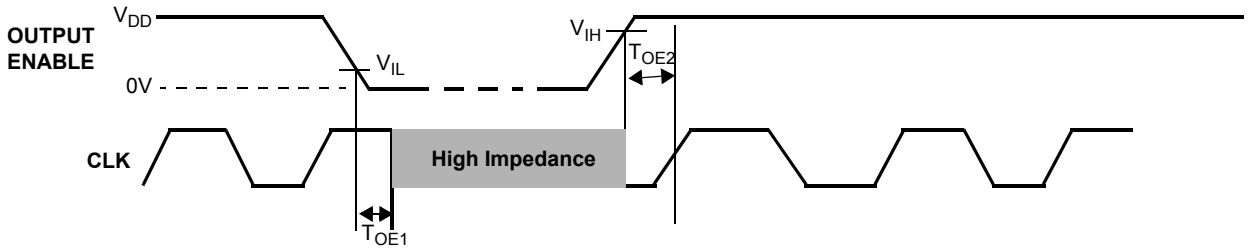


Output Rise/Fall Time



Output Rise time (Tr) = 20 to 80% of V_{DD}
Output Fall time (Tf) = 80 to 20% of V_{DD}

Output Enable/Disable Timing

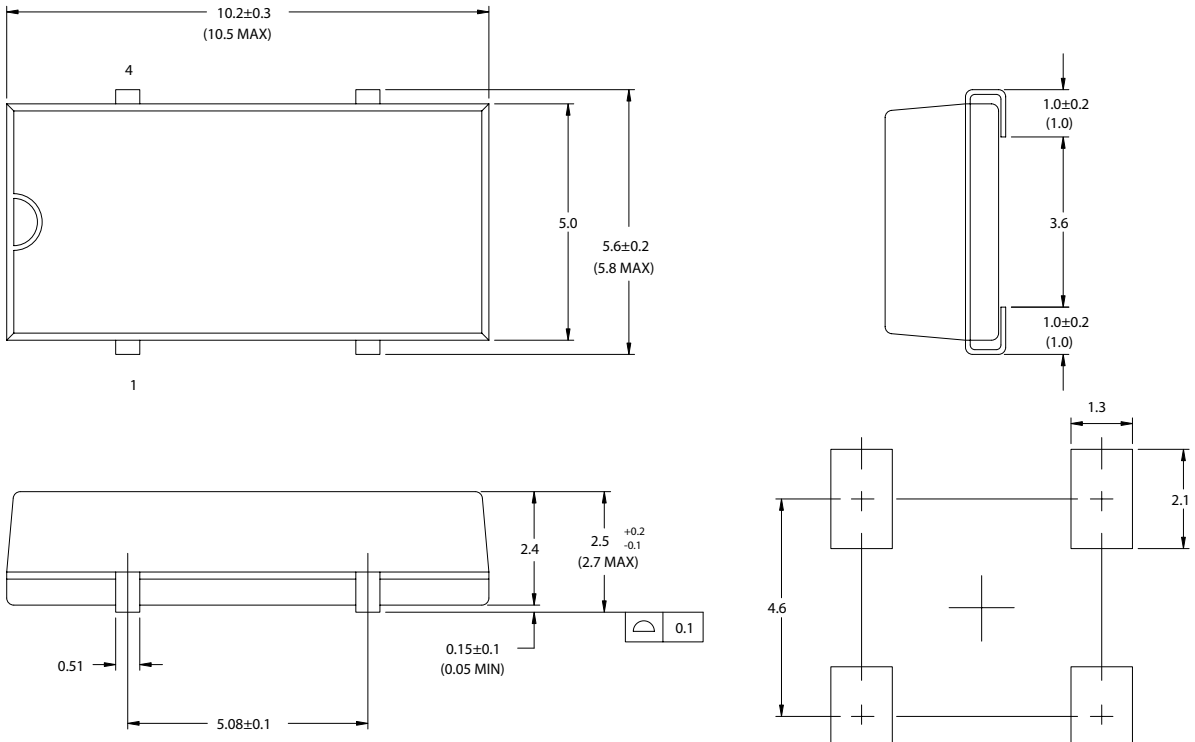


Ordering Information

Part Number[1,2]	Package description	Product Flow
CY25702JXCZZZZ	4-Lead Plastic JE04A SMD – Lead-free	Commercial, –20° to 70°C
CY25702JXCZZZZT	4-Lead Plastic JE04A SMD, Tape and Reel – Lead-free	Commercial, –20° to 70°C
CY25702FJXC	4-Lead Plastic JE04A SMD – Lead-free	Commercial, –20° to 70°C
CY25702FJXCT	4-Lead Plastic JE04A SMD, Tape and Reel – Lead-free	Commercial, –20° to 70°C
CY25702XCZZZ	4-Lead Plastic JE04B SMD – Lead-free	Commercial, –20° to 70°C
CY25702XCZZZT	4-Lead Plastic JE04B SMD, Tape and Reel – Lead-free	Commercial, –20° to 70°C
CY25702FXC	4-Lead Plastic JE04B SMD – Lead-free	Commercial, –20° to 70°C
CY25702FXCT	4-Lead Plastic JE04B SMD, Tape and Reel – Lead-free	Commercial, –20° to 70°C

Package Drawings and Dimensions

4-Lead JEC JE04A



DIMENSIONS IN MILLIMETERS

REFERENCE JEDEC: N/A

PKG. WEIGHT: 0.24 gms

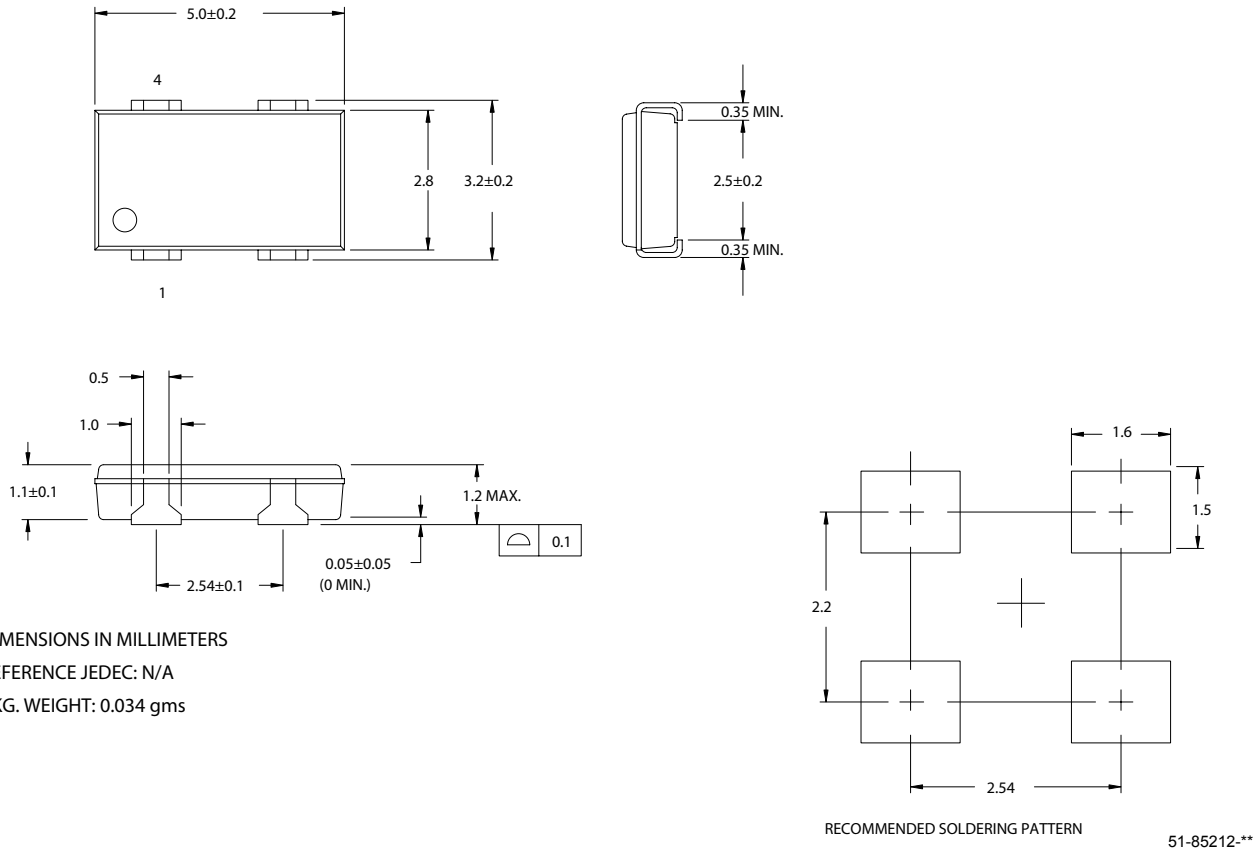
RECOMMENDED SOLDERING PATTERN

51-85204-*A

Notes:
1. "ZZZZ" or "ZZZ" denotes the assigned product dash number. This number will be assigned by factory after the output frequency and spread percent programming data is received from the customer.
2. "FJXC" or "FX" suffix is used for products programmed in field by Cypress distributors.

Package Drawings and Dimensions (continued)

4-Lead JE (5.0 x 2.8 MM) JE04B



DIMENSIONS IN MILLIMETERS

REFERENCE JEDEC: N/A

PKG. WEIGHT: 0.034 gms

RECOMMENDED SOLDERING PATTERN

51-85212-**

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Document History Page

Document Title: CY25702 Programmable High-Frequency Crystal Oscillator (XO) Document Number: 38-07721				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	296081	See ECN	RGL	New data sheet
*A	333298	See ECN	RGL	Added Jitter Specifications Corrected the Ordering Information table to match the DevMaster