

TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

## 256-MBIT (32M × 8 BITS) CMOS NAND E<sup>2</sup>PROM

### DESCRIPTION

The TC58256A is a single 3.3 V 256-Mbit (276,824,064) bit NAND Electrically Erasable and Programmable Read-Only Memory (NAND E<sup>2</sup>PROM) organized as 528 bytes × 32 pages × 2048 blocks. The device has a 528-byte static register which allows program and read data to be transferred between the register and the memory cell array in 528-byte increments. The Erase operation is implemented in a single block unit (16 Kbytes + 512 bytes: 528 bytes × 32 pages).

The TC58256A is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

### FEATURES

- Organization
  - Memory cell array 528 × 64K × 8
  - Register 528 × 8
  - Page size 528 bytes
  - Block size (16K + 512) bytes
- Modes
  - Read, Reset, Auto Page Program
  - Auto Block Erase, Status Read
- Mode control
  - Serial input/output
  - Command control
- Power supply VCC = 2.7 V to 3.6 V
- Program/Erase Cycles 1E5 cycle (with ECC)
- Access time
  - Cell array to register 25 μs max
  - Serial Read Cycle 50 ns min
- Operating current
  - Read (50 ns cycle) 10 mA typ.
  - Program (avg.) 10 mA typ.
  - Erase (avg.) 10 mA typ.
  - Standby 100 μA
- Package
  - TSOP148-P-1220-0.50 (Weight: 0.53 g typ.)

### PIN ASSIGNMENT (TOP VIEW)

|               |      |   |    |        |
|---------------|------|---|----|--------|
| NC            | □ 1  | ○ | 48 | □ NC   |
| NC            | □ 2  |   | 47 | □ NC   |
| NC            | □ 3  |   | 46 | □ NC   |
| NC            | □ 4  |   | 45 | □ NC   |
| NC            | □ 5  |   | 44 | □ I/O8 |
| GND           | □ 6  |   | 43 | □ I/O7 |
| RY/ <u>BY</u> | □ 7  |   | 42 | □ I/O6 |
| <u>RE</u>     | □ 8  |   | 41 | □ I/O5 |
| <u>CE</u>     | □ 9  |   | 40 | □ NC   |
| NC            | □ 10 |   | 39 | □ NC   |
| NC            | □ 11 |   | 38 | □ NC   |
| VCC           | □ 12 |   | 37 | □ VCC  |
| VSS           | □ 13 |   | 36 | □ VSS  |
| NC            | □ 14 |   | 35 | □ NC   |
| NC            | □ 15 |   | 34 | □ NC   |
| CLE           | □ 16 |   | 33 | □ NC   |
| <u>ALE</u>    | □ 17 |   | 32 | □ I/O4 |
| <u>WE</u>     | □ 18 |   | 31 | □ I/O3 |
| <u>WP</u>     | □ 19 |   | 30 | □ I/O2 |
| NC            | □ 20 |   | 29 | □ I/O1 |
| NC            | □ 21 |   | 28 | □ NC   |
| NC            | □ 22 |   | 27 | □ NC   |
| NC            | □ 23 |   | 26 | □ NC   |
| NC            | □ 24 |   | 25 | □ NC   |

### PIN NAMES

| I/O1 to I/O8  | I/O port             |
|---------------|----------------------|
| <u>CE</u>     | Chip enable          |
| <u>WE</u>     | Write enable         |
| <u>RE</u>     | Read enable          |
| CLE           | Command latch enable |
| ALE           | Address latch enable |
| <u>WP</u>     | Write protect        |
| RY/ <u>BY</u> | Ready/Busy           |
| GND           | Ground input         |
| VCC           | Power supply         |
| VSS           | Ground               |

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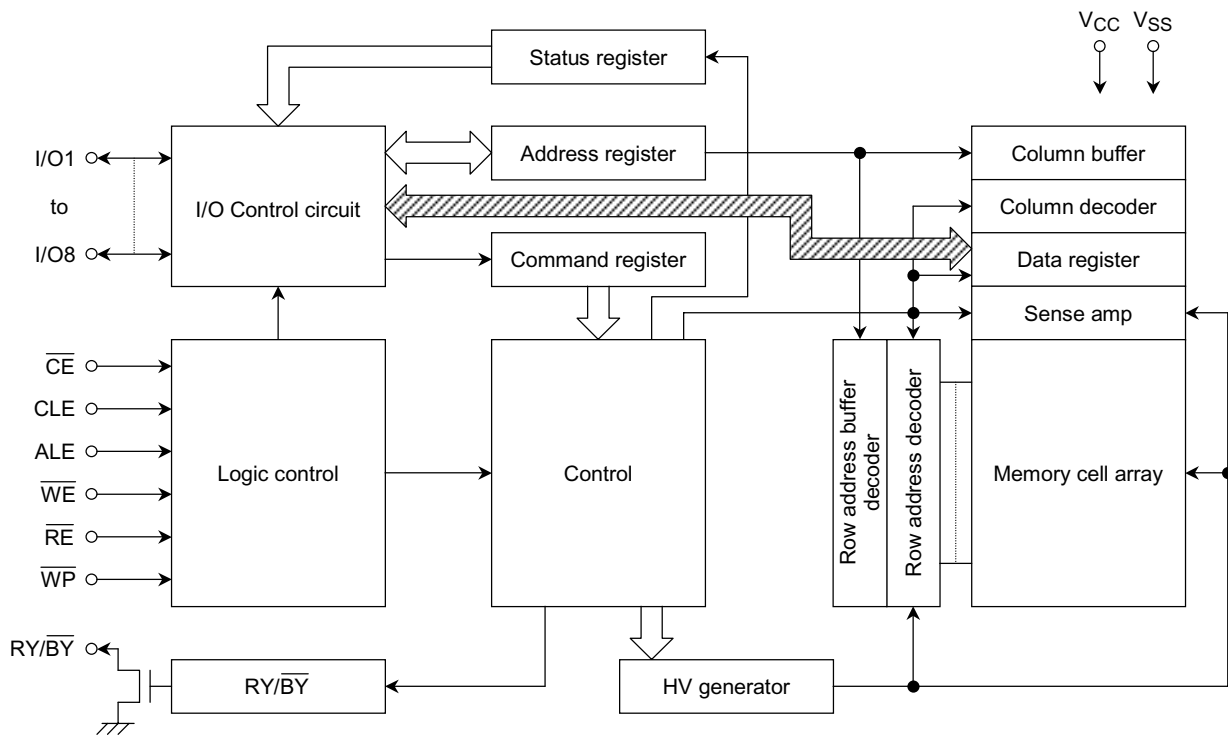
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## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| SYMBOL              | RATING                      | VALUE                                       | UNIT |
|---------------------|-----------------------------|---|------|
| V <sub>CC</sub>     | Power Supply Voltage        | -0.6 to 4.6                                 | V    |
| V <sub>IN</sub>     | Input Voltage               | -0.6 to 4.6                                 | V    |
| V <sub>I/O</sub>    | Input/Output Voltage        | -0.6 V to V <sub>CC</sub> + 0.3 V (≤ 4.6 V) | V    |
| P <sub>D</sub>      | Power Dissipation           | 0.3   | W    |
| T <sub>solder</sub> | Soldering Temperature (10s) | 260   | °C   |
| T <sub>stg</sub>    | Storage Temperature         | -55 to 150                                  | °C   |
| T <sub>opr</sub>    | Operating Temperature       | 0 to 70                                     | °C   |

## CAPACITANCE \*(Ta = 25°C, f = 1 MHz)

| SYMBOL           | PARAMETER | CONDITION              | MIN | MAX | UNIT |
|------------------|-----------|------------------------|-----|-----|------|
| C <sub>IN</sub>  | Input     | V <sub>IN</sub> = 0 V  | —   | 10  | pF   |
| C <sub>OUT</sub> | Output    | V <sub>OUT</sub> = 0 V | —   | 10  | pF   |

\* This parameter is periodically sampled and is not tested for every device.

## VALID BLOCKS (1)

| SYMBOL   | PARAMETER              | MIN  | TYP. | MAX  | UNIT   |
|----------|------------------------|------|------|------|--------|
| $N_{VB}$ | Number of Valid Blocks | 2008 | —    | 2048 | Blocks |

(1) The TC58256A occasionally contains unusable blocks. Refer to Application Note (14) toward the end of this document.

## RECOMMENDED DC OPERATING CONDITIONS

| SYMBOL   | PARAMETER                | MIN   | TYP. | MAX            | UNIT |
|----------|--------------------------|-------|------|----------------|------|
| $V_{CC}$ | Power Supply Voltage     | 2.7   | 3.3  | 3.6            | V    |
| $V_{IH}$ | High Level input Voltage | 2.0   | —    | $V_{CC} + 0.3$ | V    |
| $V_{IL}$ | Low Level Input Voltage  | -0.3* | —    | 0.8            | V    |

\* -2 V (pulse width lower than 20 ns)

## DC CHARACTERISTICS ( $T_a = 0^\circ$ to $70^\circ\text{C}$ , $V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$ )

| SYMBOL                      | PARAMETER                                 | CONDITION  | MIN | TYP. | MAX      | UNIT          |
|-----------------------------|---|--|-----|------|----------|---------------|
| $I_{IL}$                    | Input Leakage Current                     | $V_{IN} = 0\text{ V to }V_{CC}$  | —   | —    | $\pm 10$ | $\mu\text{A}$ |
| $I_{LO}$                    | Output Leakage Current                    | $V_{OUT} = 0.4\text{ V to }V_{CC}$   | —   | —    | $\pm 10$ | $\mu\text{A}$ |
| $I_{CCO1}$                  | Operating Current (Serial Read)           | $\overline{CE} = V_{IL}$ , $I_{OUT} = 0\text{ mA}$ , $t_{\text{cycle}} = 50\text{ ns}$ | —   | 10   | 30       | mA            |
| $I_{CCO3}$                  | Operating Current (Command Input)         | $t_{\text{cycle}} = 50\text{ ns}$  | —   | 10   | 30       | mA            |
| $I_{CCO4}$                  | Operating Current (Data Input)            | $t_{\text{cycle}} = 50\text{ ns}$  | —   | 10   | 30       | mA            |
| $I_{CCO5}$                  | Operating Current (Address Input)         | $t_{\text{cycle}} = 50\text{ ns}$  | —   | 10   | 30       | mA            |
| $I_{CCO7}$                  | Programming Current                       | —  | —   | 10   | 30       | mA            |
| $I_{CCO8}$                  | Erasing Current                           | —  | —   | 10   | 30       | mA            |
| $I_{CCS1}$                  | Standby Current                           | $\overline{CE} = V_{IH}$   | —   | —    | 1        | mA            |
| $I_{CCS2}$                  | Standby Current                           | $\overline{CE} = V_{CC} - 0.2\text{ V}$  | —   | —    | 100      | $\mu\text{A}$ |
| $V_{OH}$                    | High Level Output Voltage                 | $I_{OH} = -400\ \mu\text{A}$   | 2.4 | —    | —        | V             |
| $V_{OL}$                    | Low Level Output Voltage                  | $I_{OL} = 2.1\text{ mA}$   | —   | —    | 0.4      | V             |
| $I_{OL} (RY/\overline{BY})$ | Output Current of RY/ $\overline{BY}$ pin | $V_{OL} = 0.4\text{ V}$  | —   | 8    | —        | mA            |

## AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

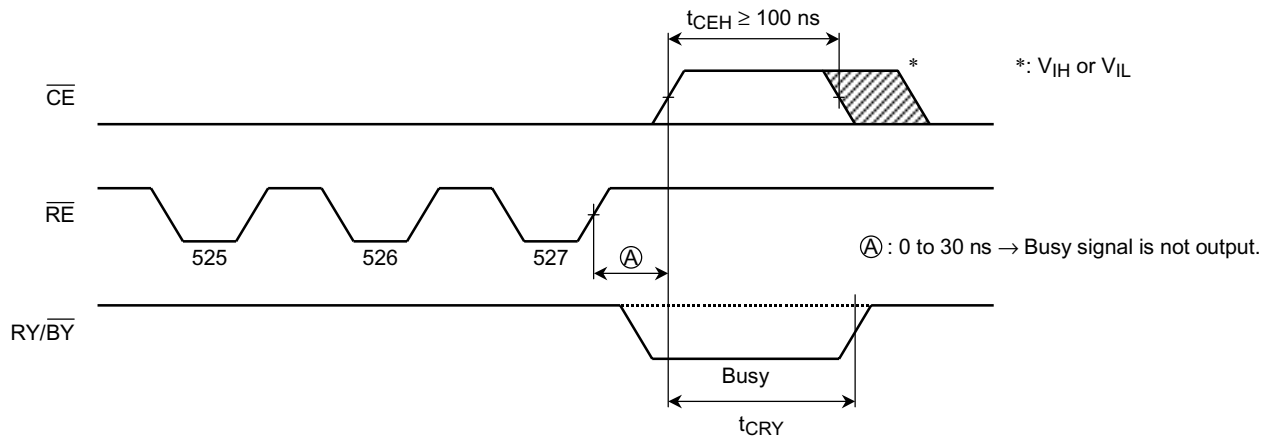
(Ta = 0° to 70°C, VCC = 2.7 V to 3.6 V)

| SYMBOL            | PARAMETER  | MIN | MAX               | UNIT | NOTES   |
|-------------------|--|-----|-------------------|------|---------|
| t <sub>CLS</sub>  | CLE Setup Time   | 0   | —                 | ns   |         |
| t <sub>CLH</sub>  | CLE Hold Time  | 10  | —                 | ns   |         |
| t <sub>CS</sub>   | $\overline{CE}$ Setup Time   | 0   | —                 | ns   |         |
| t <sub>CH</sub>   | $\overline{CE}$ Hold Time  | 10  | —                 | ns   |         |
| t <sub>WP</sub>   | Write Pulse Width  | 25  | —                 | ns   |         |
| t <sub>ALS</sub>  | ALE Setup Time   | 0   | —                 | ns   |         |
| t <sub>ALH</sub>  | ALE Hold Time  | 10  | —                 | ns   |         |
| t <sub>DS</sub>   | Data Setup Time  | 20  | —                 | ns   |         |
| t <sub>DH</sub>   | Data Hold Time   | 10  | —                 | ns   |         |
| t <sub>WC</sub>   | Write Cycle Time   | 50  | —                 | ns   |         |
| t <sub>WH</sub>   | $\overline{WE}$ High Hold Time   | 15  | —                 | ns   |         |
| t <sub>WW</sub>   | $\overline{WP}$ High to $\overline{WE}$ Low                                      | 100 | —                 | ns   |         |
| t <sub>RR</sub>   | Ready to $\overline{RE}$ Falling Edge  | 20  | —                 | ns   |         |
| t <sub>RP</sub>   | Read Pulse Width   | 35  | —                 | ns   |         |
| t <sub>RC</sub>   | Read Cycle Time  | 50  | —                 | ns   |         |
| t <sub>REA</sub>  | $\overline{RE}$ Access Time (Serial Data Access)                                 | —   | 35                | ns   |         |
| t <sub>CEH</sub>  | $\overline{CE}$ High Time for Last Address in Serial Read Cycle                  | 100 | —                 | ns   | (2)     |
| t <sub>REAI</sub> | $\overline{RE}$ Access Time (ID Read)  | —   | 35                | ns   |         |
| t <sub>OH</sub>   | Data Output Hold Time  | 10  | —                 | ns   |         |
| t <sub>RHZ</sub>  | $\overline{RE}$ High to Output High Impedance                                    | —   | 30                | ns   |         |
| t <sub>CHZ</sub>  | $\overline{CE}$ High to Output High Impedance                                    | —   | 20                | ns   |         |
| t <sub>REH</sub>  | $\overline{RE}$ High Hold Time   | 15  | —                 | ns   |         |
| t <sub>IR</sub>   | Output-High-impedance-to- $\overline{RE}$ Rising Edge                            | 0   | —                 | ns   |         |
| t <sub>RSTO</sub> | $\overline{RE}$ Access Time (Status Read)  | —   | 35                | ns   |         |
| t <sub>CSTO</sub> | $\overline{CE}$ Access Time (Status Read)  | —   | 45                | ns   |         |
| t <sub>RHW</sub>  | $\overline{RE}$ High to $\overline{WE}$ Low                                      | 0   | —                 | ns   |         |
| t <sub>WHC</sub>  | $\overline{WE}$ High to $\overline{CE}$ Low                                      | 30  | —                 | ns   |         |
| t <sub>WHR</sub>  | $\overline{WE}$ High to $\overline{RE}$ Low                                      | 30  | —                 | ns   |         |
| t <sub>AR1</sub>  | ALE Low to $\overline{RE}$ Low (ID Read)   | 100 | —                 | ns   |         |
| t <sub>CR</sub>   | $\overline{CE}$ Low to $\overline{RE}$ Low (ID Read)                             | 100 | —                 | ns   |         |
| t <sub>R</sub>    | Memory Cell Array to Starting Address  | —   | 25                | μs   |         |
| t <sub>WB</sub>   | $\overline{WE}$ High to Busy   | —   | 200               | ns   |         |
| t <sub>AR2</sub>  | ALE Low to $\overline{RE}$ Low (Read Cycle)                                      | 50  | —                 | ns   |         |
| t <sub>RB</sub>   | $\overline{RE}$ Last Clock Rising Edge to Busy (in Sequential Read)              | —   | 200               | ns   |         |
| t <sub>CRY</sub>  | $\overline{CE}$ High to Ready (When interrupted by $\overline{CE}$ in Read Mode) | —   | $1 + t_r (RY/BY)$ | μs   | (1) (2) |
| t <sub>RST</sub>  | Device Reset Time (Read/Program/Erase)   | —   | 6/10/500          | μs   |         |

## AC TEST CONDITIONS

| PARAMETER                      | CONDITION                       |
|--------------------------------|---------------------------------|
| Input level                    | 2.4 V, 0.4 V                    |
| Input pulse rise and fall time | 3 ns                            |
| Input comparison level         | 1.5 V, 1.5 V                    |
| Output data comparison level   | 1.5 V, 1.5 V                    |
| Output load                    | C <sub>L</sub> (100 pF) + 1 TTL |

- Note: (1)  $\overline{CE}$  High to Ready time depends on the pull-up resistor tied to the  $RY/\overline{BY}$  pin.  
 (Refer to Application Note (9) toward the end of this document.)
- (2) Sequential Read is terminated when  $t_{CEH}$  is greater than or equal to 100 ns. If the  $\overline{RE}$  to  $\overline{CE}$  delay is less than 30 ns,  $RY/\overline{BY}$  signal stays Ready.



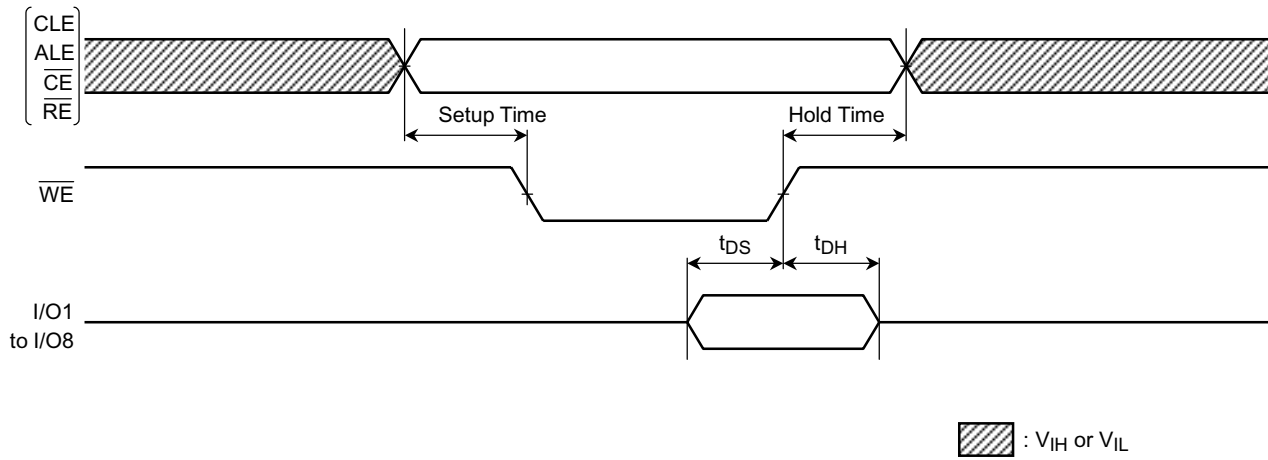
**PROGRAMMING AND ERASING CHARACTERISTICS ( $T_a = 0^\circ$  to  $70^\circ\text{C}$ ,  $V_{CC} = 2.7$  V to  $3.6$  V)**

| SYMBOL       | PARAMETER                                 | MIN | TYP.       | MAX  | UNIT          | NOTES |
|--------------|---|-----|------------|------|---------------|-------|
| $t_{PROG}$   | Programming Time                          | —   | 200 to 300 | 1000 | $\mu\text{s}$ |       |
| N            | Number of Programming Cycles on Same Page | —   | —          | 3    |               | (1)   |
| $t_{BERASE}$ | Block Erasing Time                        | —   | 2          | 10   | ms            |       |

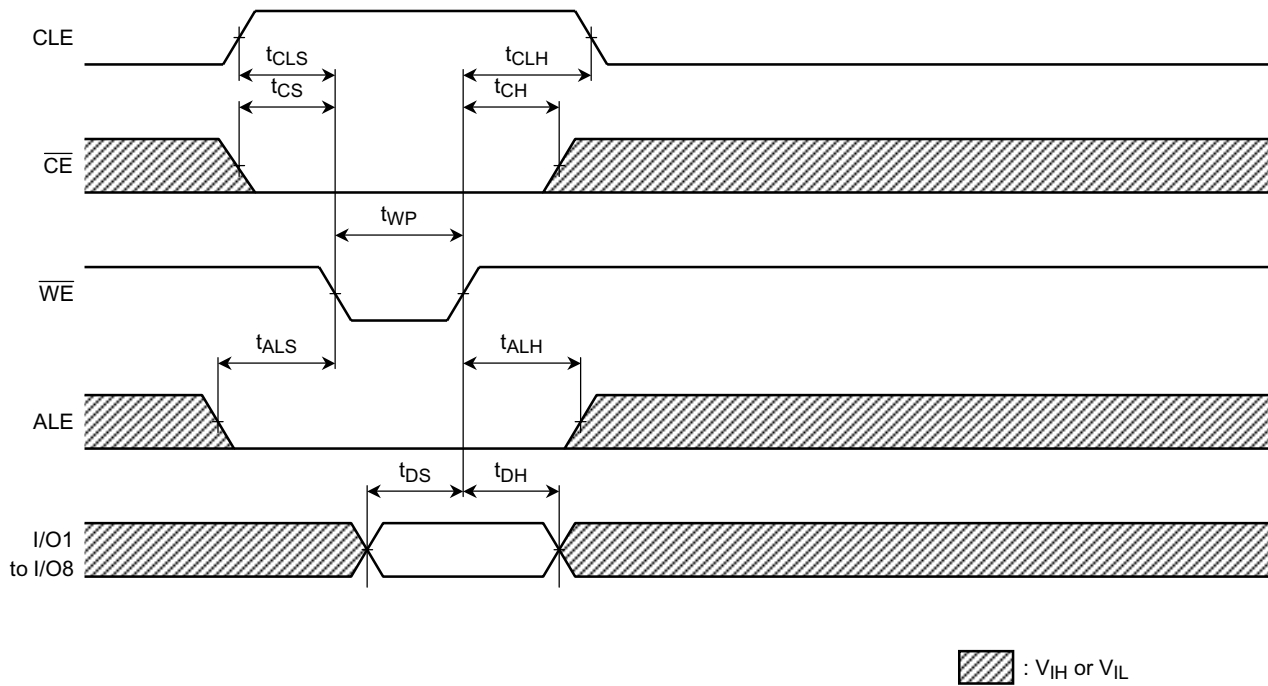
(1): Refer to Application Note (12) toward the end of this document.

**TIMING DIAGRAMS**

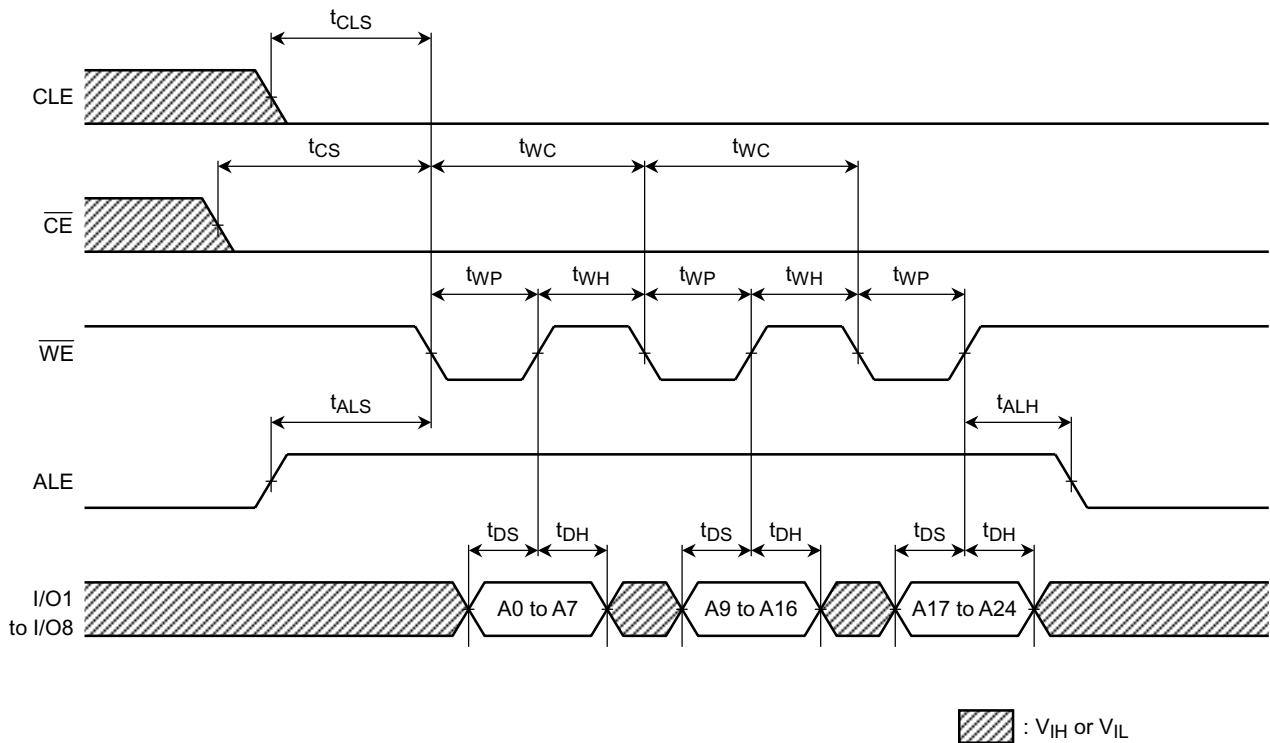
Latch Timing Diagram for Command/Address/Data



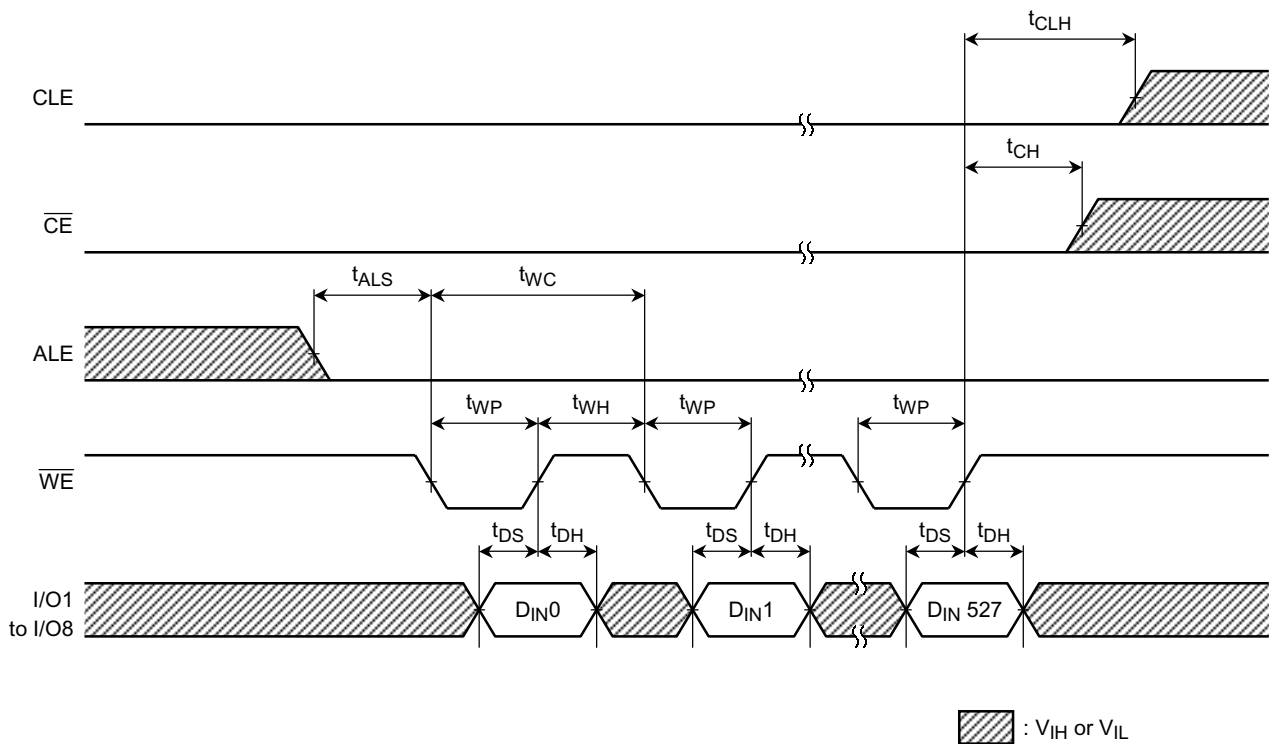
Command Input Cycle Timing Diagram



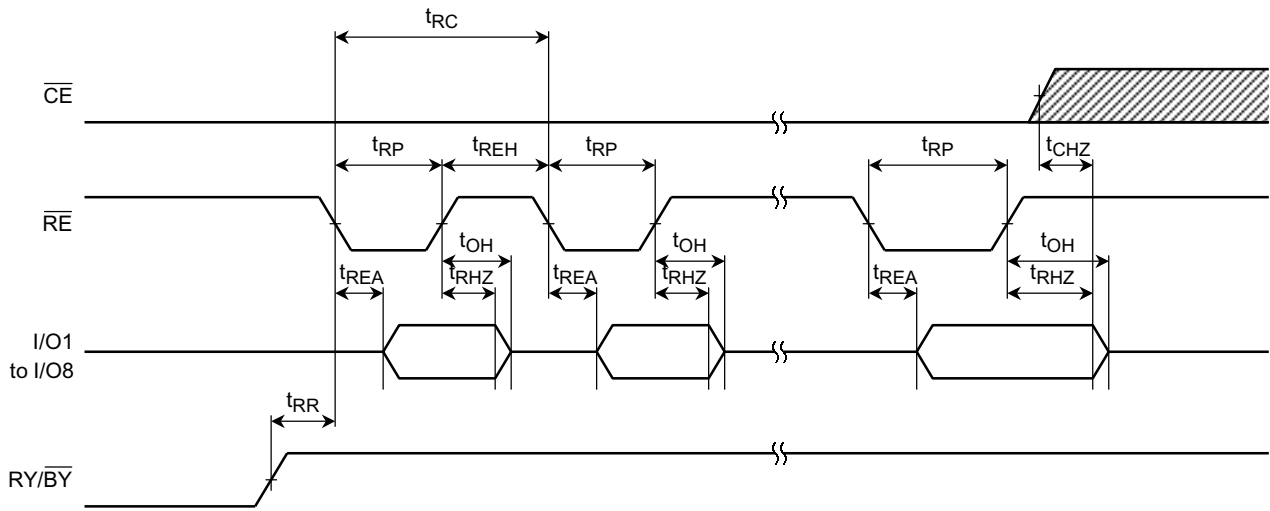
Address Input Cycle Timing Diagram



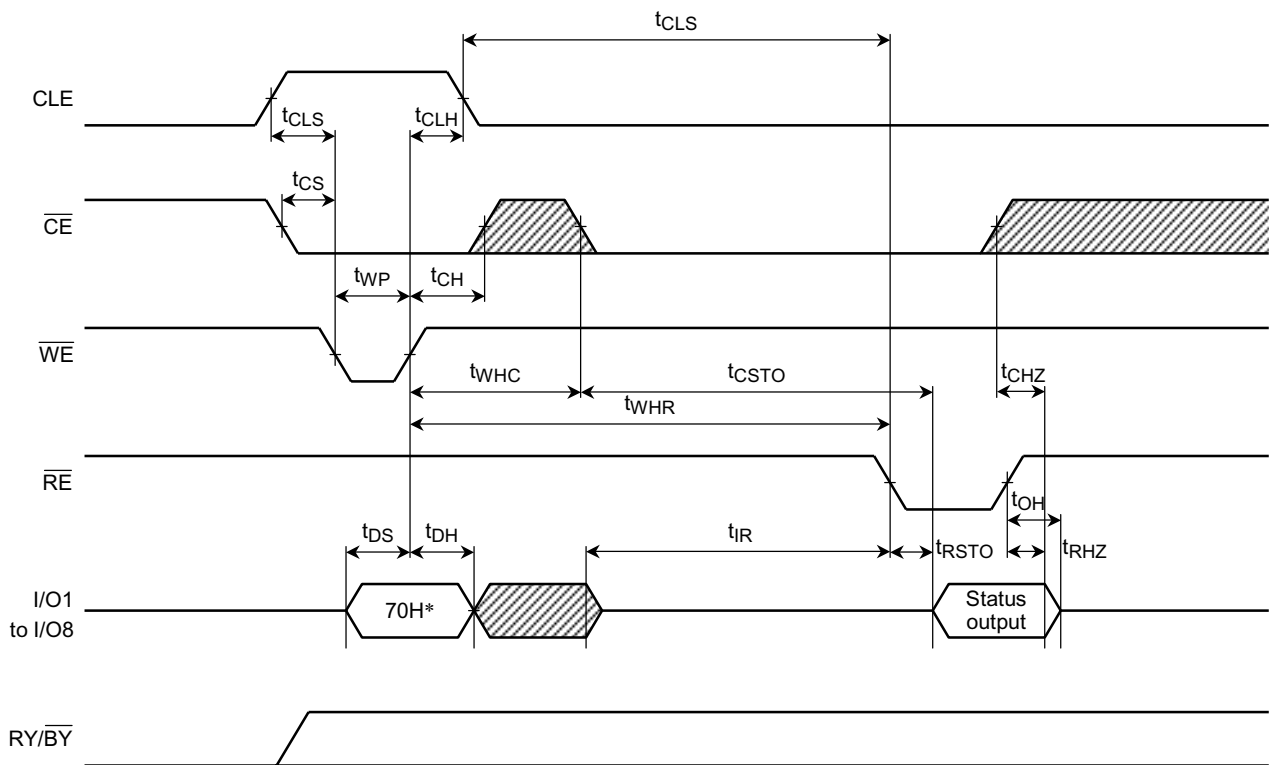
Data Input Cycle Timing Diagram




Serial Read Cycle Timing Diagram



Status Read Cycle Timing Diagram

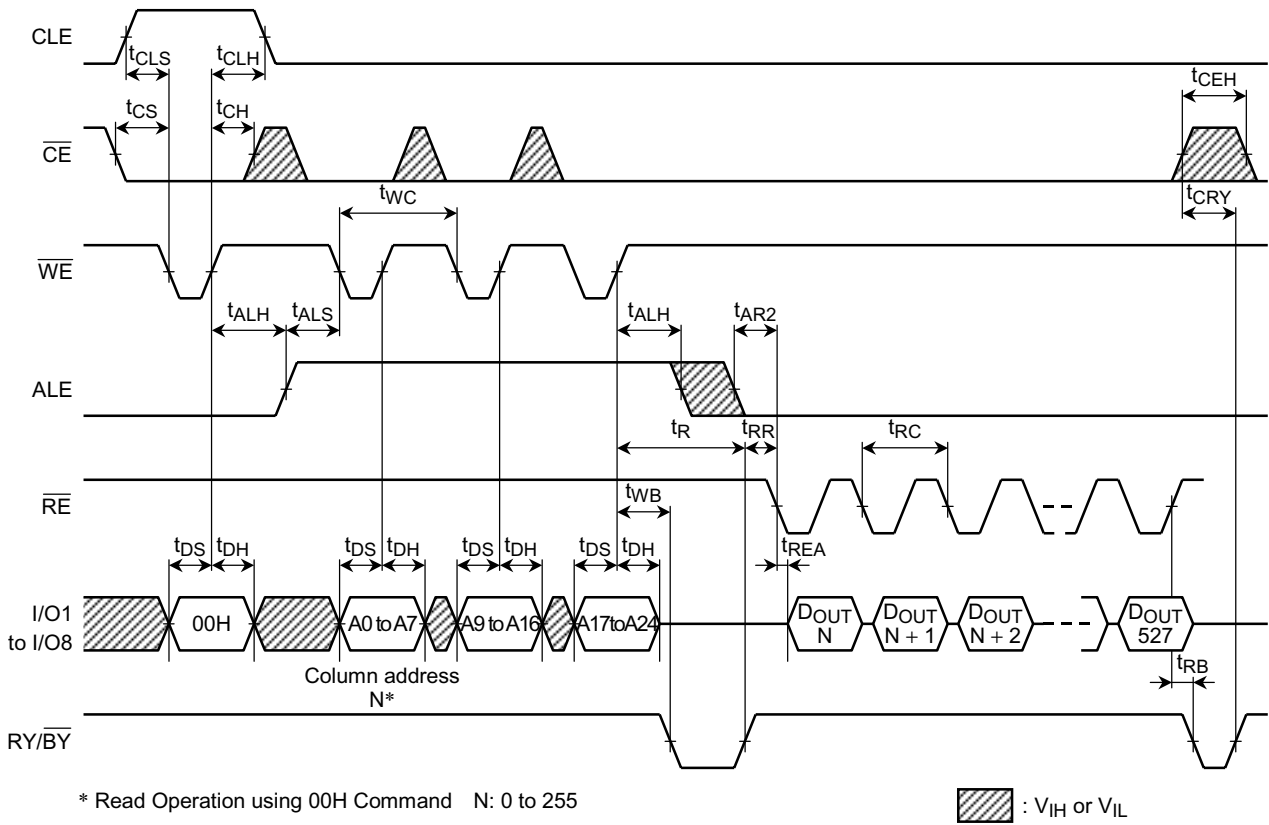


\* 70H represents the hexadecimal number

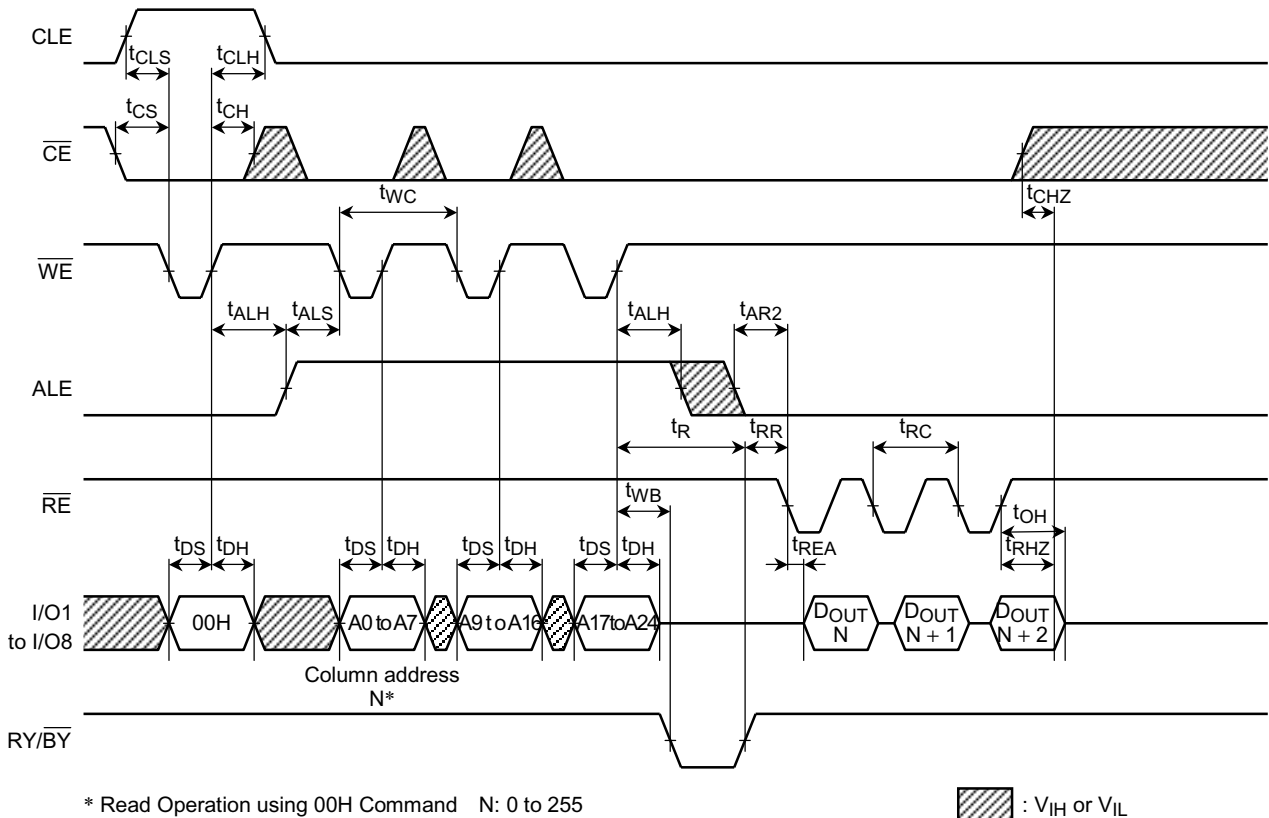
 :  $V_{IH}$  or  $V_{IL}$



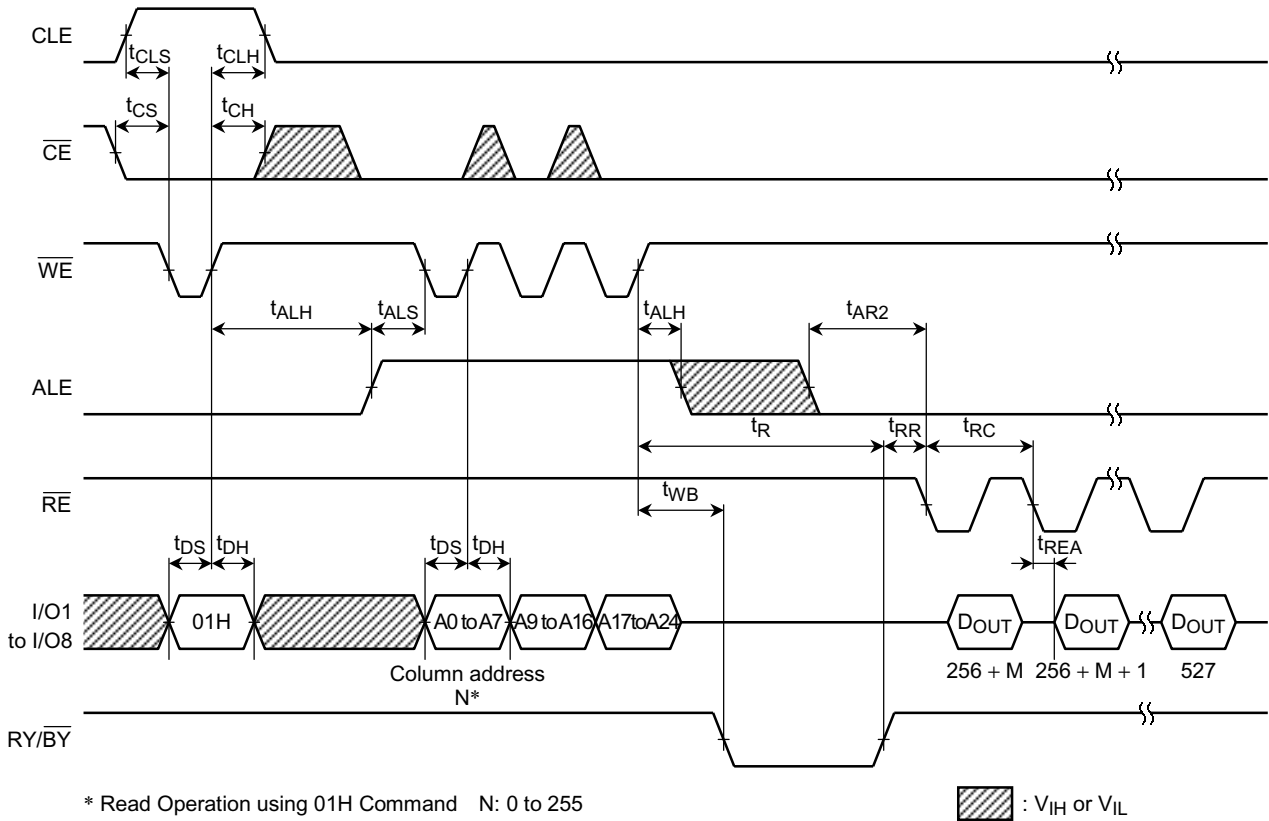
Read Cycle (1) Timing Diagram



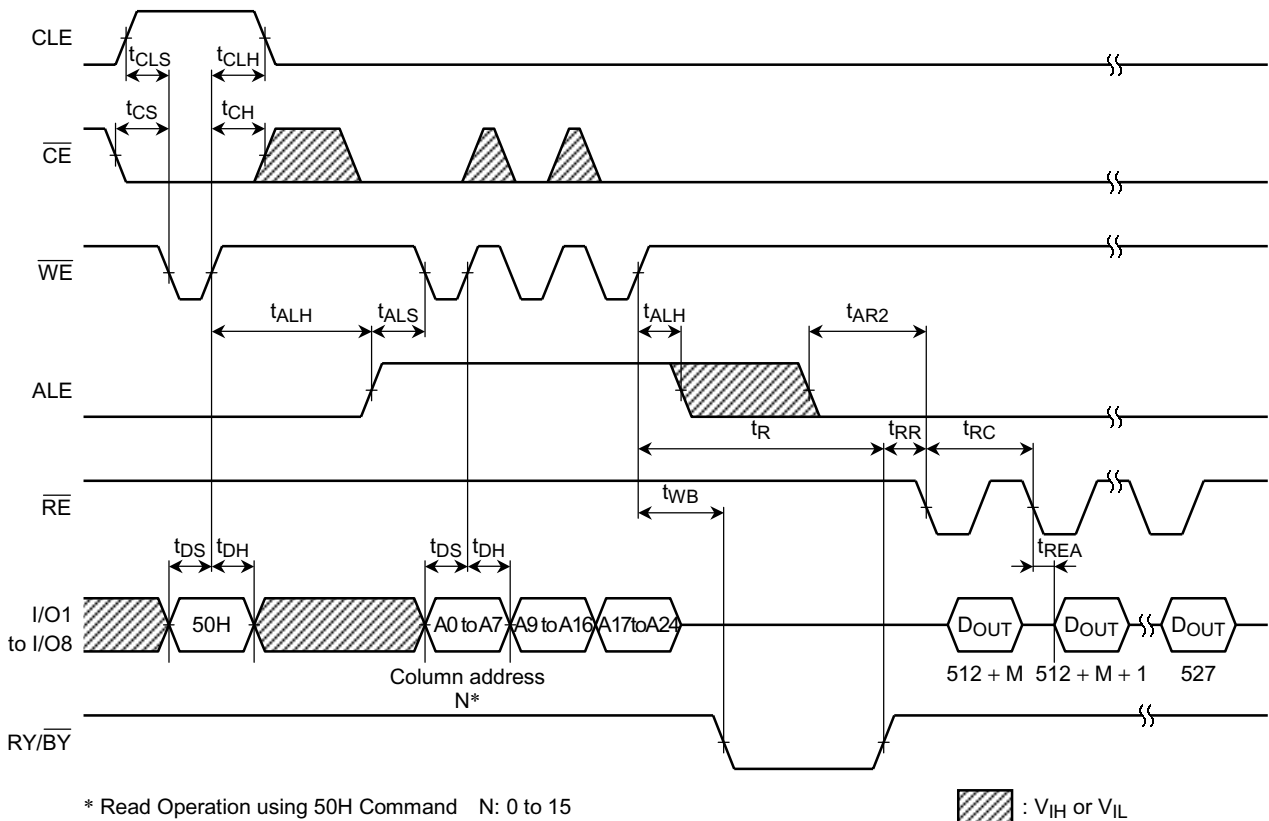
Read Cycle (1) Timing Diagram: When Interrupted by  $\overline{CE}$



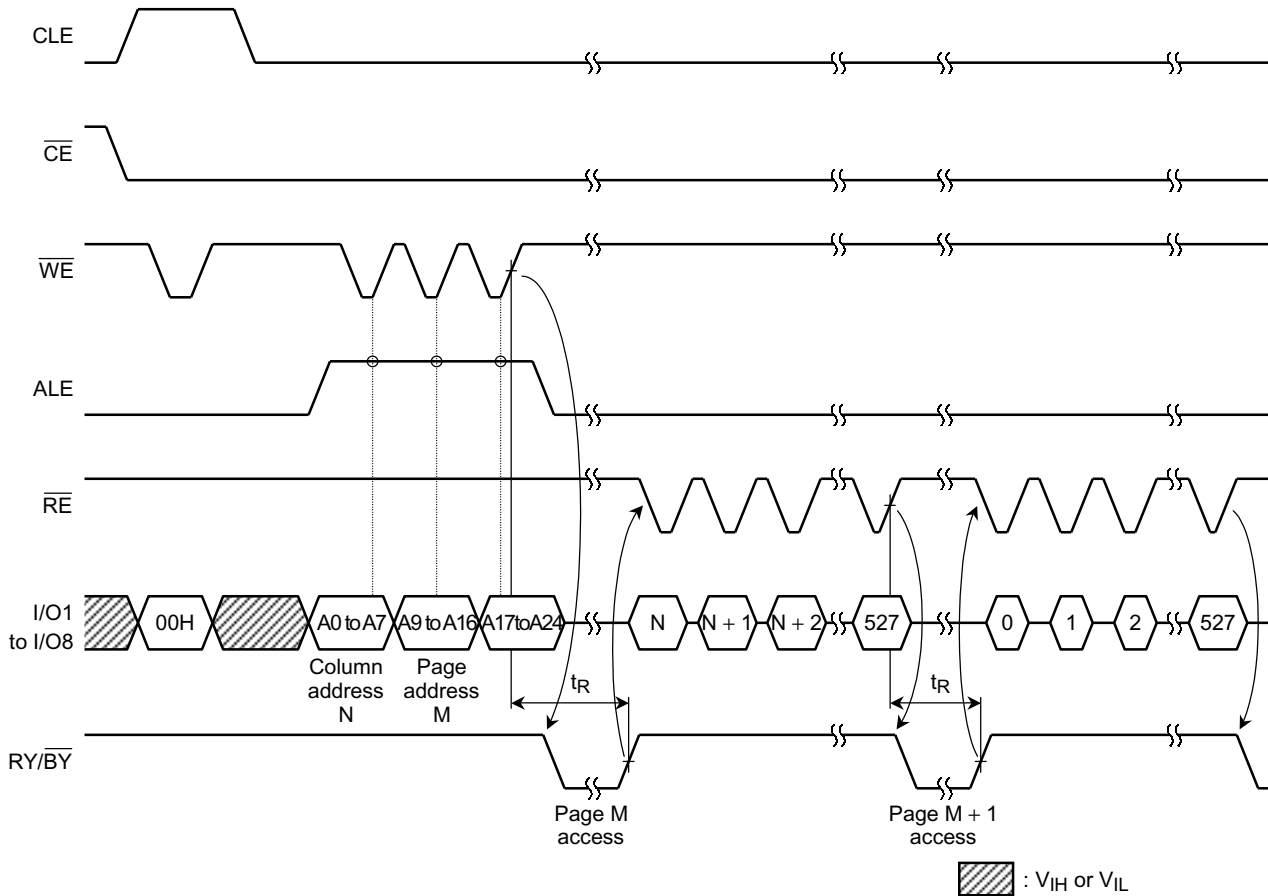
Read Cycle (2) Timing Diagram



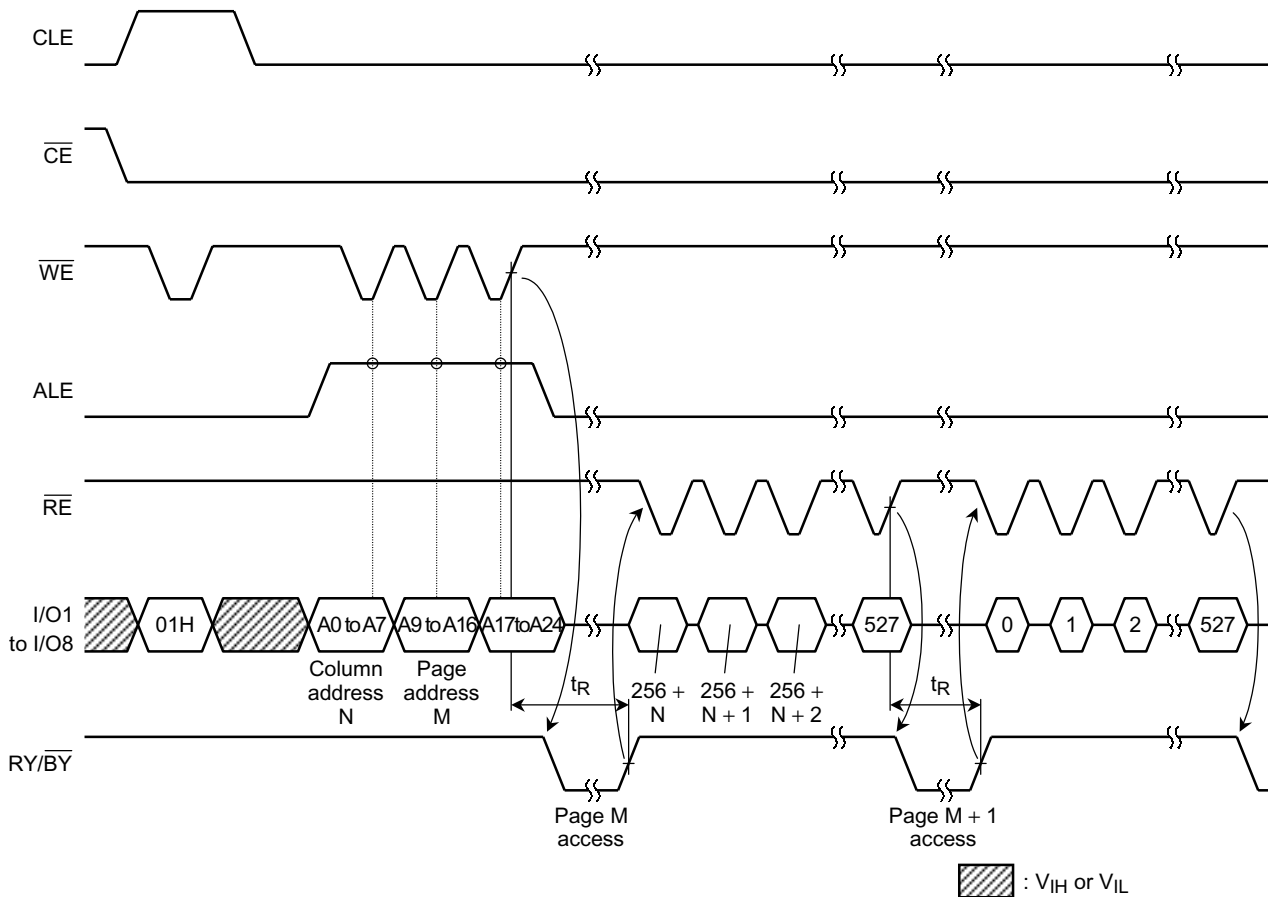
Read Cycle (3) Timing Diagram



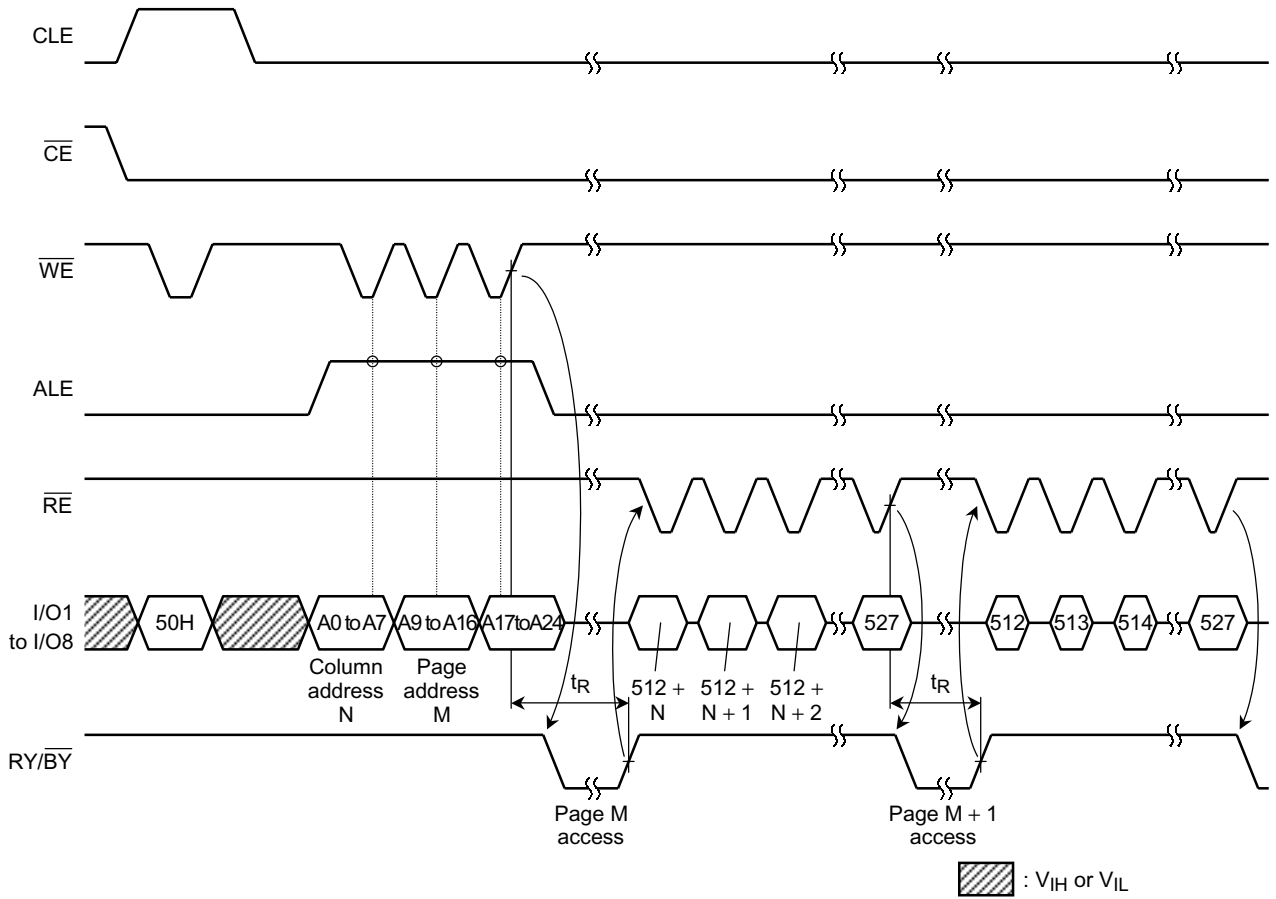
## Sequential Read (1) Timing Diagram



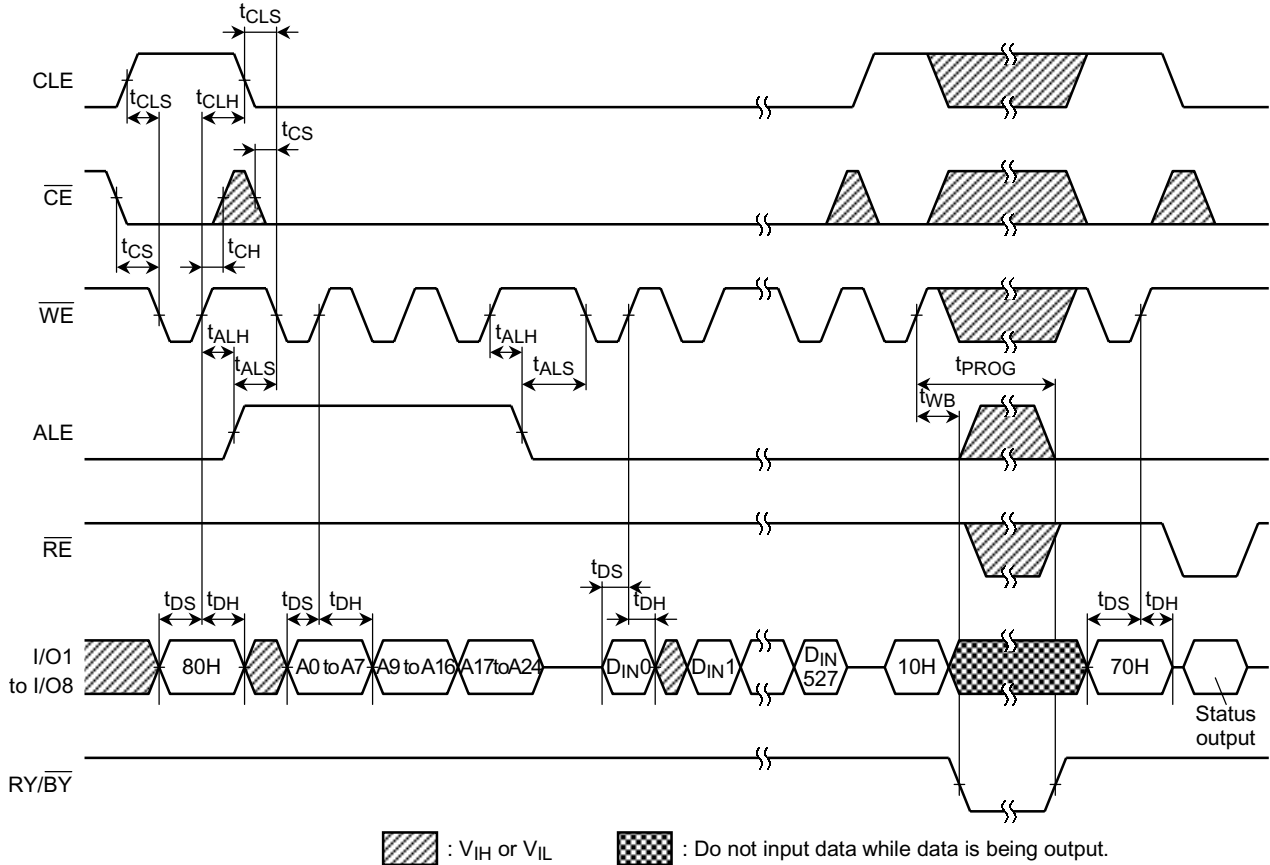
## Sequential Read (2) Timing Diagram



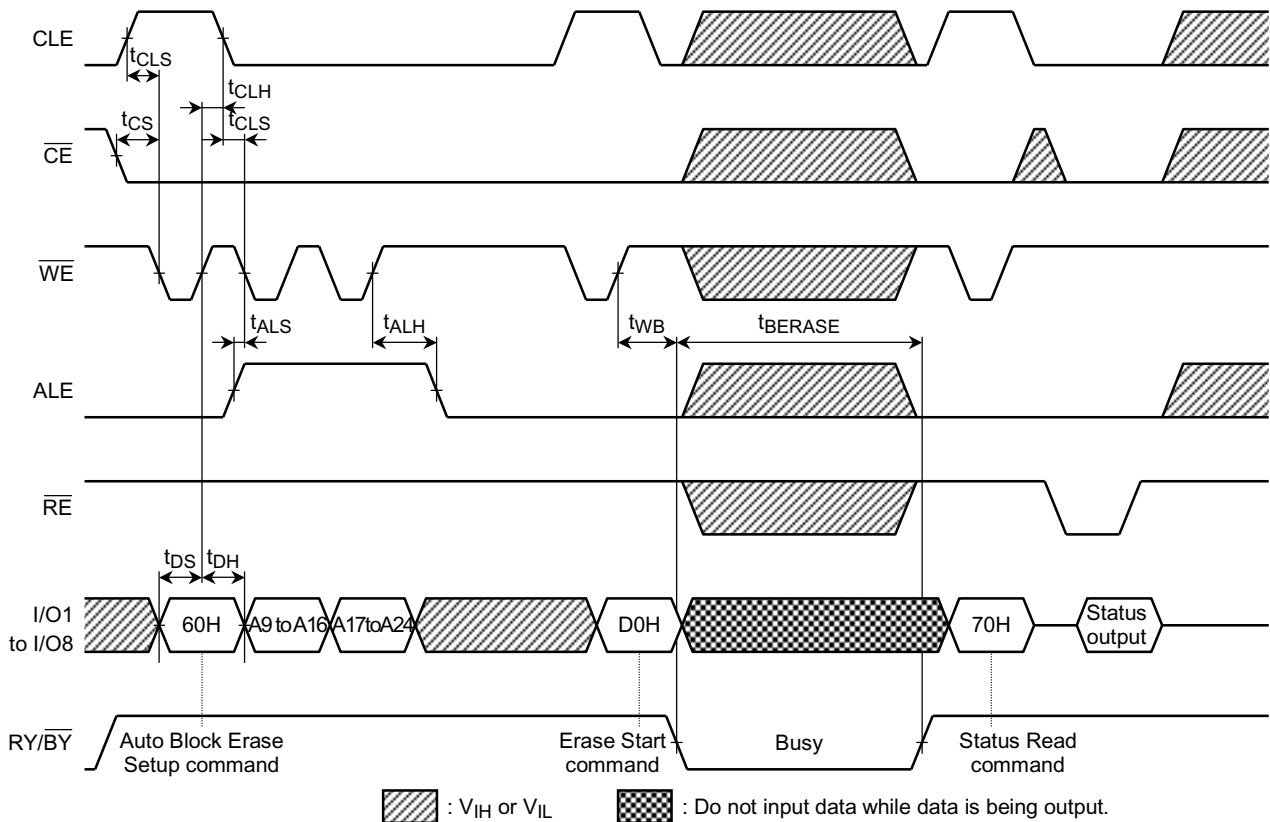
Sequential Read (3) Timing Diagram



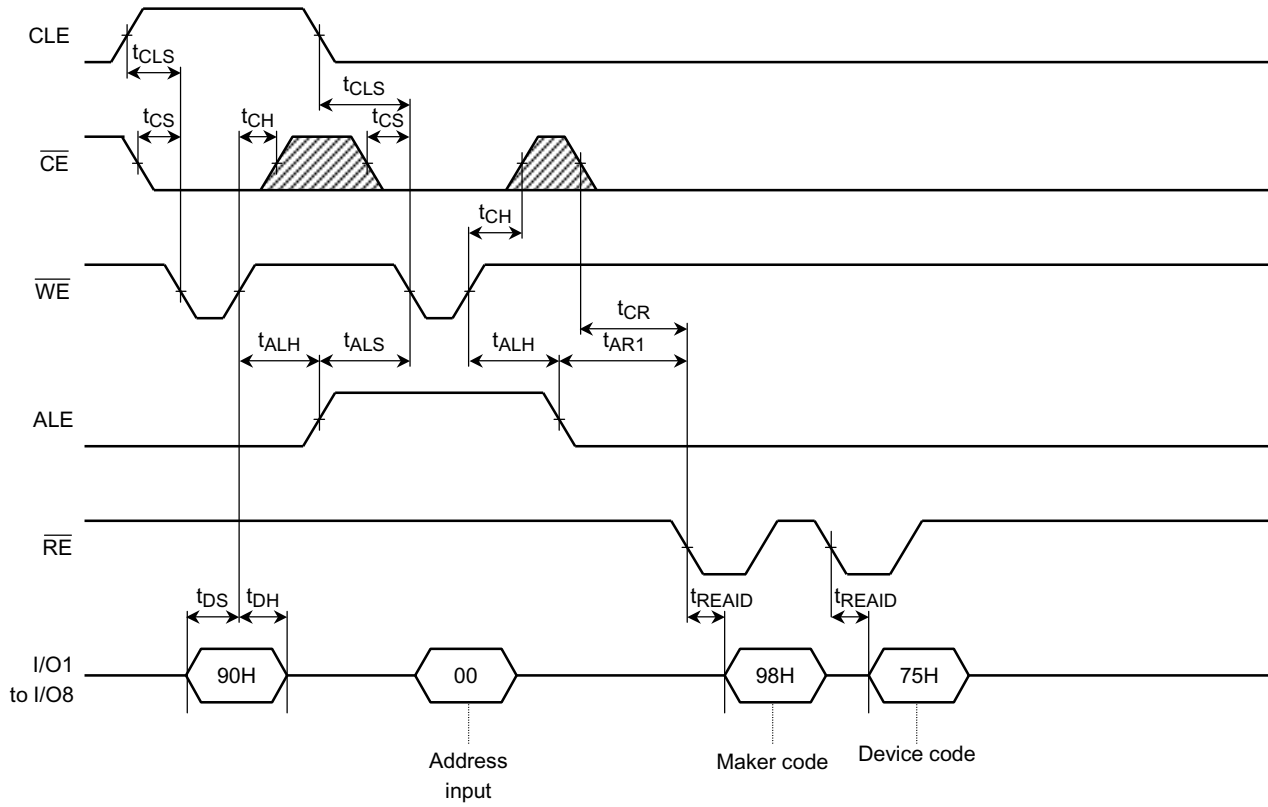
Auto-Program Operation Timing Diagram




Auto Block Erase Timing Diagram



ID Read Operation Timing Diagram



 :  $V_{IH}$  or  $V_{IL}$

## PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information. The device pin-outs are configured as shown in Figure 1.

### Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the  $\overline{WE}$  signal while CLE is High.

### Address Latch Enable: ALE

The ALE signal is used to control loading of either address information or input data into the internal address/data register.

Address information is latched on the rising edge of  $\overline{WE}$  if ALE is High.

Input data is latched if ALE is Low.

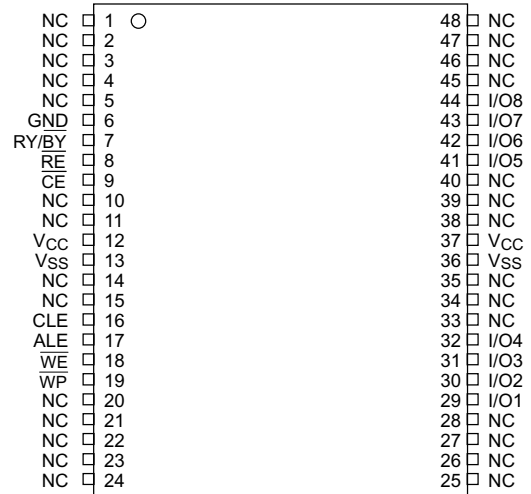


Figure 1. Pinout

### Chip Enable: $\overline{CE}$

The device goes into a low-power Standby mode when  $\overline{CE}$  goes High during a Read operation. The  $\overline{CE}$  signal is ignored when device is in Busy state ( $\overline{RY}/\overline{BY} = L$ ), such as during a Program or Erase operation, and will not enter Standby mode even if the  $\overline{CE}$  input goes High. The  $\overline{CE}$  signal must stay Low during the Read mode Busy state to ensure that memory array data is correctly transferred to the data register.

### Write Enable: $\overline{WE}$

The  $\overline{WE}$  signal is used to control the acquisition of data from the I/O port.

### Read Enable: $\overline{RE}$

The  $\overline{RE}$  signal controls serial data output. Data is available  $t_{REA}$  after the falling edge of  $\overline{RE}$ .

The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

### I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

### Write Protect: $\overline{WP}$

The  $\overline{WP}$  signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when  $\overline{WP}$  is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

### Ready/Busy: RY/ $\overline{BY}$

The RY/ $\overline{BY}$  output signal is used to indicate the operating condition of the device. The RY/ $\overline{BY}$  signal is in Busy state ( $\overline{RY}/\overline{BY} = L$ ) during the Program, Erase and Read operations and will return to Ready state ( $\overline{RY}/\overline{BY} = H$ ) after completion of the operation. The output buffer for this signal is an open drain.

## Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.

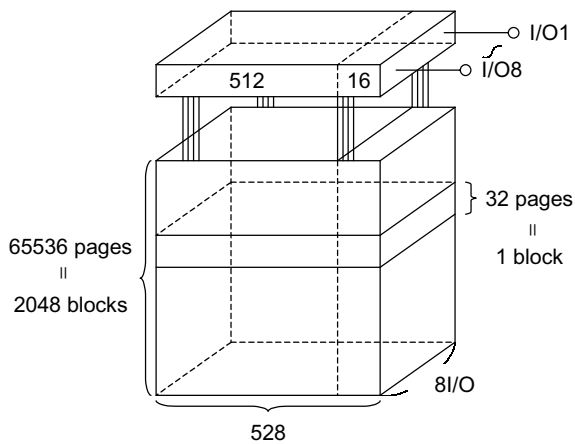


Figure 2. Schematic Cell Layout

A page consists of 528 bytes in which 512 bytes are used for main memory storage and 16 bytes are for redundancy or for other uses.

1 page = 528 bytes

1 block = 528 bytes × 32 pages = (16K + 512) bytes

Capacity = 528 bytes × 32 pages × 2048 blocks

An address is read in via the I/O port over three consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

|              | I/O8 | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 |
|--------------|------|------|------|------|------|------|------|------|
| First cycle  | A7   | A6   | A5   | A4   | A3   | A2   | A1   | A0   |
| Second cycle | A16  | A15  | A14  | A13  | A12  | A11  | A10  | A9   |
| Third cycle  | A24  | A23  | A22  | A21  | A20  | A19  | A18  | A17  |

A0~A7: Column address

A9~A24: Page address

(A14~A24: Block address

A9~A13: NAND address in block)

\*: A8 is automatically set to Low or High by a 00H command or a 01H command.

## Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by the ten different command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE,  $\overline{CE}$ ,  $\overline{WE}$ ,  $\overline{RE}$  and  $\overline{WP}$  signals, as shown in Table 2.

Table 2. Logic table

|                           | CLE | ALE | $\overline{CE}$ | $\overline{WE}$ | $\overline{RE}$ | $\overline{WP}$ |
|---------------------------|-----|-----|-----------------|-----------------|-----------------|-----------------|
| Command Input             | H   | L   | L               |                 | H               | *               |
| Data Input                | L   | L   | L               |                 | H               | *               |
| Address Input             | L   | H   | L               |                 | H               | *               |
| Serial Data Output        | L   | L   | L               | H               |                 | *               |
| During Programming (Busy) | *   | *   | *               | *               | *               | H               |
| During Erasing (Busy)     | *   | *   | *               | *               | *               | H               |
| Program, Erase Inhibit    | *   | *   | *               | *               | *               | L               |

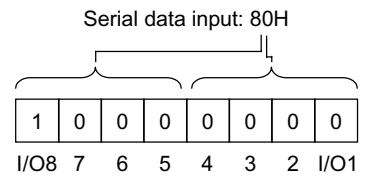
H:  $V_{IH}$ , L:  $V_{IL}$ , \*:  $V_{IH}$  or  $V_{IL}$



Table 3. Command table (HEX)

|                   | First Cycle | Second Cycle | Acceptable while Busy |
|-------------------|-------------|--------------|-----------------------|
| Serial Data Input | 80          | —            |                       |
| Read Mode (1)     | 00          | —            |                       |
| Read Mode (2)     | 01          | —            |                       |
| Read Mode (3)     | 50          | —            |                       |
| Reset             | FF          | —            | ○                     |
| Auto Program      | 10          | —            |                       |
| Auto Block Erase  | 60          | D0           |                       |
| Status Read       | 70          | —            | ○                     |
| ID Read           | 90          | —            |                       |

HEX data bit assignment  
(Example)



Once the device has been set to Read mode by a 00H, 01H or 50H command, additional Read commands are not needed for sequential page Read operations. Table 4 shows the operation states for Read mode.

Table 4. Read mode operation states

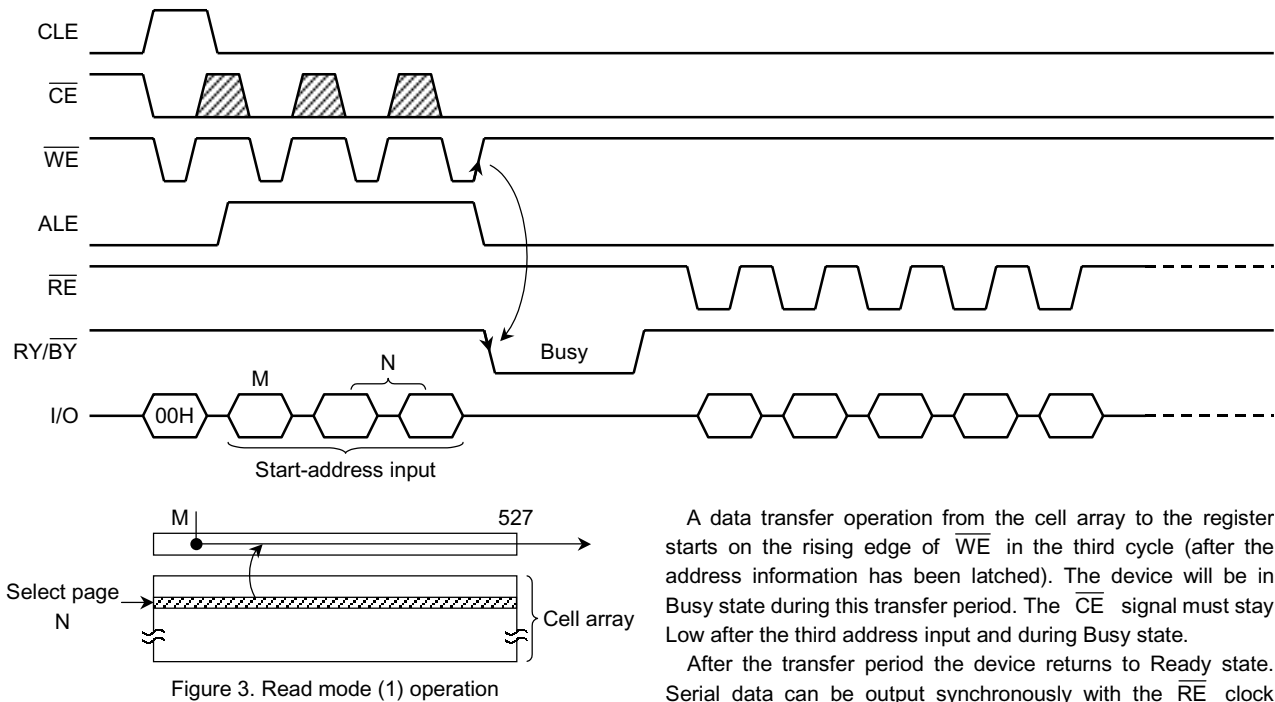
|                 | CLE | ALE | $\overline{CE}$ | $\overline{WE}$ | $\overline{RE}$ | I/O1~I/O8      | Power   |
|-----------------|-----|-----|-----------------|-----------------|-----------------|----------------|---------|
| Output Select   | L   | L   | L               | H               | L               | Data output    | Active  |
| Output Deselect | L   | L   | L               | H               | H               | High impedance | Active  |
| Standby         | L   | L   | H               | H               | *               | High impedance | Standby |

H:  $V_{IH}$ , L:  $V_{IL}$ , \*:  $V_{IH}$  or  $V_{IL}$

**DEVICE OPERATION**

Read Mode (1)

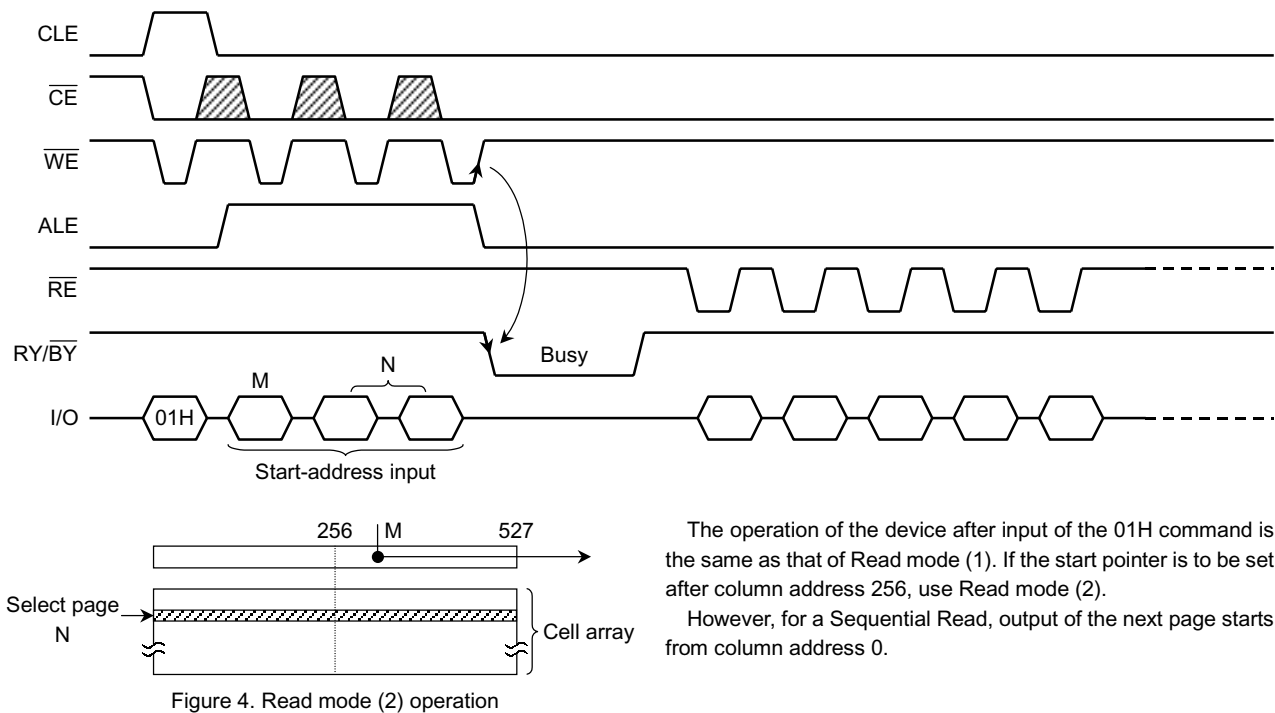
Read mode (1) is set when a 00H command is issued to the Command register. Refer to Figure 3 below for timing details and the block diagram.



A data transfer operation from the cell array to the register starts on the rising edge of  $\overline{WE}$  in the third cycle (after the address information has been latched). The device will be in Busy state during this transfer period. The  $\overline{CE}$  signal must stay Low after the third address input and during Busy state.

After the transfer period the device returns to Ready state. Serial data can be output synchronously with the  $\overline{RE}$  clock from the start pointer designated in the address input cycle.

Read Mode (2)



The operation of the device after input of the 01H command is the same as that of Read mode (1). If the start pointer is to be set after column address 256, use Read mode (2).

However, for a Sequential Read, output of the next page starts from column address 0.

Read Mode (3)

Read mode (3) has the same timing as Read modes (1) and (2) but is used to access information in the extra 16-byte redundancy area of the page. The start pointer is therefore set to a value between byte 512 and byte 527.

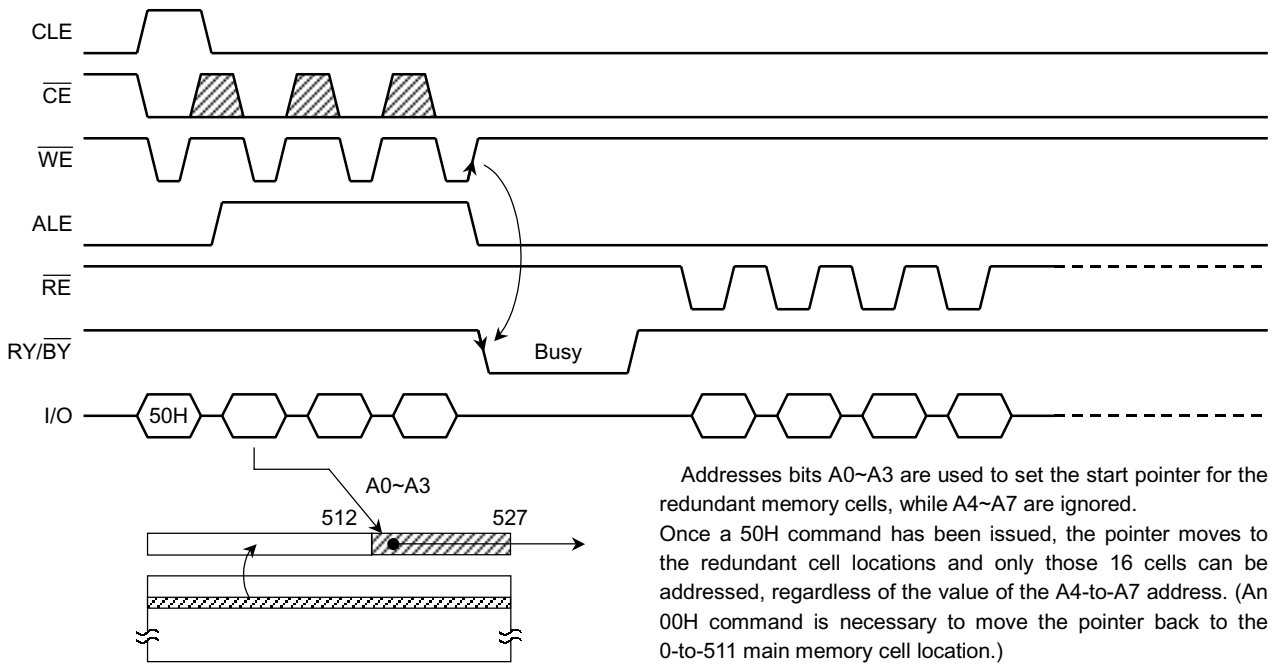
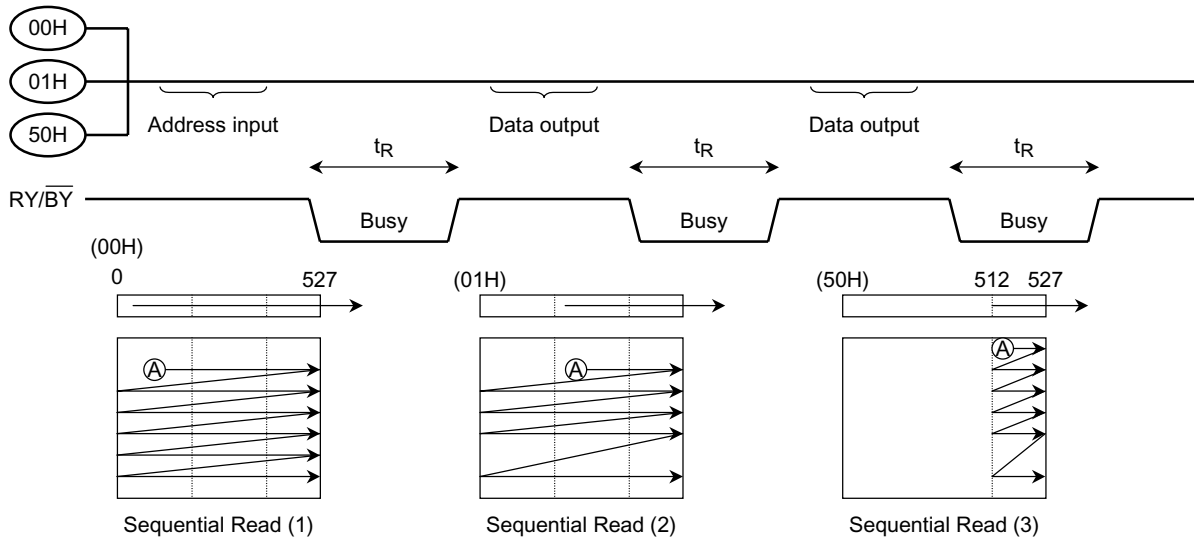


Figure 5. Read mode (3) operation

Sequential Read (1) (2) (3)

This mode allows the sequential reading of pages without additional address input.



Sequential Read modes (1) and (2) output the contents of addresses 0~527 as shown above, while Sequential Read mode (3) outputs the contents of the redundant address locations only. When the pointer reaches the last address, the device continues to output the data from this address \*\* on each  $\overline{RE}$  clock signal.

\*\* Column address 527 on the last page.

**Status Read**

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port on the  $\overline{RE}$  clock after a 70H command input. The resulting information is outlined in Table 5.

Table 5. Status output table

|      | STATUS        | OUTPUT     |                  |
|------|---------------|------------|------------------|
| I/O1 | Pass/Fail     | Pass: 0    | Fail: 1          |
| I/O2 | Not Used      | 0          |                  |
| I/O3 | Not Used      | 0          |                  |
| I/O4 | Not Used      | 0          |                  |
| I/O5 | Not Used      | 0          |                  |
| I/O6 | Not Used      | 0          |                  |
| I/O7 | Ready/Busy    | Ready: 1   | Busy: 0          |
| I/O8 | Write Protect | Protect: 0 | Not Protected: 1 |

The Pass/Fail status on I/O1 is only valid when the device is in the Ready state.

An application example with multiple devices is shown in Figure 6.

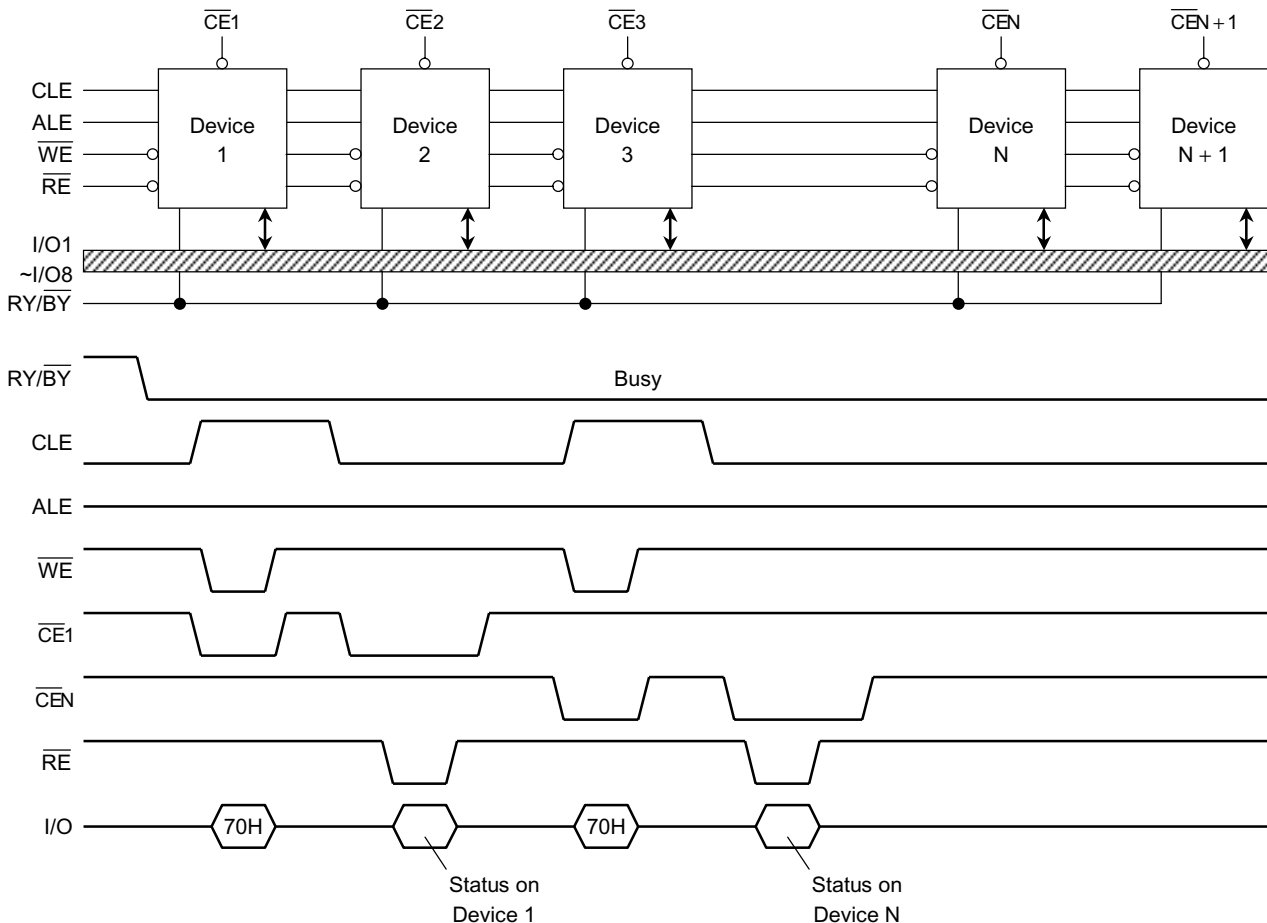


Figure 6. Status Read timing application example

System Design Note: If the  $\overline{RY/BY}$  pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

Auto Page Program

The device carries out an Automatic Page Program operation when it receives a “10H” Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)

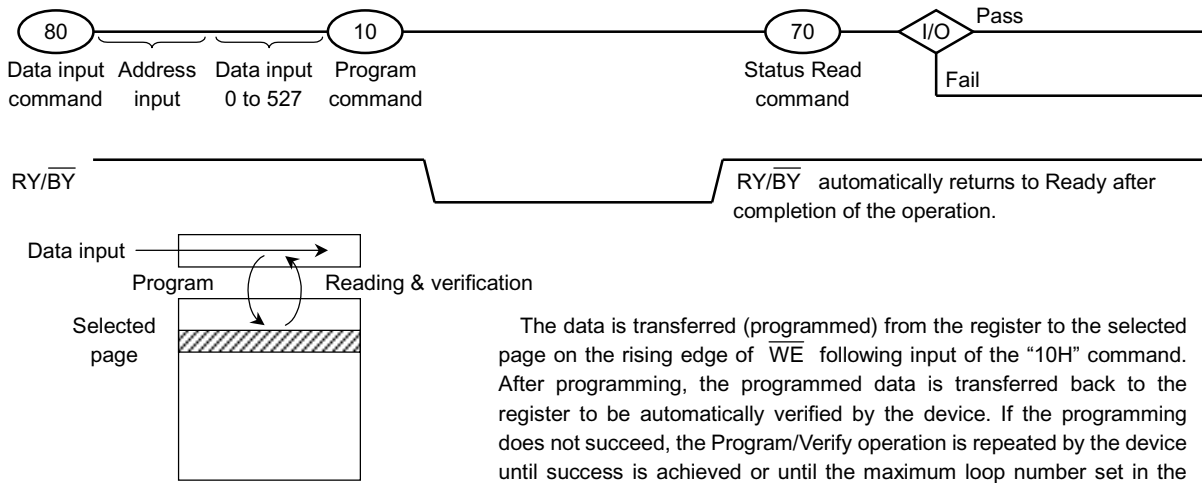
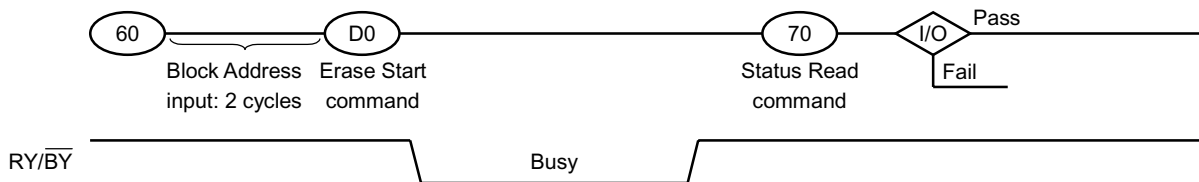


Figure 7. Auto Page Program operation

Auto Block Erase

The Auto Block Erase operation starts on the rising edge of  $\overline{WE}$  after the Erase Start command “D0H” which follows the Erase Setup command “60H”. This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.

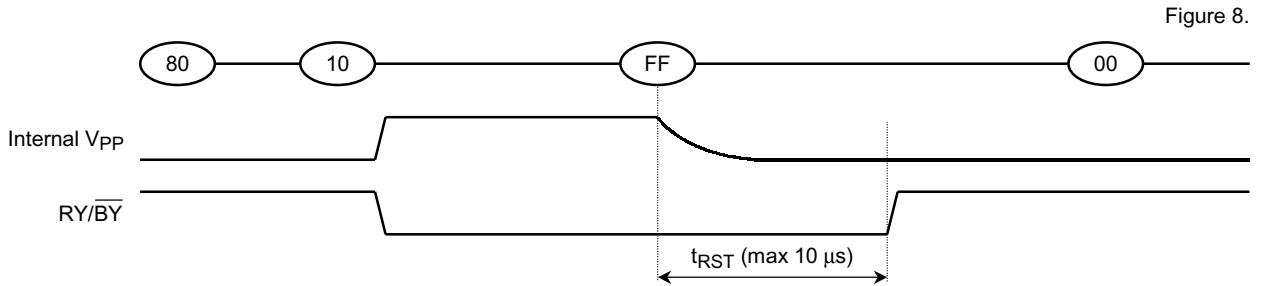


**Reset**

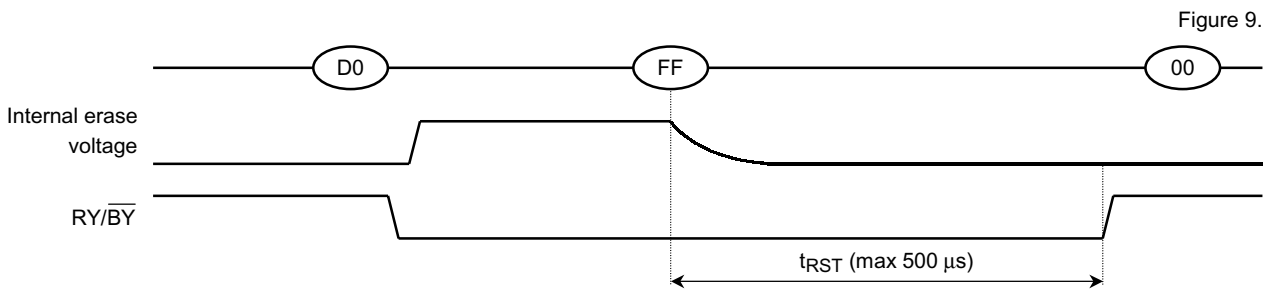
The Reset mode stops all operations. For example, in the case of a Program or Erase operation the internally generated voltage is discharged to 0 volts and the device enters Wait state.

The response to an “FFH” Reset command input during the various device operations is as follows:

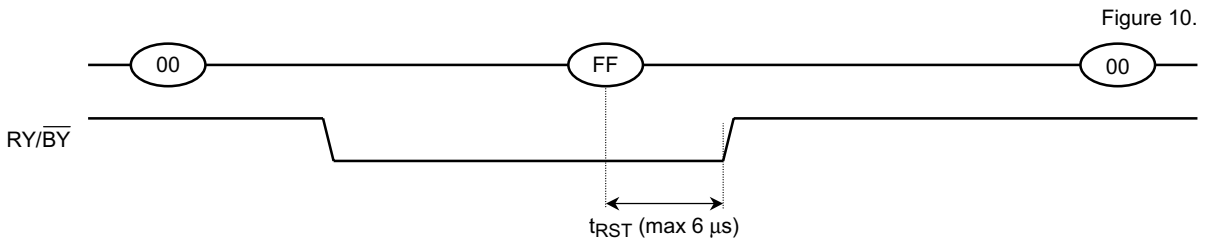
When a Reset (FFH) command is input during programming



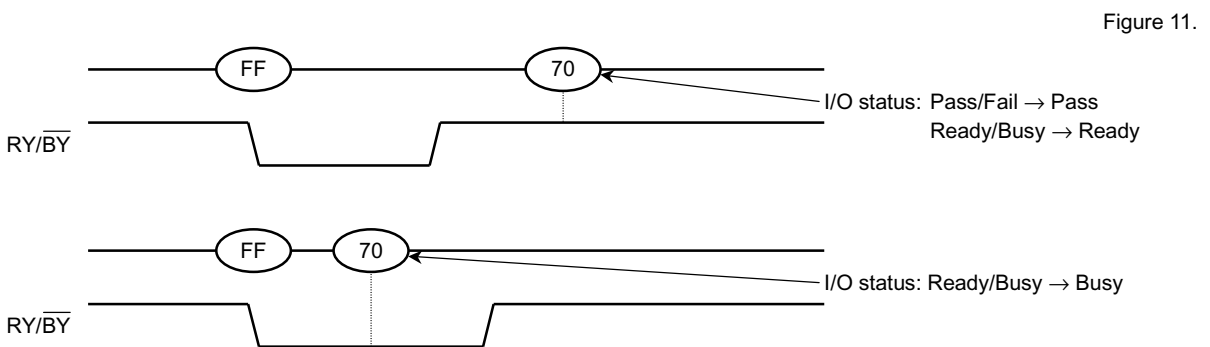
When a Reset (FFH) command is input during erasing



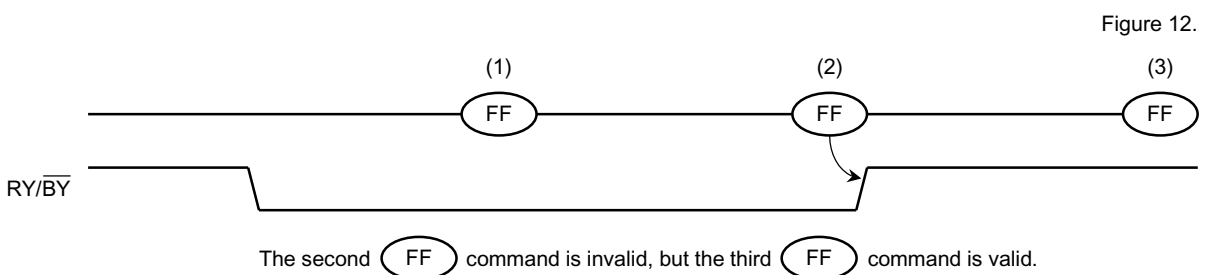
When a Reset (FFH) command is input during Read operation



When a Status Read command (70H) is input after a Reset

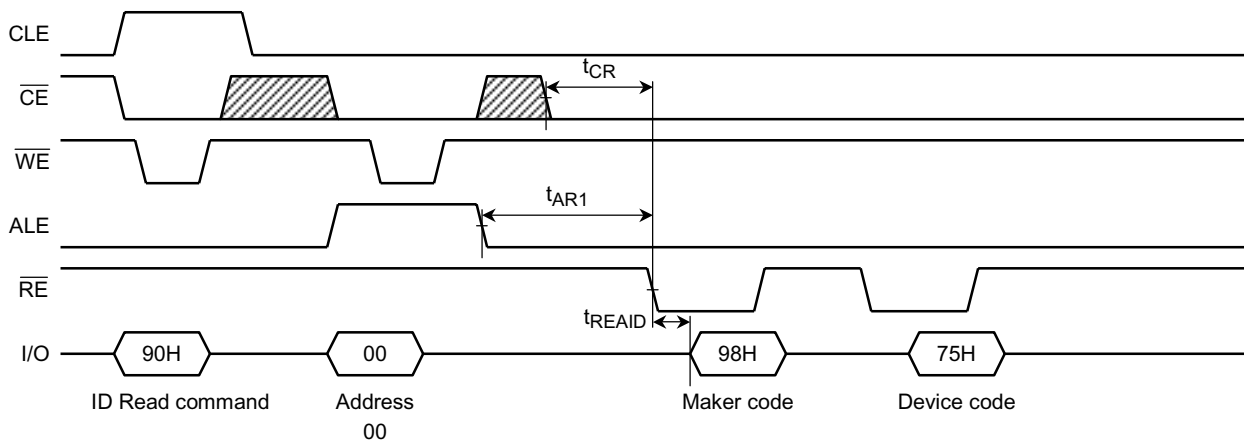


When two or more Reset commands are input in succession



ID Read

The TC58256A contains ID codes which identify the device type and the manufacturer.  
The ID codes can be read out under the following timing conditions:



For the specifications of the access times  $t_{READ}$ ,  $t_{CR}$  and  $t_{AR1}$  refer to the AC Characteristics.

Figure 13. ID Read timing

Table 6. ID Codes read out by ID read command 90H

|             | I/O8 | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | Hex Data |
|-------------|------|------|------|------|------|------|------|------|----------|
| Maker code  | 1    | 0    | 0    | 1    | 1    | 0    | 0    | 0    | 98H      |
| Device code | 0    | 1    | 1    | 1    | 0    | 1    | 0    | 1    | 75H      |

**APPLICATION NOTES AND COMMENTS**

(1) Power-on/off sequence:

The  $\overline{WP}$  signal is useful for protecting against data corruption at power-on/off. The following timing sequence is necessary.

The  $\overline{WP}$  signal may be negated any time after the  $V_{CC}$  reaches 2.5 V and  $\overline{CE}$  signal is kept high in power up sequence.

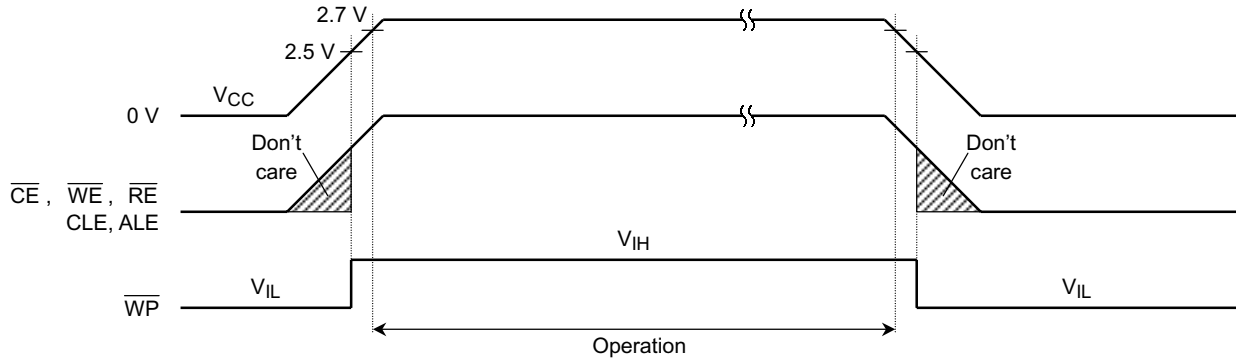


Figure 15. Power-on/off Sequence

In order to operate this device stably, after  $V_{CC}$  becomes 2.5 V, it recommends starting access after about 200  $\mu$ s.

(2) Status after power-on

The following sequence is necessary because some input signals may not be stable at power-on.

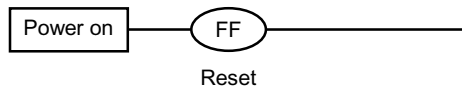


Figure 16.

(3) Prohibition of unspecified commands

The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

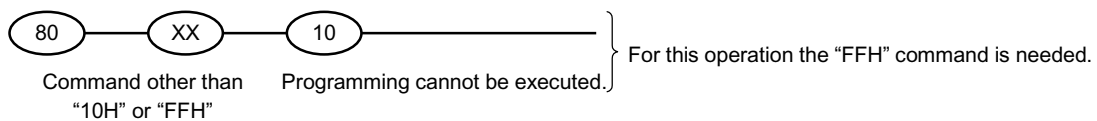
(4) Restriction of command while Busy state

During Busy state, do not input any command except 70H and FFH.

(5) Acceptable commands after Serial Input command "80H"

Once the Serial Input command "80H" has been input, do not input any command other than the Program Execution command "10H" or the Reset command "FFH".

If a command other than "10H" or "FFH" is input, the Program operation is not performed.





(6) Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.

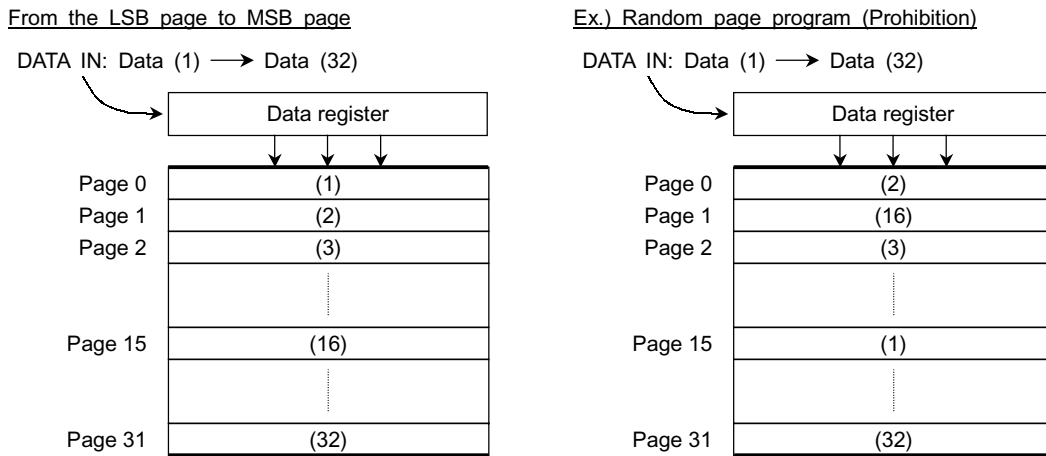


Figure 17. page programming within a block

(7) Status Read during a Read operation

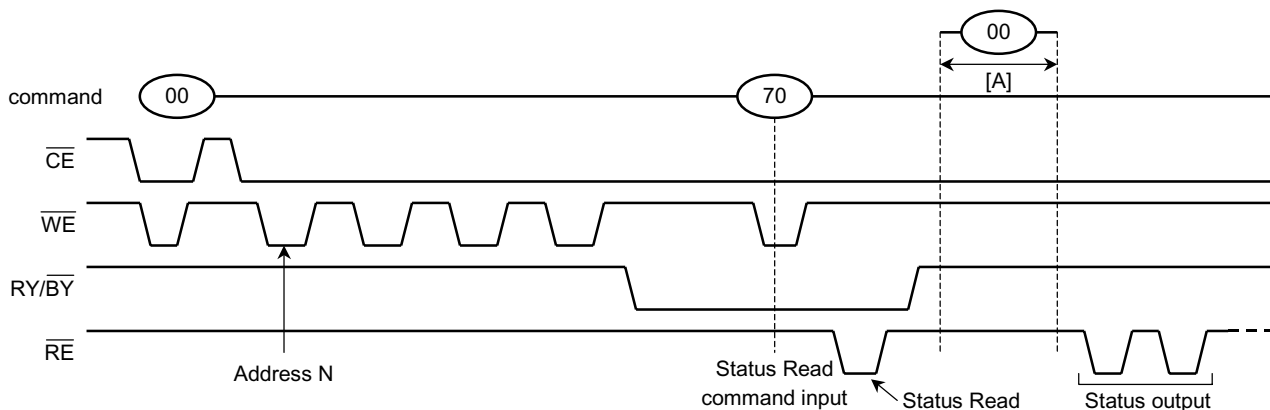


Figure 18.

The device status can be read out by inputting the Status Read command “70H” in Read mode.

Once the device has been set to Status Read mode by a “70H” command, the device will not return to Read mode.

Therefore, a Status Read during a Read operation is prohibited.

However, when the Read command “00H” is input during [A], Status mode is reset and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary

(8) Pointer control for “00H”, “01H” and “50H”

The device has three Read modes which set the destination of the pointer. Table 7 shows the destination of the pointer, and Figure 14 is a block diagram of their operations.

Table 8. Pointer Destination

| Read Mode | Command | Pointer    |
|-----------|---------|------------|
| (1)       | 00H     | 0 to 255   |
| (2)       | 01H     | 256 to 511 |
| (3)       | 50H     | 512 to 527 |

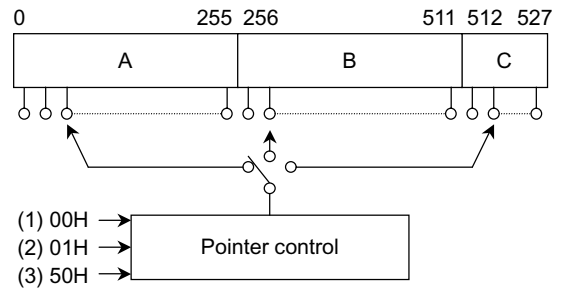
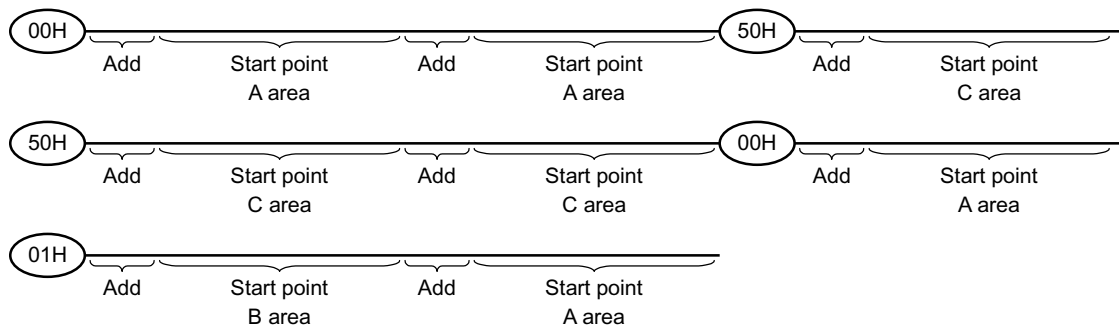


Figure 19. Pointer control

The pointer is set to region A by the “00H” command, to region B by the “01H” command, and to region C by the “50H” command.

(Example)

The “00H” command must be input to set the pointer back to region A when the pointer is pointing to region C.



To program region C only, set the start point to region C using the 50H command.

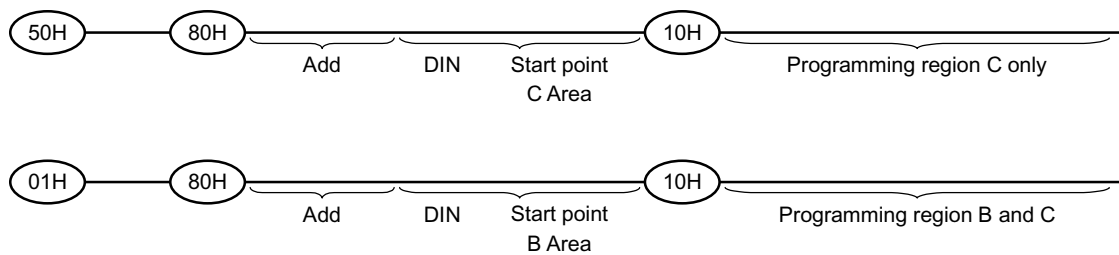
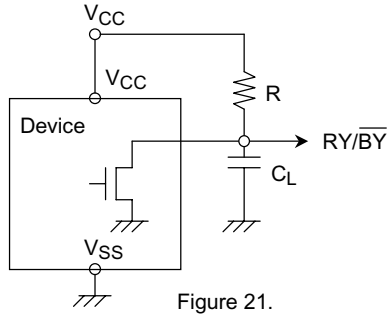


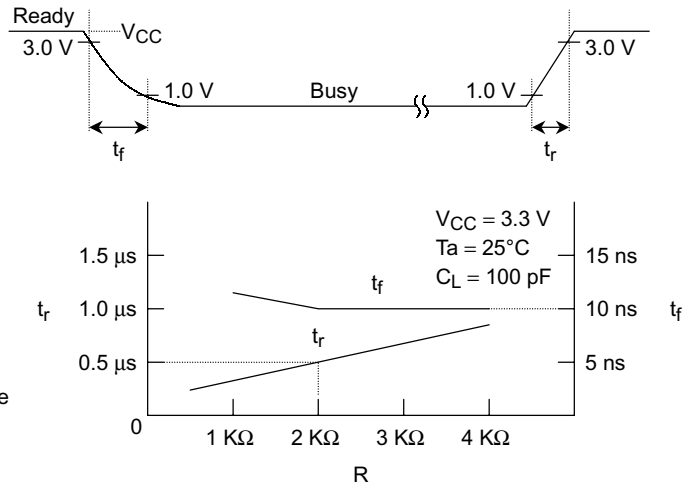
Figure 20. Example of How to Set the Pointer

(9)  $\overline{RY/BY}$  : termination for the Ready/Busy pin ( $\overline{RY/BY}$ )

A pull-up resistor needs to be used for termination because the  $\overline{RY/BY}$  buffer consists of an open drain circuit.



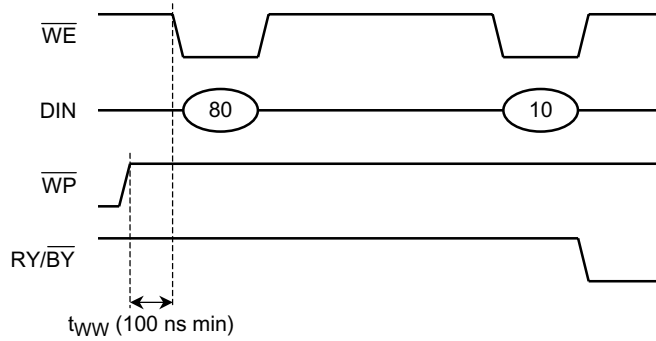
This data may vary from device to device.  
We recommend that you use this data as a reference when selecting a resistor value.



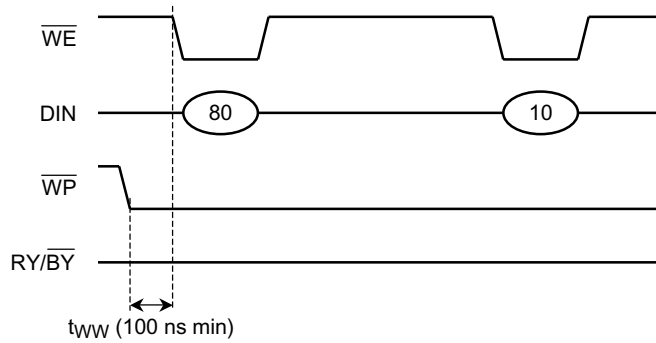
(10) Note regarding the  $\overline{WP}$  signal

The Erase and Program operations are automatically reset when  $\overline{WP}$  goes Low. The operations are enabled and disabled as follows:

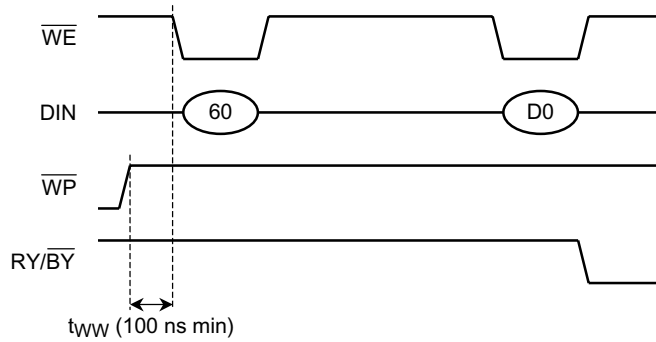
Enable Programming



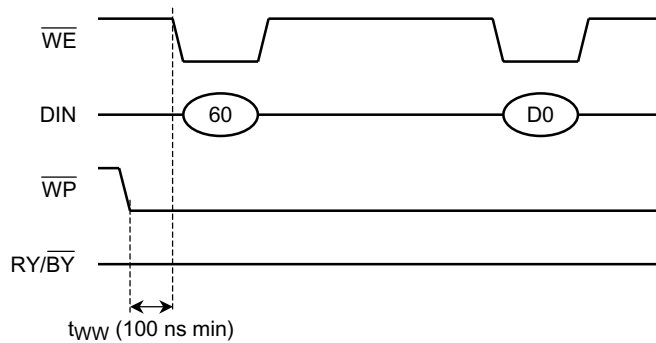
Disable Programming



Enable Erasing



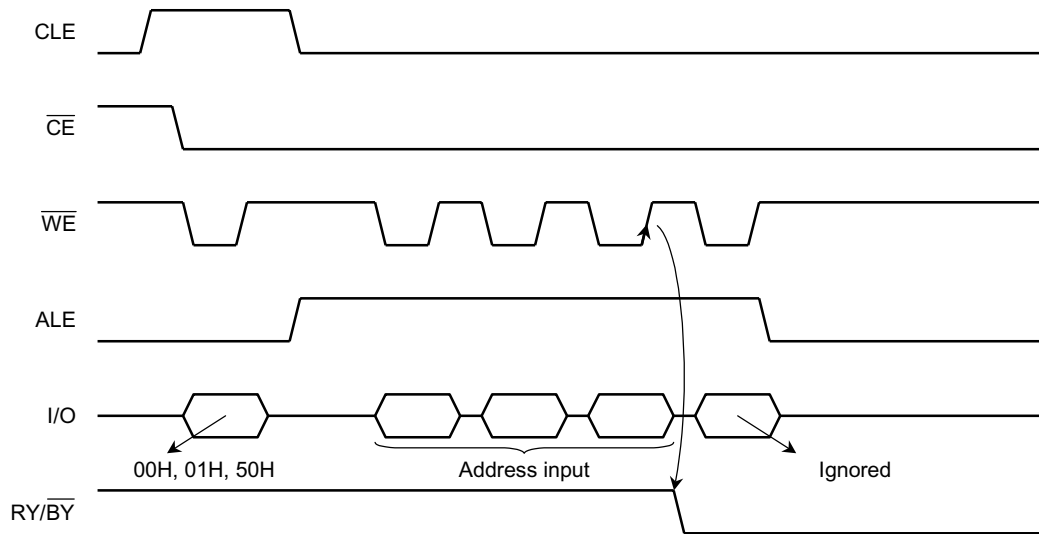
Disable Erasing



(11) When four address cycles are input

Although the device may read in a fourth address, it is ignored inside the chip.

Read operation



Internal read operation starts when  $\overline{WE}$  goes High in the third cycle.

Figure 22.

Program operation

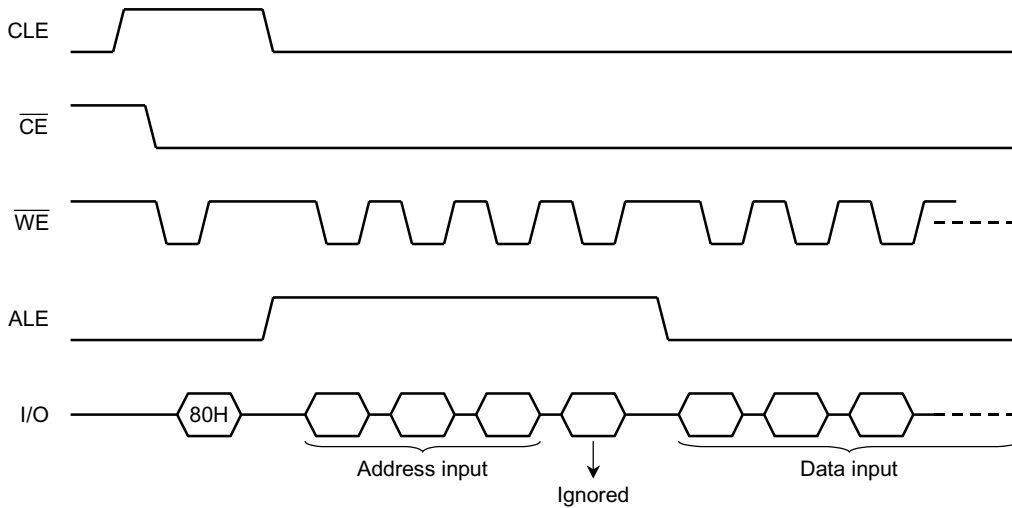


Figure 23.

(12) Several programming cycles on the same page (Partial Page Program)

A page can be divided into up to 3 segments. Each segment can be programmed individually as follows:

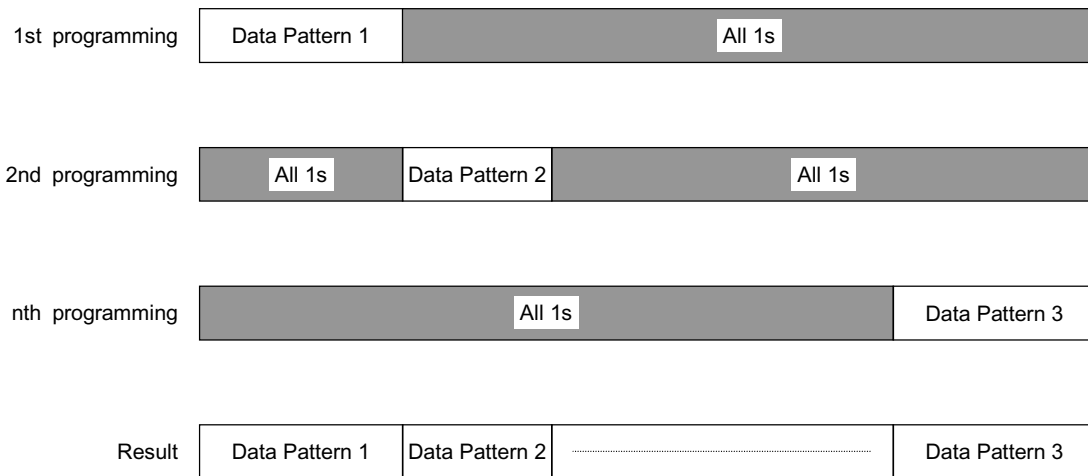


Figure 24.

Note: The input data for unprogrammed or previously programmed page segments must be "1" (i.e. the inputs for all page bytes outside the segment which is to be programmed should be set to all "1").

(13) Note regarding the  $\overline{RE}$  signal

$\overline{RE}$  The internal column address counter is incremented synchronously with the  $\overline{RE}$  clock in Read mode. Therefore, once the device has been set to Read mode by a "00H", "01H" or "50H" command, the internal column address counter is incremented by the  $\overline{RE}$  clock independently of the address input timing. If the  $\overline{RE}$  clock input pulses start before the address input, and the pointer reaches the last column address, an internal read operation (array to register) will occur and the device will enter Busy state. (Refer to Figure 25.)

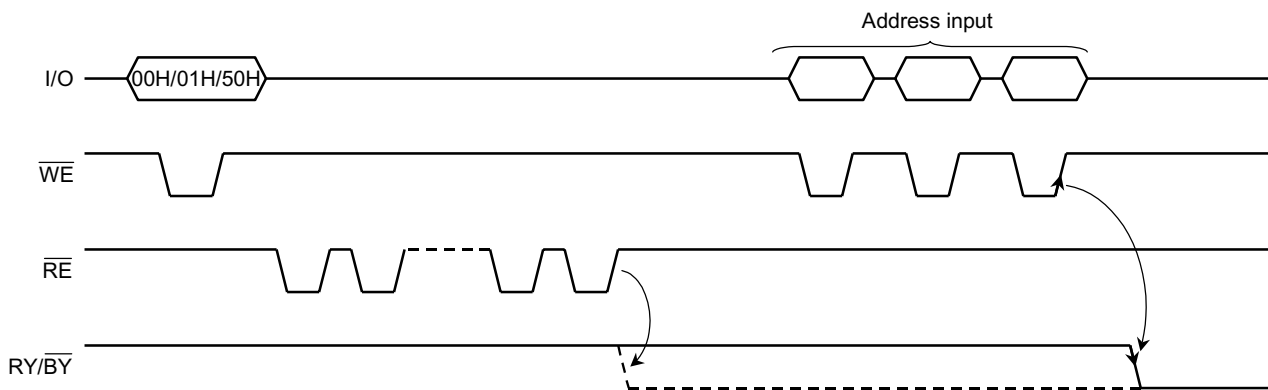


Figure 25.

Hence the  $\overline{RE}$  clock input must start after the address input.

(14) Invalid blocks (bad blocks)

The device contains unusable blocks. Therefore, at the time of use, please check whether a block is bad and do not use these bad blocks.

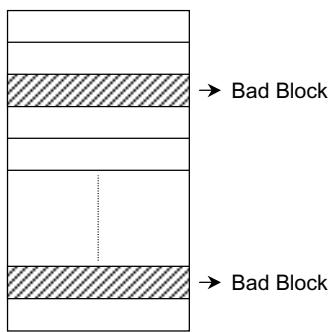


Figure 26.

At the time of shipment, all data bytes in a Valid Block are FFH. For Bad Block, all bytes are not in the FFH state. Please don't perform erase operation to Bad Block.

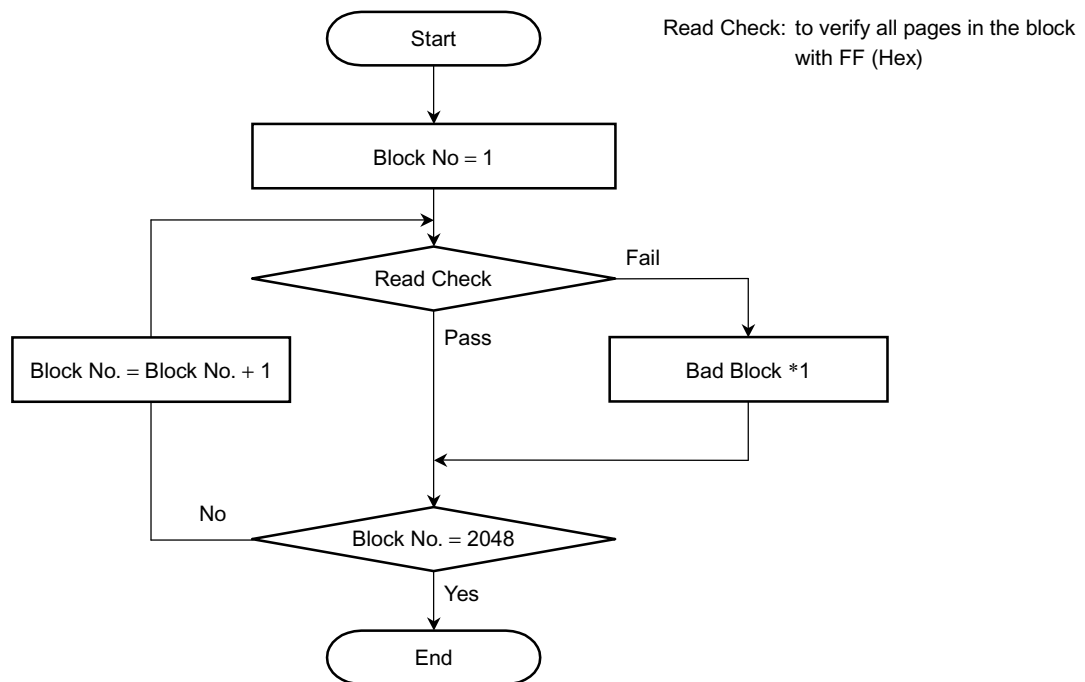
Check if the device has any bad blocks after installation into the system. Figure 27 shows the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the Bit line by the Select gate

The number of valid blocks at the time of shipment is as follows:

|                           | MIN  | TYP. | MAX  | UNIT  |
|---------------------------|------|------|------|-------|
| Valid (Good) Block Number | 2008 | —    | 2048 | Block |

Bad Block Test Flow



\*1: No erase operation is allowed to detected bad blocks

Figure 27

(15) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation.

The following possible failure modes should be considered when implementing a highly reliable system.

| FAILURE MODE |                              | DETECTION AND COUNTERMEASURE SEQUENCE         |
|--------------|------------------------------|---|
| Block        | Erase Failure                | Status Read after Erase → Block Replacement   |
| Page         | Programming Failure          | Status Read after Program → Block Replacement |
| Single Bit   | Programming Failure<br>1 → 0 | (1) Block Verify after Program → Retry        |
|              |                              | (2) ECC                                       |

- ECC: Error Correction Code
- Block Replacement

Program

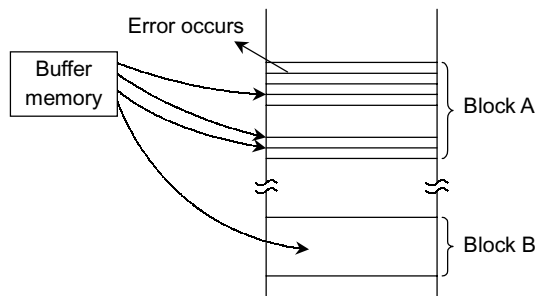


Figure 28.

When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

Erase

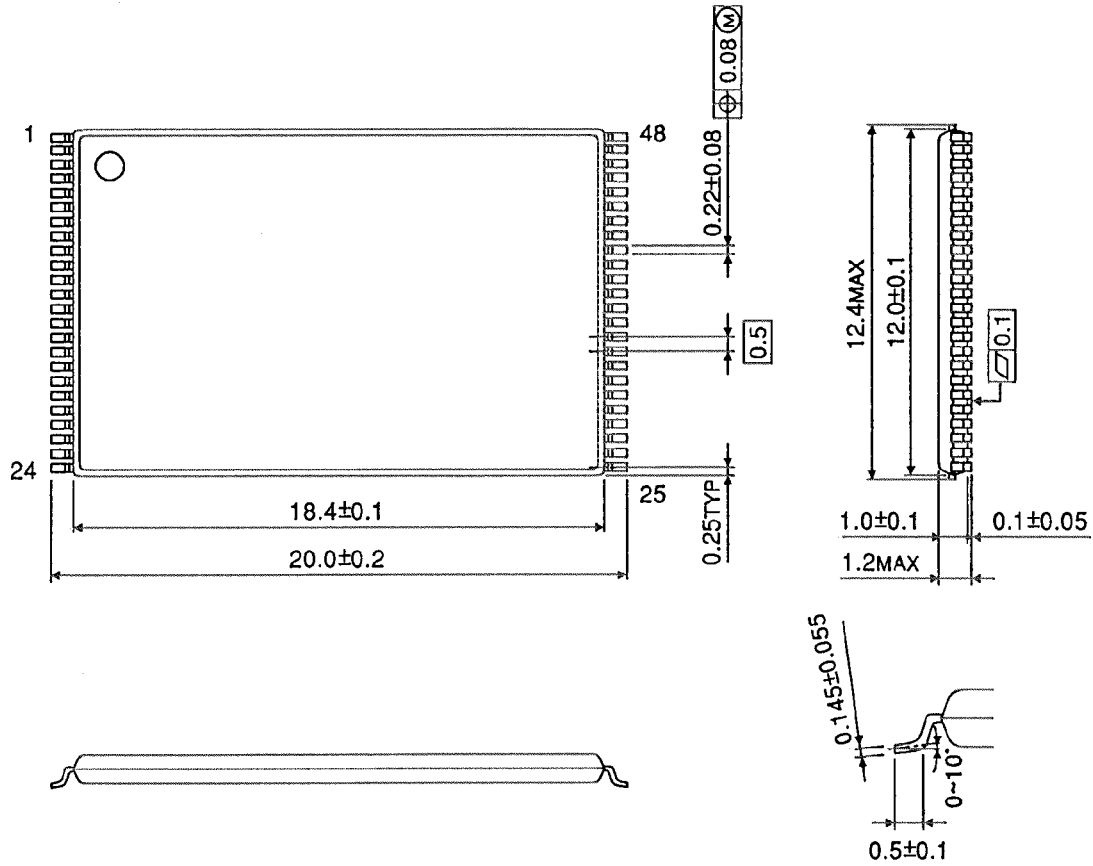
When an error occurs in an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).



## Package Dimensions

TSOPI48-P-1220-0.50

Unit: mm



Weight: 0.53 g (typ.)