TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288 WORDS × 8 BIT STATIC RAM

DESCRIPTION

The TC554001AF/AFT/ATR is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5V ± 10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 10mA/MHz(typ) and minimum cycle time of 70 ns. It is automatically placed in low-power mode at 2 μA standby current (typ) when chip enable ($\overline{CE}$) is asserted high. There are two control inputs. $\overline{CE}$ is used to select the device and for data retention control, and output enable ($\overline{OE}$) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required.The TC554001AF/AFT/ATR is available in a standard plastic 32-pin small-outline package(SOP) and normal and reverse pinout plastic 32-pin thin-small-outline package(TSOP).

FEATURES

- Low-power dissipation
  Operating: 55 mW/MHz (typical)
- Single power supply voltage of 5 V ± 10 %
- Power down features using $\overline{CE}$
- Data retention supply voltage of 2.0 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Standby Current (maximum) :

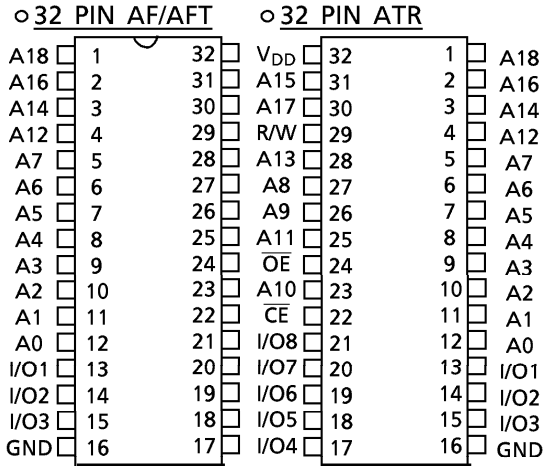
	TC554001AF/AFT/ATR	
	-70, -85, -10	-75L, -85L, -10L
5.5V	100 μA	50 μA
3.0V	50 μA	25 μA

- Access Time (maximum)

	TC554001AF/AFT/ATR		
	-70, -70L	-85, -85L	-10, -10L
Access Time	70 ns	85 ns	100 ns
$\overline{CE}$ Access Time	70 ns	85 ns	100 ns
$\overline{OE}$ Access Time	35 ns	45 ns	50 ns

- Package:
  SOP32-P-525-1.27 (AF) (Weight: 1.14g typ)
  TSOP II 32-P-400-1.27 (AFT) (Weight: 0.53g typ)
  TSOP II 32-P-400-1.27A (ATR) (Weight: 0.53g typ)

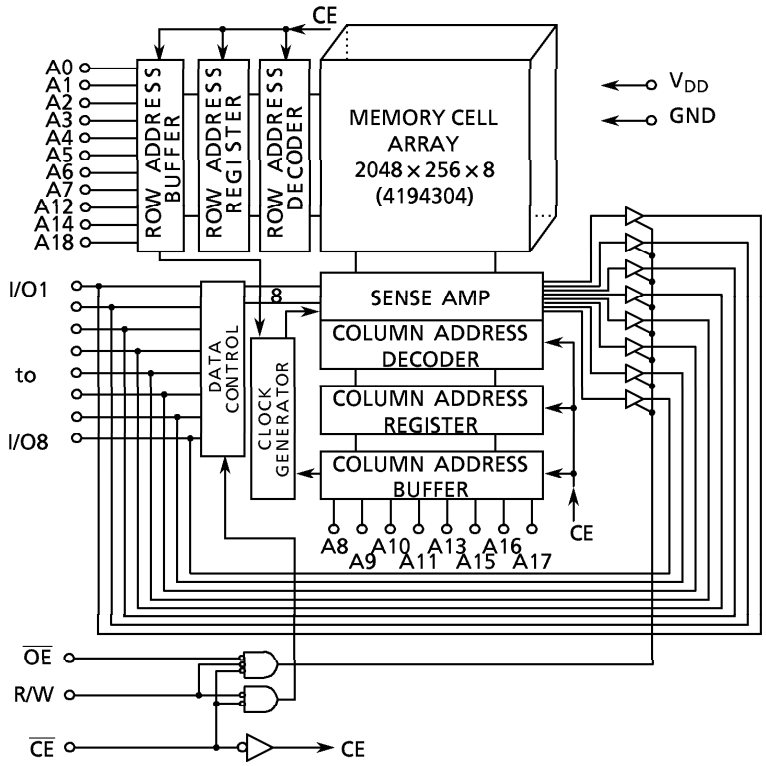
PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

A0 to A18	Address Inputs
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
I/O1 to I/O8	Data Input/Output
V_{DD}	Power (+ 5 V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 to I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	×	L	D_{IN}	I_{DDO}
Output Disabled	L	H	H	High-Z	I_{DDO}
Standby	H	×	×	High-Z	I_{DDS}

Note: × = don't care. H = logic high. L = logic low.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	− 0.3 to 7.0	V
V_{IN}	Input Voltage	− 0.3* to 7.0	V
$V_{I/O}$	Input and Output Voltage	− 0.5 to V_{DD} + 0.5	V
P_D	Power Dissipation	0.6	W
Tsolder	Soldering Temperature (10 s)	260	°C
Tstrg.	Storage Temperature	− 55 to 150	°C
Topr.	Operating Temperature	0 to 70	°C

* − 3.0 V when measured at a pulse width of 50 ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	– 0.3*	–	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	V

* – 3.0 V when measured at a pulse width of 50 ns

DC CHARACTERISTICS (Ta = 0° to 70°C, V_{DD} = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION				MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{DD}				–	–	± 1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4 V				– 1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V				2.1	–	–	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 V to V_{DD}				–	–	± 1.0	μA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL} and R/W = V_{IH} I_{OUT} = 0 mA Other Inputs = V_{IH}/V_{IL}	Tcycle	min		–	–	70	mA
				1 μs		–	15	–	
I_{DDO2}		$\overline{CE}$ = 0.2 V and R/W = V_{DD} – 0.2 V I_{OUT} = 0 mA Other Inputs = V_{DD} – 0.2 V/0.2 V	Tcycle	min		–	–	60	mA
				1 μs		–	10	–	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}				–	–	3	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} – 0.2 V V_{DD} = 2.0 to 5.5 V Ta = 0° to 70°C	-70, -85, -10	Ta = 25°C		–	2	–	μA
				Ta = 0° to 70°C		–	–	100	
			-70L, -85L, -10L	Ta = 25°C		–	2	5	
				Ta = 0° to 70°C		–	–	50	

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = 0° to 70°C, V_{DD} = 5 V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC554001AF/AFT/ATR						UNIT
		-70, -70L		-85, -85L		-10, -10L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	70	–	85	–	100	–	ns
t_{ACC}	Address Access Time	–	70	–	85	–	100	
t_{CO}	Chip Enable Access Time	–	70	–	85	–	100	
t_{OE}	Output Enable Access Time	–	35	–	45	–	50	
t_{COE}	Chip Enable Low to Output Active	10	–	10	–	10	–	
t_{OEE}	Output Enable Low to Output Active	5	–	5	–	5	–	
t_{OD}	Chip Enable High to Output High-Z	–	25	–	30	–	35	
t_{ODO}	Output Enable High to Output High-Z	–	25	–	30	–	35	
t_{OH}	Output Data Hold Time	10	–	10	–	10	–	

WRITE CYCLE

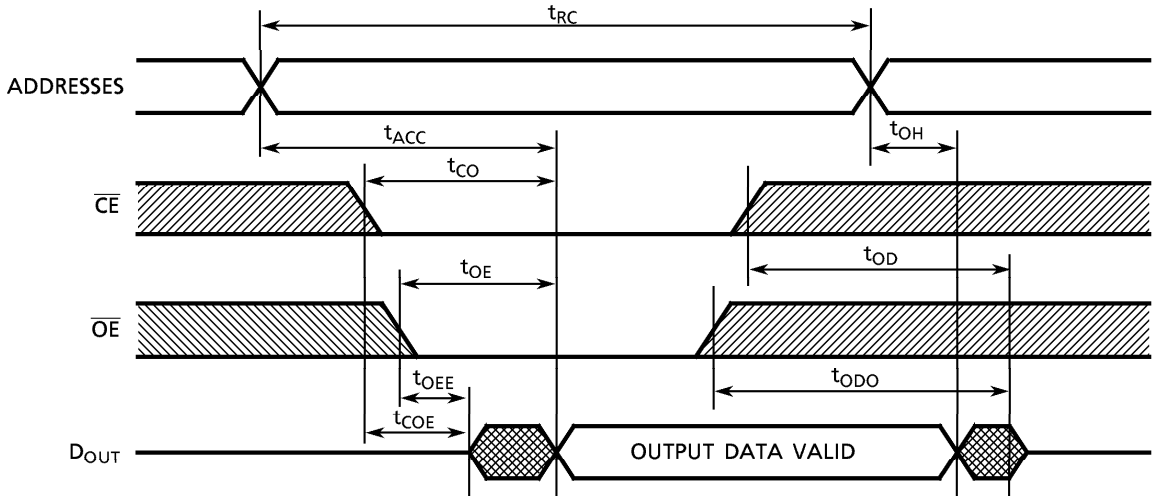
SYMBOL	PARAMETER	TC554001AF/AFT/ATR						UNIT
		-70, -70L		-85, -85L		-10, -10L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	70	–	85	–	100	–	ns
t_{WP}	Write Pulse Width	50	–	55	–	60	–	
t_{CW}	Chip Enable to End of Write	60	–	70	–	80	–	
t_{AS}	Address Setup Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{ODW}	R/W Low to Output High-Z	–	25	–	30	–	35	
t_{OEW}	R/W Hige to Output Active	5	–	5	–	5	–	
t_{DS}	Data Setup Time	30	–	35	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	

AC TEST CONDITIONS

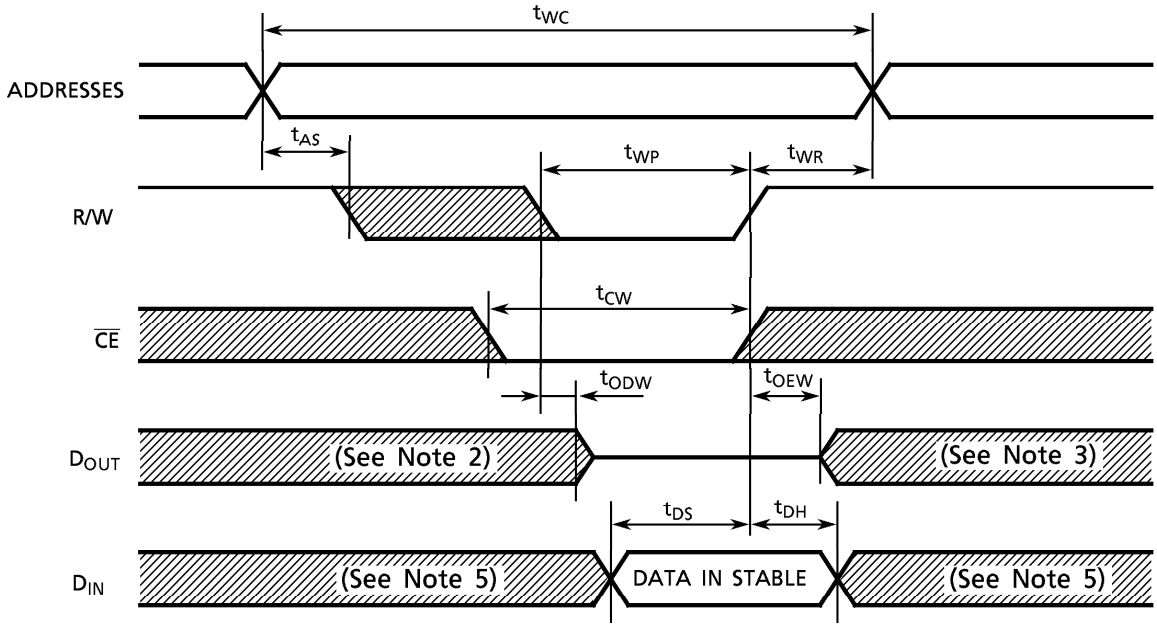
Output Load: 100 pF + one TTL gate
Input Pulse Level: 0.6 V, 2.4 V
Timing Measurements: 1.5 V
Reference Level: 1.5 V
t_r, t_F: 5 ns

TIMING WAVEFORMS

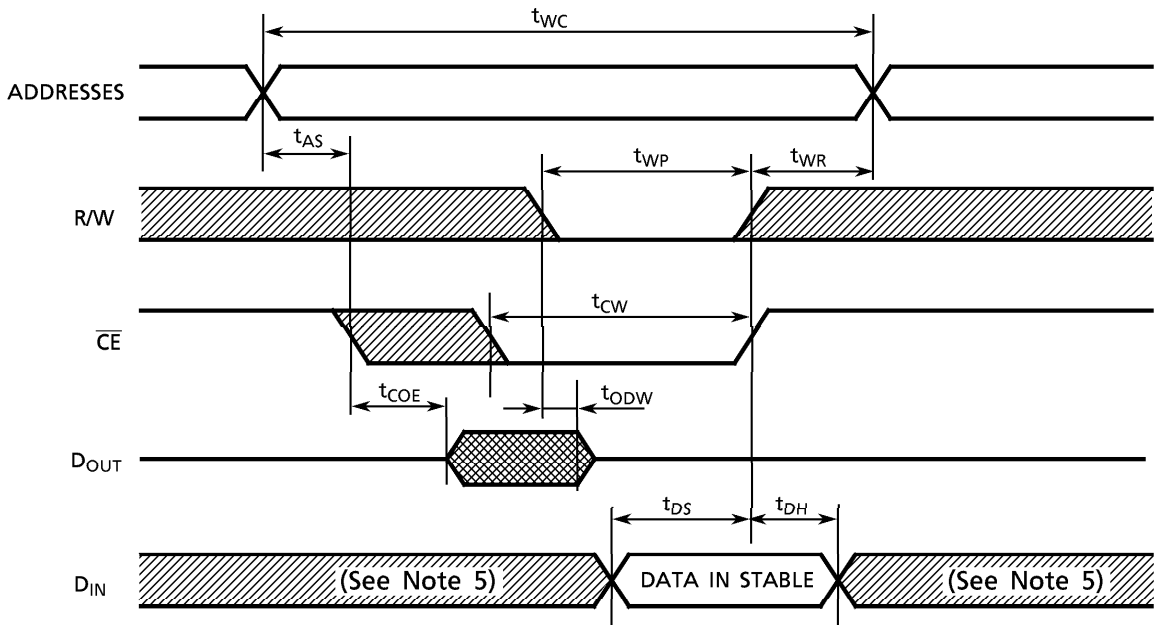
READ CYCLE (See Note 1)



WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 ($\overline{CE}$ CONTROLLED) (See Note 4)



(1) R/W remains High for Read Cycle.

(2) If $\overline{CE}$ goes coincident with or after R/W goes LOW, the output will remain at high impedance.

(3) If $\overline{CE}$ goes HIGH coincident with or before R/W goes HIGH, the output will remain at high impedance.

(4) IF $\overline{CE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

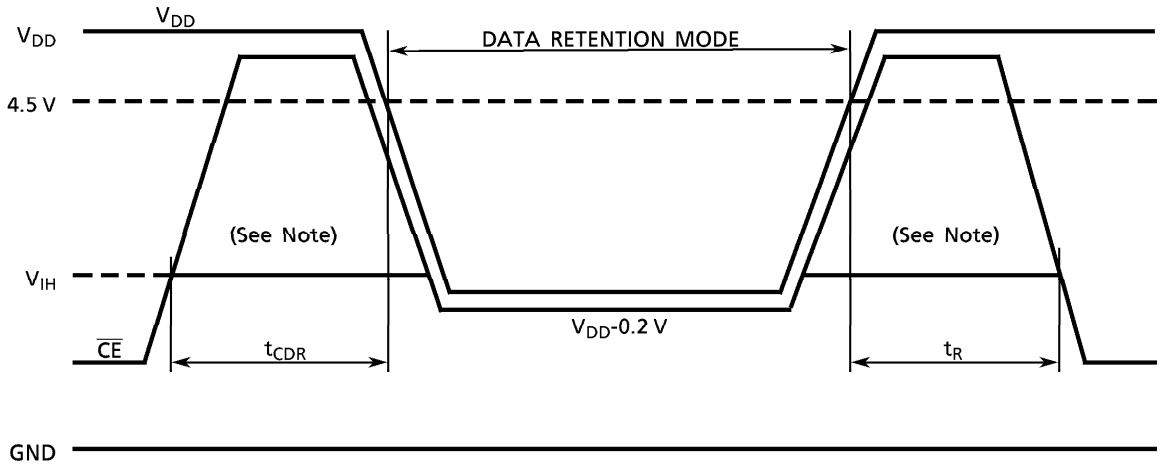
(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = 0° to 70°C)

SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
V_{DH}	Data Retention Supply Voltage			2.0	–	5.5	V
I_{DDS2}	Standby Current	-70, -85, -10	V_{DH} = 3.0 V	–	–	50	μA
			V_{DH} = 5.5 V	–	–	100	
		-70L, -85L, -10L	V_{DH} = 3.0 V	–	–	25*	
			V_{DH} = 5.5 V	–	–	50	
t_{CDR}	Chip Deselect to Data Retention Mode Time			0	–	–	nS
t_R	Recovery Time			5	–	–	mS

* 5 μA (max) at Ta = 0° to 40°C

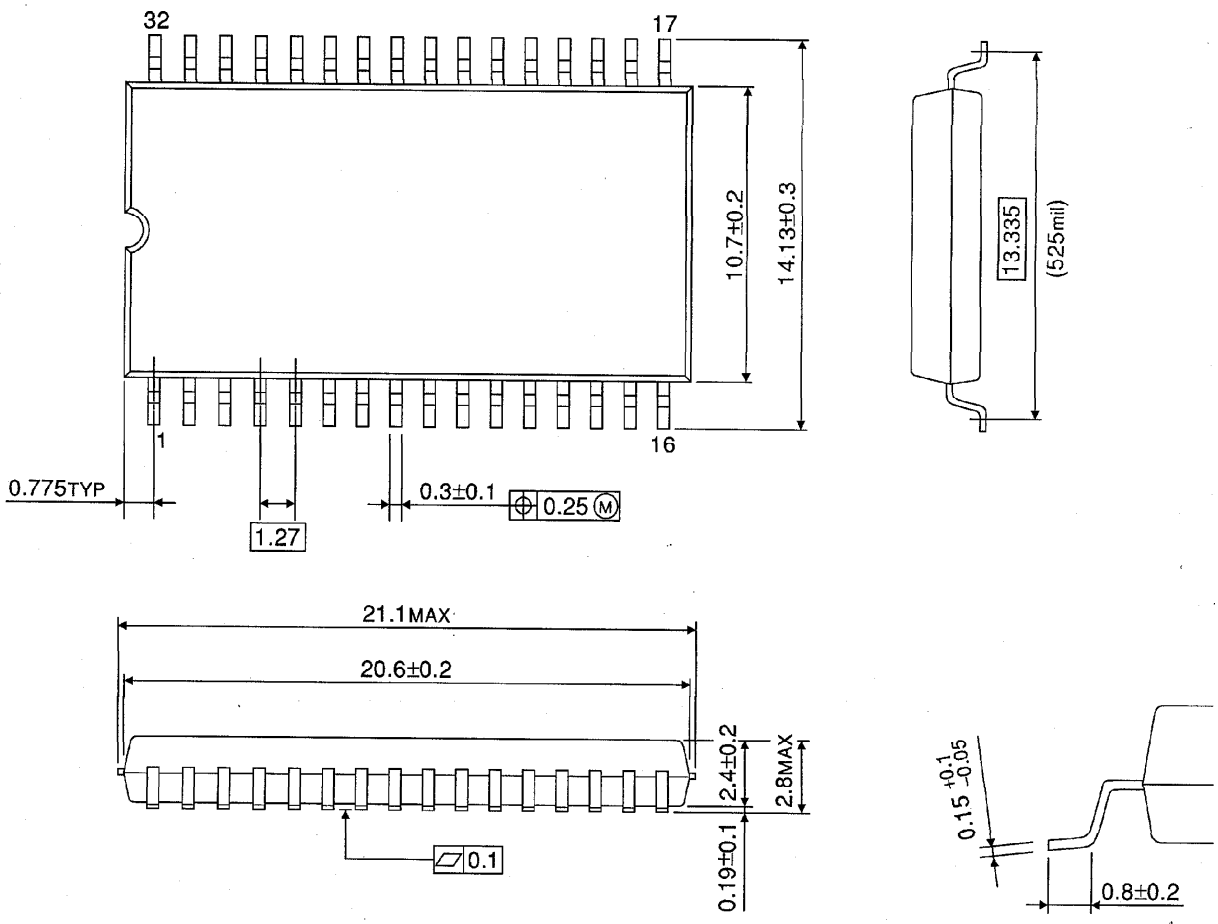
$\overline{CE}$ Controlled Data Retention Mode



Note: When $\overline{CE}$ is operating at the V_{IH} level (2.2V), the standby current is given by I_{DDS1} during the transition of V_{DD} from 4.5 to 2.4V.

PACKAGE DIMENSIONS (SOP32-P-525-1.27)

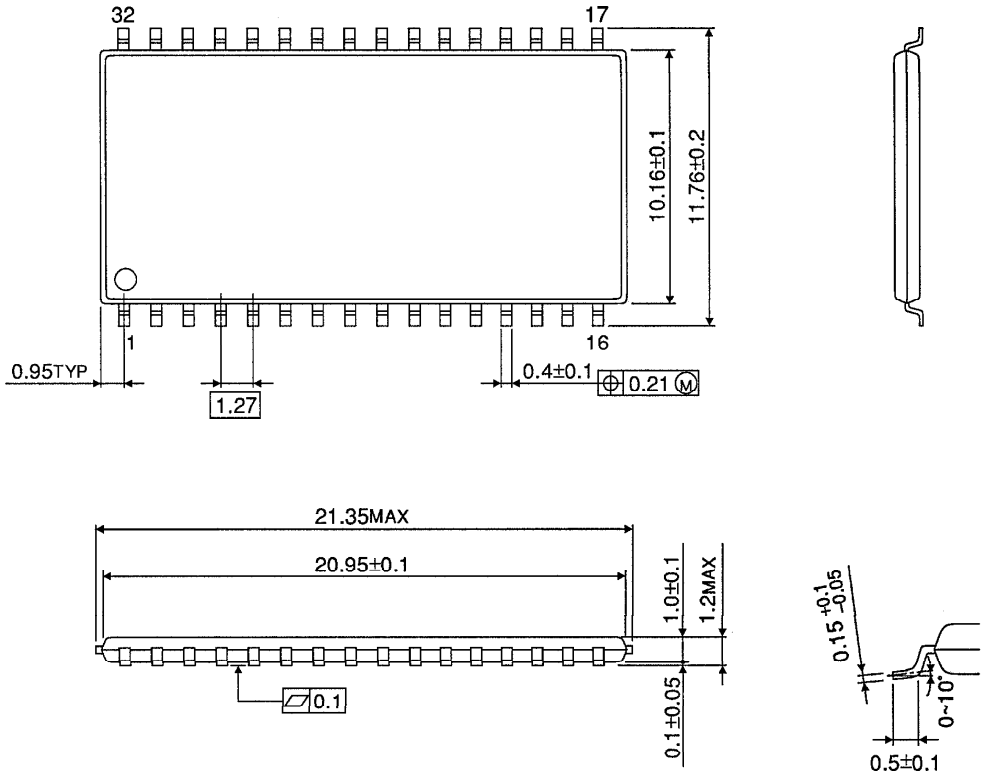
Unit in mm



Weight: 1.14g (typ)

PACKAGE DIMENSIONS (TSOPII 32-P-400-1.27)

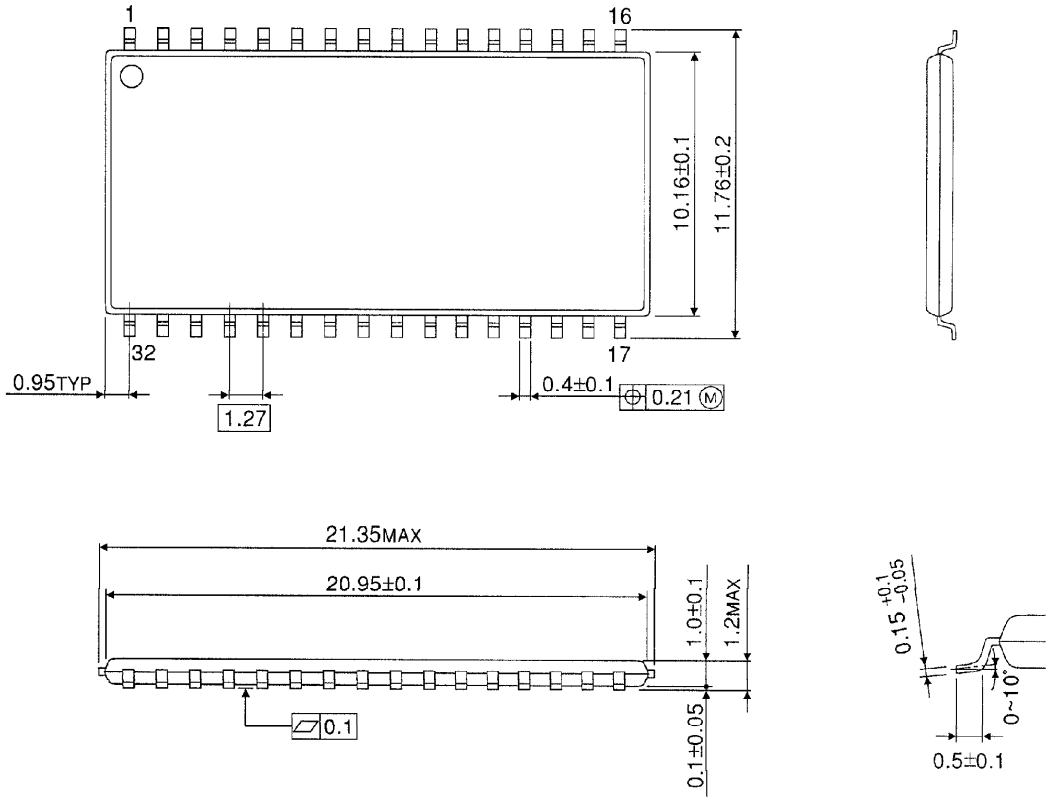
Unit in mm



Weight: 0.53g (typ)

PACKAGE DIMENSIONS (TSOPII 32-P-400-1.27A)

Unit in mm



Weight: 0.53g (typ)