

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

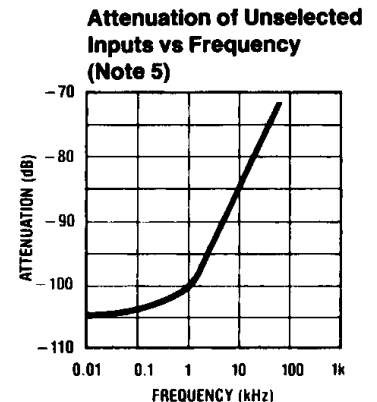
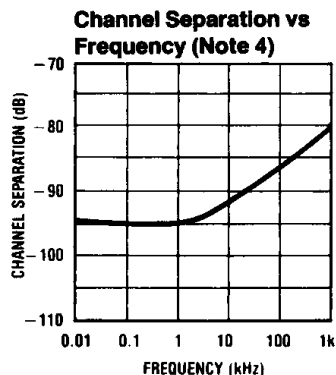
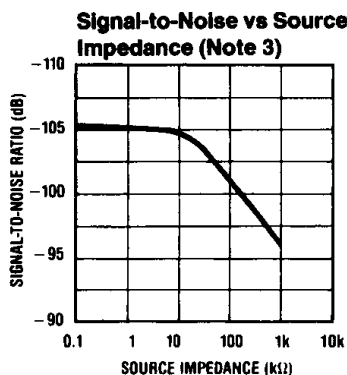
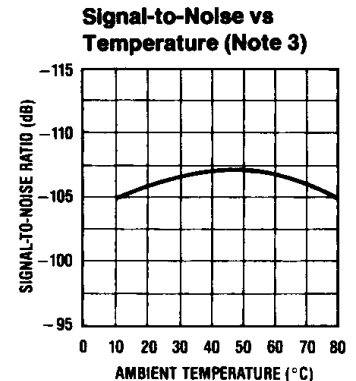
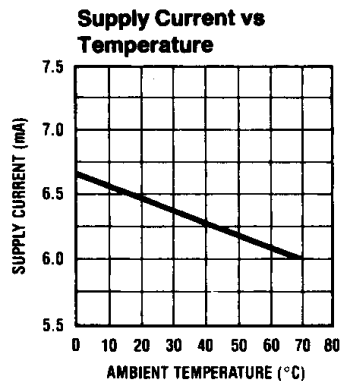
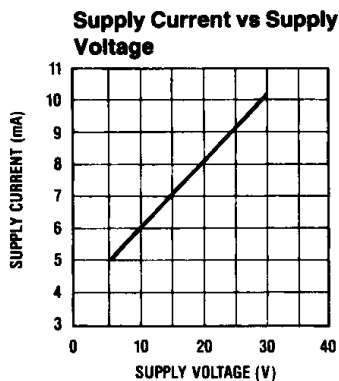
Supply Voltage 28V
Pin 7 Input Current 5 mA

Operating Temperature Range -20°C to +70°C
Storage Temperature Range -65°C to +150°C
Power Dissipation (Note 1) 1.3W
Lead Temp. (Soldering, 10 seconds) 260°C

Electrical Characteristics $V_S = 12V, T_A = 25^\circ C$

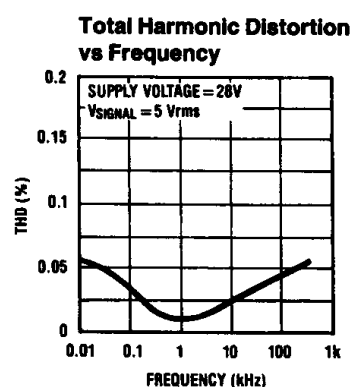
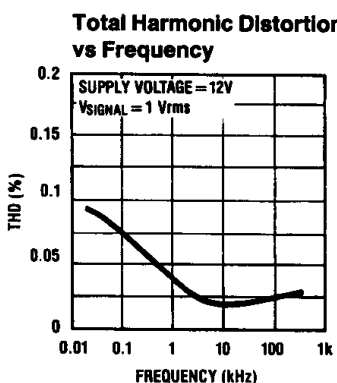
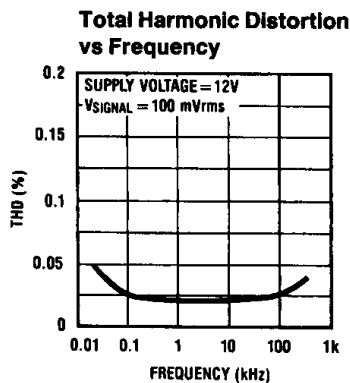
Parameter	Conditions	Typical	Tested Limit (Note 7)	Design Limit (Note 8)	Units (Limits)
Supply Voltage			28		V _(max)
Supply Voltage				5	V _(min)
Supply Current	V _{SUPPLY} = 12V	6.4	8.5		mA _(max)
	V _{SUPPLY} = 28V	10	14		mA _(max)
Voltage Gain		0	±0.7		dB
Signal Handling (Notes 2, 6)	V _{SUPPLY} = 12V	3.0	2.8		V _{rms(min)}
Small-Signal Bandwidth		300			kHz
Distortion THD	V _{SIGNAL} = 1 V _{rms} @ 1 kHz	0.04	0.1		% _(max)
Noise Voltage at Output (Note 3)	CCIR/ARM R _S = 0Ω	5		20	μV _(max)
Channel Separation (Note 4)	V _{SIGNAL} = 1 V _{rms} @ 1 kHz	-95		-70	dB _(min)
Relative Output in Muted State	V _{SIGNAL} = 1 V _{rms} @ 1 kHz	-90	-70		dB _(min)
Output Impedance		10			Ω
Signal Input Impedance		30			MΩ
Logic Low Input Level				0.8	V _(max)
Logic High Input Level				2.0	V _(min)
Logic High Input Level				V _{SUPPLY}	V _(max)

Typical Performance Characteristics ($V_S = 12V, T_A = 25^\circ C$ unless otherwise noted)

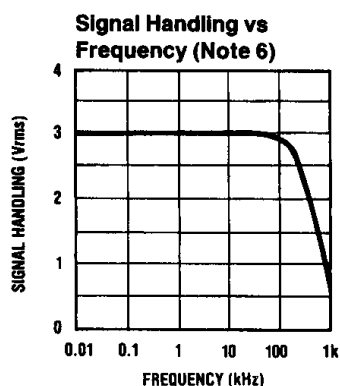


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Typical Performance Characteristics (Continued) ($V_S = 12V$, $T_A = 25^\circ C$ unless otherwise noted)



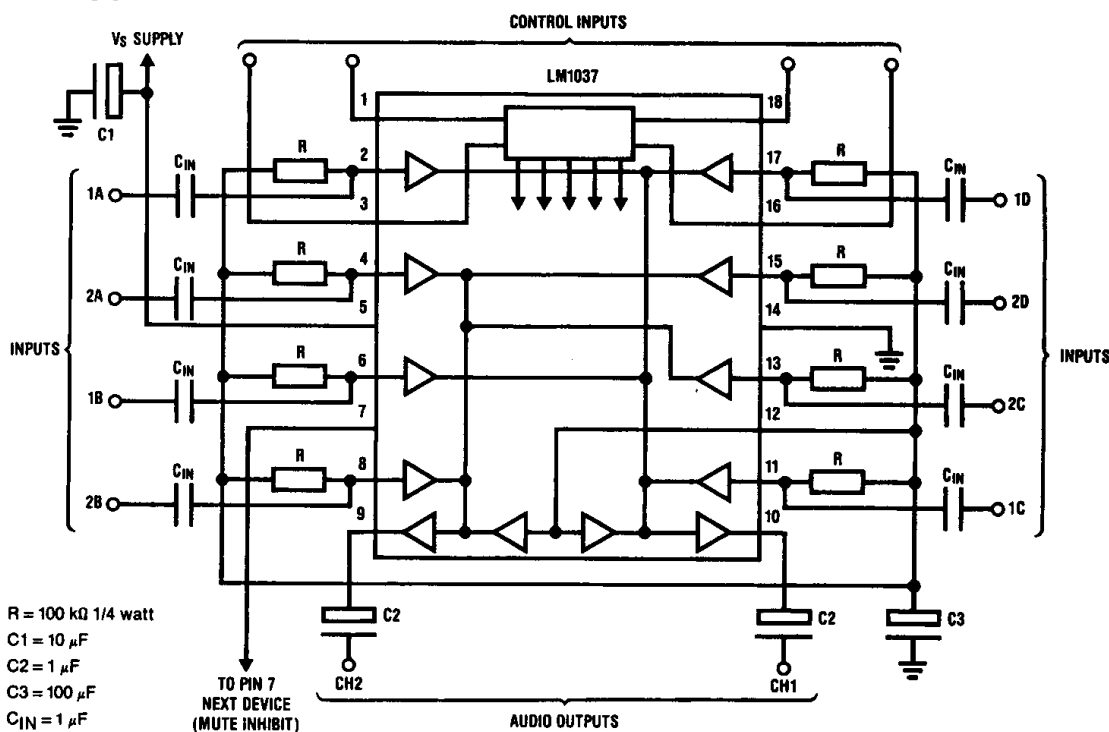
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- Note 1:** Above $T_A = 25^\circ C$ derate based on $T_J \text{ max} = 150^\circ C$ and $\theta_{JA} = 90^\circ C/W$.
- Note 2:** The instantaneous maximum voltage difference between any two input pins of one channel is 9.6V. Voltages in excess of this level may cause increased distortion and degraded channel separation.
- Note 3:** Gaussian noise, monitored over a period of 50 ms per channel, with a CCIR filter referenced to 2 kHz, and an average-responding meter. Signal to noise ratios are referenced to 1V rms input signal.
- Note 4:** The level of output signal of a selected undriven amplifier with respect to the output level of a selected driven amplifier. For test purposes, signal is applied to only one input and all other inputs are decoupled to eliminate stray pick-up through external components. Channel separation is then defined as the ratio of signal levels of the two output pins.
- Note 5:** For test purposes, signals are connected to three unselected input pins of one channel group and all other inputs are decoupled to eliminate stray pick-up through external components.
- Note 6:** Supply voltage 12V; signal handling defined at 1% distortion, 1 kHz.
- Note 7:** Guaranteed and 100% production tested.
- Note 8:** Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Typical Application



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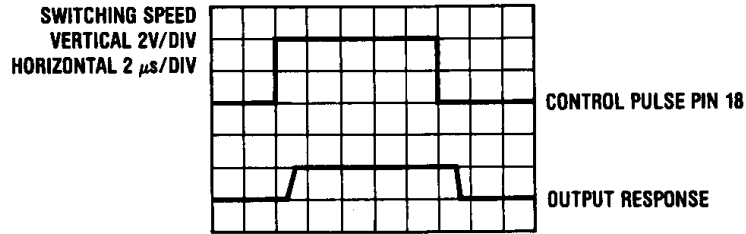
Truth Tables

LM1037

Channel selection is achieved by the application of DC voltages to the control pins. Unselected control pins should be held low.

DC Control Pin in HIGH State	Input Pair Switched to Output Pins (10, 9)
16	A (2,4)
18	B (6,8)
1	C (11,13)
3	D (17,15)
None	Mute (12)

Low switching level (V_L) < 0.8V
 High switching level (V_H) > 2.0V and up to V_{SUPPLY}



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2 DEVICES CONNECTED IN PARALLEL

To increase the channel switching capacity, two or more devices can be connected together by the direct coupling of the mute inhibit pin 7 and the output pins 9 and 10. Only one output capacitor is required for each common output.

	DC Control Pin in HIGH State	Input Pair Switched to Output Pins (10,9)
Device Number 1	16	A (2,4)
	18	B (6,8)
	1	C (11,13)
	3	D (17,15)
Device Number 2	16	A (2,4)
	18	B (6,8)
	1	C (11,13)
	3	D (17,15)
	None	Mute (12)

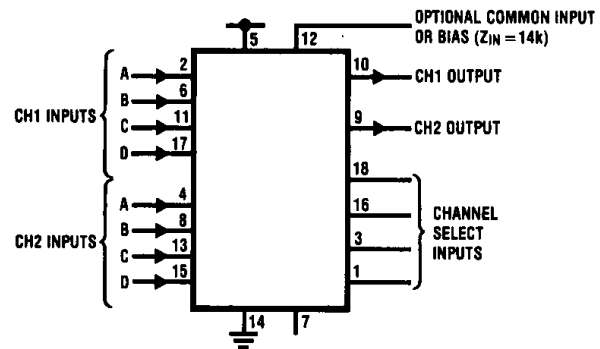
Pin Function Description

Device Pins	Description
Pin 16—Inputs A Select Pin 18—Inputs B Select Pin 1—Inputs C Select Pin 3—Inputs D Select	A high input level selects the corresponding channel. Only one channel should be selected at a time. Unselected channels should have their select inputs at a low level. Open circuit pins represent a high input level.
Pins 2, 6, 11, 17— Inputs for Output 1 (Pin 10) Pins 4, 8, 13, 15— Inputs for Output 2 (Pin 9) Pin 12—Mute Bias Level	Two sets of four high impedance channel inputs for the connection of signals to be switched. The DC level at this pin is applied to the outputs when no input is selected and pin 7 is open. The level is internally set by a 25 k Ω and 33 k Ω potential divider at 0.6 V _S . This level may be adjusted by means of external resistors. Pin 12 may also be used as an additional common input in which case this signal is present on both outputs when no control input is applied.
Pin 7—Mute Inhibit Input	With this pin unconnected and no channel selection input is present; the mute level at pin 12 is applied to the outputs. With pin 7 grounded and no channel selection input present, the device output emitter-followers are disabled allowing parallel connection to other device outputs. This pin is a current input and any current applied should be limited to 5 mA maximum. Pin 7 of several devices may be directly connected for parallel operation.
Pin 9—Output 2 Pin 10—Output 1	These are common output pins for each channel. There are three possible output conditions: 1) Signal selected from 1 of 4 inputs. 2) Mute level output. 3) Device not selected—internal 6 k Ω pull-down resistors to ground.
Pin 5 Pin 14	Positive supply voltage. Negative or ground supply voltage.

Application Hints

The basic circuit arrangement with minimum external components for use with DC coupled signals is shown in *Figure 1*. This arrangement may be used in a normal signal selection system or in the feedback path of DC coupled amplifiers for example to make a simple dual programmable power supply. By switching feedback connections dual programmable gain or frequency response amplifiers may be obtained.

For switching between signal sources in stereo systems the LM1037 may be connected as shown in the typical application circuit. The input bias is obtainable from pin 12 or an alternative source may be used. If split supply operation is required, pin 12 may be grounded and the signals referenced to ground.



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DC coupled signals $1.2V < V_{IN} < V_S - 1V$

FIGURE 1

Simplified Circuit Schematic (All signal and control inputs are Darlington connected)

