PRELIMINARY

FEMTOCLOCKS™ MULTI-RATE 3.3V, 2.5V LFPECL FREQUENCY SYNTHESIZER

ICS843034

General Description

The ICS843034 is a general purpose, low phase noise LVPECL synthesizer which can generate frequencies for a wide variety of applications. The ICS843034 has a 4:1 input Multiplexer from which the following inputs can be selected: 1 differential input, 1 single-ended input, or two crystal oscillators, thus making the device ideal for frequency translation or frequency generation. Each differential LVPECL output pair has an output divider which can be independently set so that two different frequencies can be generated. Additionally, each LVPECL output pair has a dedicated power supply pin so the outputs can run at 3.3V or 2.5V. The ICS843034-02 also supplies a buffered copy of the reference clock or crystal frequency on the single-ended REF_CLK pin which can be enabled or disabled (disabled by default). The output frequency can be programmed using either a serial or parallel programming interface.

The phase jitter of the ICS843034 is less than 1ps rms, making it suitable for use in Fibre Channel, SONET, and Ethernet applications.

Example applications include systems which must support both FEC and non FEC rates. In 10Gb Fibre Channel, for example, you can use a 25.5MHz crystal to generate a 159.375MHz reference clock, and then switch to a 20.544MHz crystal to generate 164.355MHz for 66/64 FEC. Other applications could include supporting both Ethernet frequencies and SONET frequencies in an application. When Ethernet frequencies are needed, a 25MHz crystal can be used and when SONET frequencies are needed, the input MUX can be switched to select a 38.88MHz crystal.

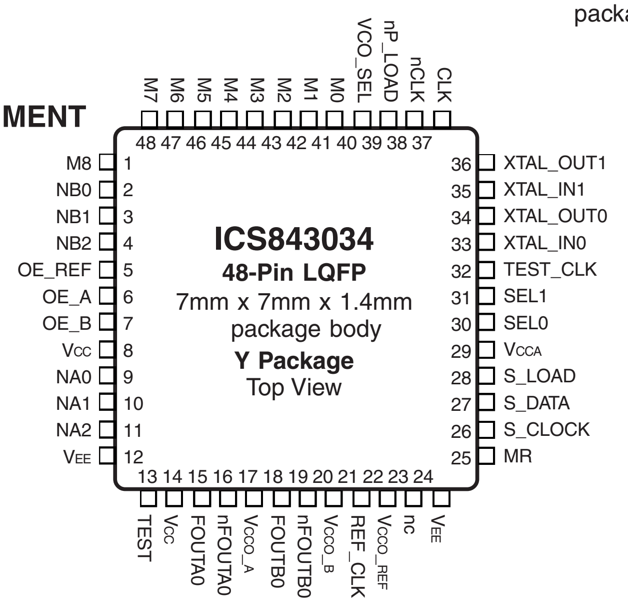
Features

- Dual differential 3.3V LVPECL outputs which can be set independently for either 3.3V or 2.5V
- 4:1 Input Mux:
  - One differential input
  - One single-ended input
  - Two crystal oscillator interfaces
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- TEST_CLK accepts LVCMOS or LVTTL input levels
- Output frequency range: 35MHz to 750MHz
- Crystal input frequency range: 12MHz to 40MHz
- VCO range: 560MHz to 750MHz
- Parallel or serial interface for programming feedback divider and output dividers
- RMS phase jitter at 333.33MHz, using a 22.222MHz crystal (12kHz to 20MHz): 0.80ps (typical)
- Supply voltage modes:

  LVPECL outputs (core/outputs):
  3.3V/3.3V
  3.3V/2.5V

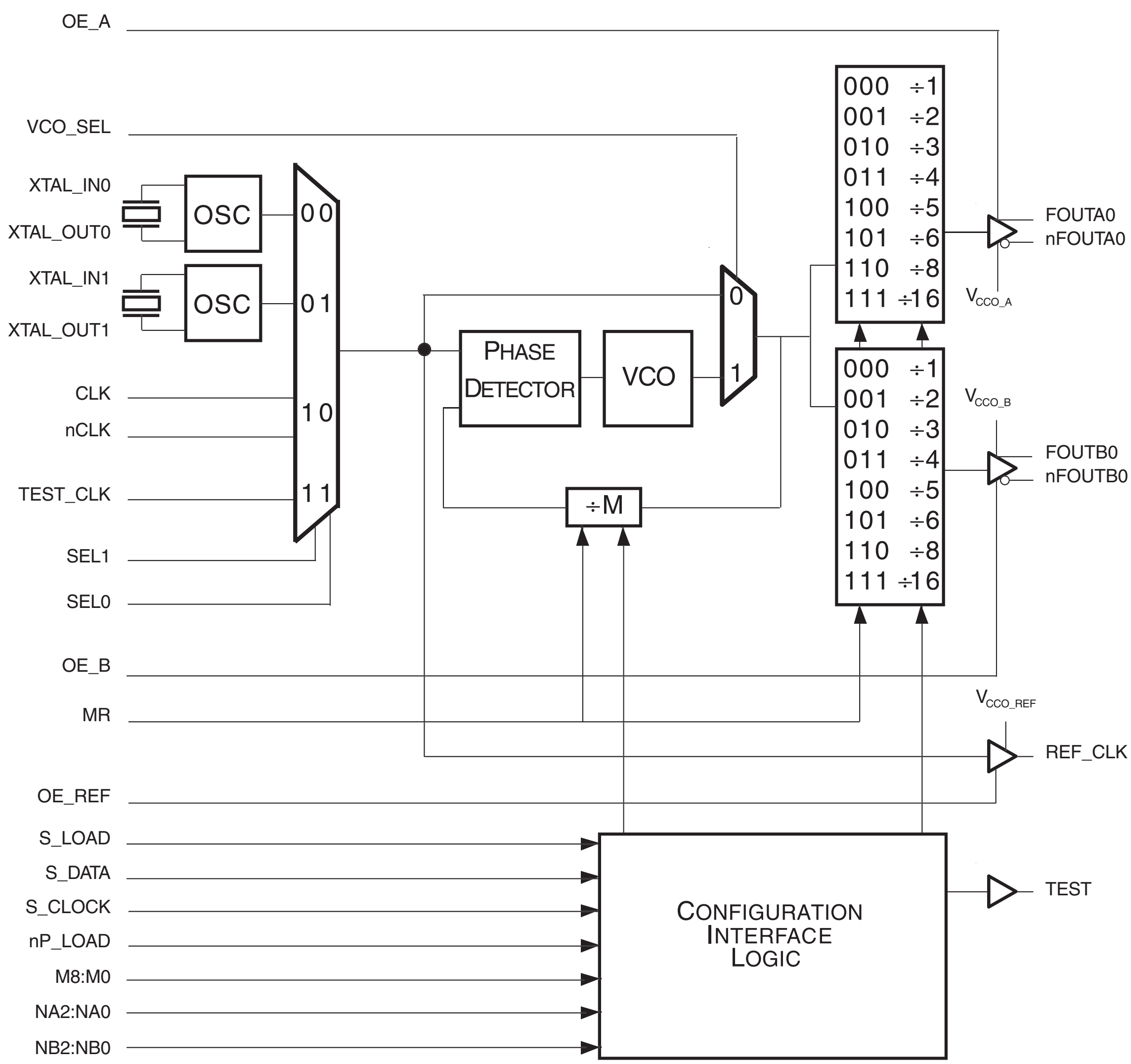
  REF_CLK output (core/outputs):
  3.3V/3.3V
- 0°C to 70°C ambient operating temperature
- Industrial temperature available upon request
- Available in both standard and lead-free RoHS-compliant packages

Pin Assignment



The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

Block Diagram



FUNCTIONAL DESCRIPTION

NOTE: The functional description that follows describes operation using a 25MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.

The ICS843034 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is fed into the phase detector. A 25MHz crystal provides a 25MHz phase detector reference frequency. The VCO of the PLL operates over a range of 560MHz to 750MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The ICS843034 supports either serial or parallel programming modes to program the M feedback divider and N output divider. *Figure 1* shows the timing diagram for each mode. In parallel mode, the nP_LOAD input is initially LOW. The data on the M, NA, and NB inputs are passed directly to the M divider and both N output dividers. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M and N dividers remain loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result, the M and Nx bits can be hardwired to set the M divider and Nx output divider to a specific default state that will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows: $\mathbf{fVCO = fxtal \times M}$

The M value and the required values of M0 through M8 are shown in Table 3B to program the VCO Frequency Function Table. Valid M values for which the PLL will achieve lock for a 25MHz reference are defined as 23 ≤ M ≤ 30. The frequency out is defined as follows: $\mathbf{FOUT = \frac{fVCO}{N} = fxtal \times M}$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider and Nx output divider when S_LOAD transitions from LOW-to-HIGH. The M divide and Nx output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider and Nx output divider on each rising edge of S_CLOCK. The serial mode can be used to program the M and Nx bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1	S_Data, Shift Register Output
1	0	Output of M divider
1	1	FOUTA0 same frequency

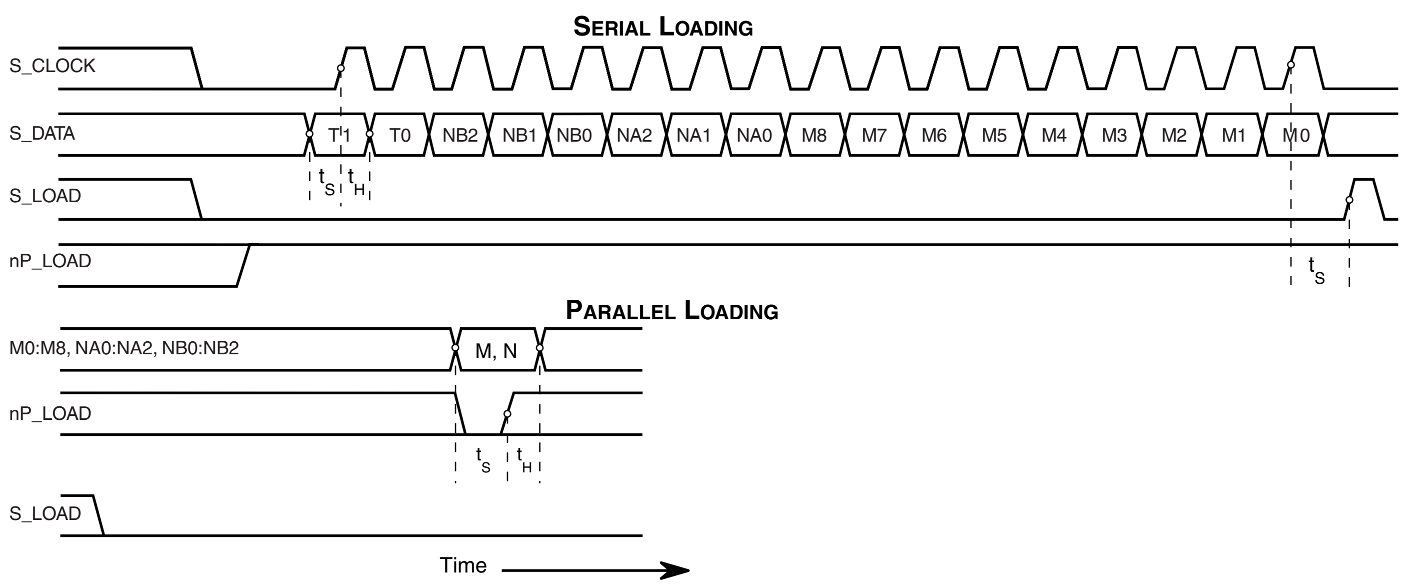


FIGURE 1. PARALLEL & SERIAL LOAD OPERATIONS

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 41, 42, 43, 44, 45, 47, 48	M8, M0, M1, M2, M3, M4, M6, M7	Input	Pulldown	M divider input. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS/LVTTL interface levels.
2, 3	NB0, NB1	Input	Pullup	Determines output divider value as defined in Table 3C, Function Table. LVCMOS/LVTTL interface levels.
4	NB2	Input	Pulldown	
5	OE_REF	Input	Pulldown	Output enable. Controls enabling and disabling of REF_CLK output. LVCMOS/LVTTL interface levels.
6	OE_A	Input	Pullup	Output enable. Controls enabling and disabling of FOUTA0, nFOUTA0 outputs. LVCMOS/LVTTL interface levels.
7	OE_B	Input	Pullup	Output enable. Controls enabling and disabling of FOUTB0, nFOUTB0 outputs. LVCMOS/LVTTL interface levels.
8, 14	V_{CC}	Power		Core supply pins.
9, 10	NA0, NA1	Input	Pullup	Determines output divider value as defined in Table 3C, Function Table. LVCMOS/LVTTL interface levels.
11	NA2	Input	Pulldown	
12, 24	V_{EE}	Power		Negative supply pins.
13	TEST	Output		Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS/LVTTL interface levels.
15, 16	FOUTA0, nFOUTA0	Output		Differential output for the synthesizer. LVPECL interface levels.
17	V_{CCO_A}	Power		Output supply pin for FOUTA0, nFOUTA0.
18, 19	FOUTB0, nFOUTB0	Output		Differential output for the synthesizer. LVPECL interface levels.
20	V_{CCO_B}	Power		Output supply pin for FOUTB0, nFOUTB0.
21	REF_CLK	Output		Reference clock output. LVCMOS/LVTTL interface levels.
22	V_{CCO_REF}	Power		Output supply pin for REF_CLK.
23	nc	Unused		No connect.
25	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, forces the internal dividers are reset causing the true outputs FOUTx to go low and the inverted outputs nFOUTx to go high. When logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not affect loaded M, N, and T values. LVCMOS/LVTTL interface levels.
26	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
27	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
28	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the dividers. LVCMOS/LVTTL interface levels.
29	V_{CCA}	Power		Analog supply pin.
30, 31	SEL0, SEL1	Input	Pulldown	Clock select inputs. LVCMOS/LVTTL interface levels.
32	TEST_CLK	Input	Pulldown	Test clock input. LVCMOS/LVTTL interface levels.
33, 34	XTAL_IN0, XTAL_OUT0	Input		Crystal oscillator interface. XTAL_IN0 is the input, XTAL_OUT0 is the output.
35, 36	XTAL_IN1, XTAL_OUT1	Input		Crystal oscillator interface. XTAL_IN1 is the input, XTAL_OUT1 is the output.

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TABLE 1. PIN DESCRIPTIONS, CONTINUED

Number	Name	Type		Description
37	CLK	Input	Pulldown	Non-inverting differential clock input.
38	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
39	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at NA2:NA0 and NB2:NB0 is loaded into the N output dividers. LVCMOS/LVTTL interface levels.
40	VCO_SEL	Input	Pullup	Determines whether synthesizer is in PLL or bypass mode. LVCMOS/LVTTL interface levels.
46	M5	Input	Pullup	M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
C_{PD}	Power Dissipation Capacitance	REF_CLK	V_{CC}, V_{CCA}, V_{CCO_REF} = 3.465V		TBD		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	REF_CLK		5	7	12	Ω

TABLE 3A. PARALLEL AND SERIAL MODE FUNCTION TABLE

Inputs							Conditions
MR	nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	
H	X	X	X	X	X	X	Reset. Forces outputs LOW.
L	L	Data	Data	X	X	X	Data on M and N inputs passed directly to the M divider and N output divider. TEST output forced LOW.
L	↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	H	X	X	↓	L	Data	M divider and N output divider values are latched.
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers.
L	H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

TABLE 3B. PROGRAMMABLE VCO FREQUENCY FUNCTION TABLE

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
575	23	0	0	0	0	1	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•
700	28	0	0	0	0	1	1	1	0	0
•	•	•	•	•	•	•	•	•	•	•
750	30	0	0	0	0	1	1	1	1	0

NOTE 1: These M divide values and the resulting frequencies correspond to crystal or TEST_CLK input frequency of 25MHz.

TABLE 3C. PROGRAMMABLE OUTPUT DIVIDER FUNCTION TABLE

Inputs			N Divider Value	Output Frequency (MHz)	
*NX2	*NX1	*NX0		Minimum	Maximum
0	0	0	1	560	750
0	0	1	2	280	375
0	1	0	3	186.66	250
0	1	1	4	140	187.5
1	0	0	5	112	150
1	0	1	6	93.33	125
1	1	0	8	70	93.75
1	1	1	16	35	46.875

*NOTE: X denotes Bank A or Bank B

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{CCO} + 0.5V
Outputs, I_O (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA}$ = 3.3V±5%, $V_{CCO\_A} = V_{CCO\_B}$ = 3.3V±5% OR 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	V_{CC}	V
V_{CCO_A}, V_{CCO_B}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
V_{CCO_REF}	Output Supply	REF_CLK	3.135	3.3	3.465	V
I_{EE}	Power Supply Current			185		mA
I_{CCA}	Analog Supply Current			20		mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V\pm5\%$, $V_{CCO\_A} = V_{CCO\_B} = V_{CCO\_REF} = 3.3V\pm5\%$, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IM}	Input Mid Voltage			V_{CC}/2 - 0.2V		V_{CC}/2 + 0.2V	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	TEST_CLK, MR, SEL[1:0], OE_REF, S_CLOCK, S_DATA, S_LOAD, nP_LOAD, Nx2, M1:M4, M6:M8	$V_{CC} = V_{IN} = 3.465V$			150	µA
		Nx0, Nx1, M5, OE_A, OE_B, VCO_SEL	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	TEST_CLK, MR, SEL[1:0], OE_REF, S_CLOCK, S_DATA, S_LOAD, nP_LOAD, Nx2, M1:M4, M6:M8	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		Nx0, Nx1, M5, OE_A, OE_B, VCO_SEL	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage	TEST; NOTE 1	$V_{CCO\_REF} = 3.3V\pm5\%$	2.6			V
		REF_CLK		V_{CCO_REF} - 0.3V		0.4	V
V_{OL}	Output Low Voltage	TEST; NOTE 1	$V_{CCO\_REF} = 3.3V\pm5\%$			0.5	V

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V\pm5\%$, $V_{CCO\_A} = V_{CCO\_B} = 3.3V\pm5\%$ OR $2.5V\pm5\%$, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	$V_{IN} = V_{CC} = 3.465V$			150	µA
		CLK	$V_{IN} = V_{CC} = 3.465V$			150	µA
I_{IL}	Input Low Current	nCLK	$V_{IN} = 0V$, $V_{CC} = 3.465V$	-150			µA
		CLK	$V_{IN} = 0V$, $V_{CC} = 3.465V$	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{CC} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V\pm5\%$, $V_{CCO\_A} = V_{CCO\_B} = 3.3V\pm5\%$ OR $2.5V\pm5\%$, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO_A}, V_{CCO_B} - 2V.

TABLE 5. INPUT FREQUENCY CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V±5\%$, $V_{CCO\_A} = V_{CCO\_B} = 3.3V±5\%$ OR 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	XTAL_IN0/XTAL_OUT0, XTAL_IN1/XTAL_OUT1		12		40	MHz
		CLK/nCLK, TEST_CLK		12		TBD	MHz
		S_CLOCK				50	MHz
t_R/t_F	Input Rise/Fall Time	TEST_CLK			TBD		ns
		S_LOAD, S_DATA, S_CLOCK			TBD		ns

NOTE: For the input crystal, CLK/nCLK and TEST_CLK frequency range, the M value must be set for the VCO to operate within the 560MHz to 750MHz range. Using the minimum input frequency of 12MHz, valid values of M are 47 ≤ M ≤ 62. Using the maximum frequency of 40MHz, valid values of M are 14 ≤ M ≤ 18.

TABLE 6. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 7A. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO\_A} = V_{CCO\_B} = 3.3V±5\%$, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency			35		750	MHz
*t*jit(Ø)	Phase Jitter, RMS (Random); NOTE 1, 2		333.33MHz, Integration Range: 12kHz - 20MHz		0.80		ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 3, 4				51		ps
*t*sk(o)	Output Skew; NOTE 2, 4, 5		Measured @ the same Output Frequency		50		ps
t_R / t_F	Output Rise/Fall Time	LVPECL Outputs	20% to 80%	200		700	ps
		REF_CLK					
t_S	Setup Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
t_H	Hold Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
odc	Output Duty Cycle				50		%
t_{LOCK}	PLL Lock Time					1	ms

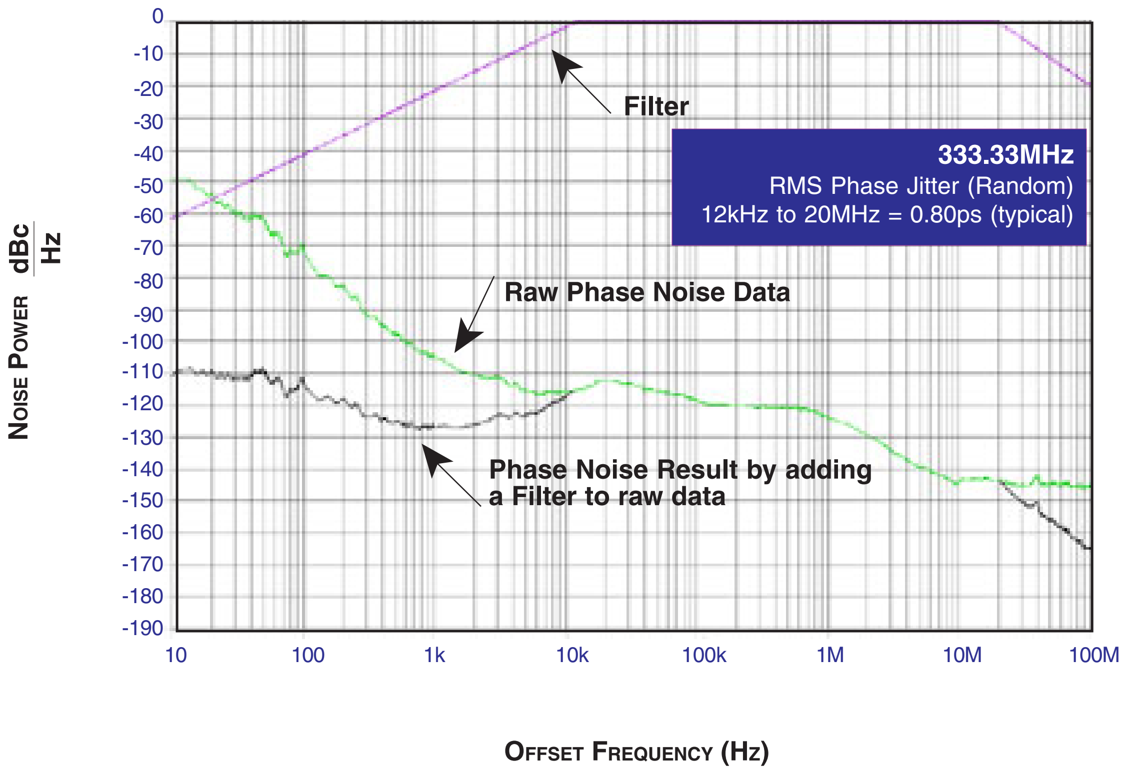
See Parameter Measurement Information section.
NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: Characterized with REF_CLK output disabled.
NOTE 3: Jitter perforance using XTAL inputs.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.

TABLE 7B. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V±5\%$, $V_{CCO\_A} = V_{CCO\_B} = 2.5V±5\%$, $T_A = 0°C$ TO $70°C$

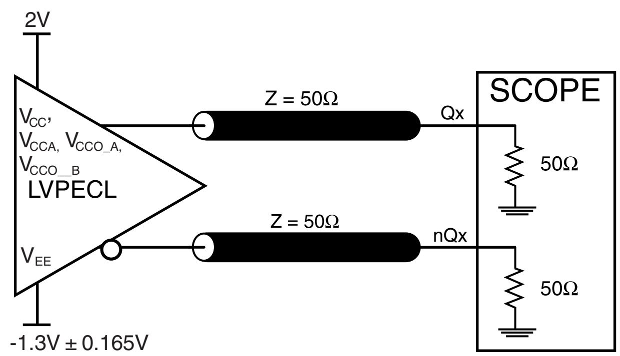
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency			35		750	MHz
*t*jit(Ø)	Phase Jitter, RMS (Random); NOTE 1, 2		333.33MHz, Integration Range: 12kHz - 20MHz		TBD		ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 3, 4				52		ps
*t*sk(o)	Output Skew; NOTE 2, 4, 5		Measured @ the same Output Frequency		50		ps
t_R / t_F	Output Rise/Fall Time	LVPECL Outputs	20% to 80%	200		700	ps
		REF_CLK					
t_S	Setup Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
t_H	Hold Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
odc	Output Duty Cycle				50		%
t_{LOCK}	PLL Lock Time					1	ms

For notes, see Table 7A above.

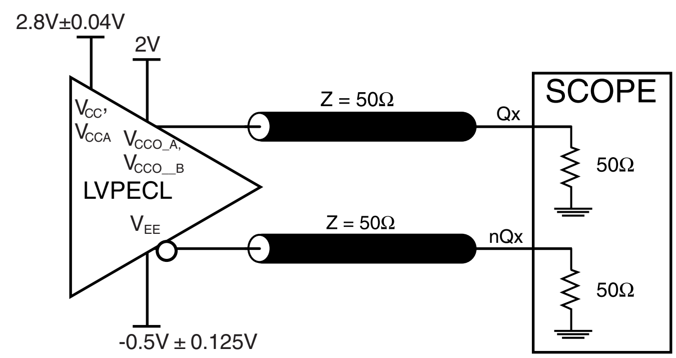
Typical Phase Noise at 333.33MHz



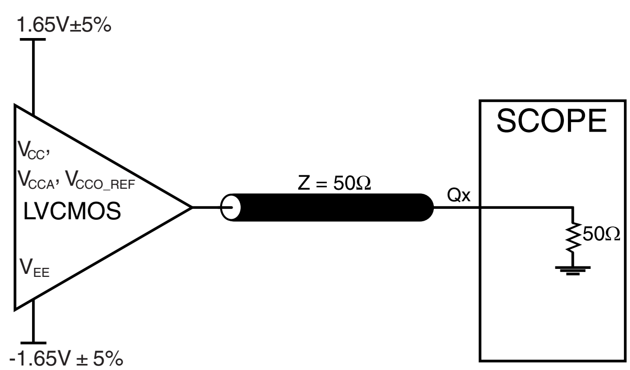
Parameter Measurement Information



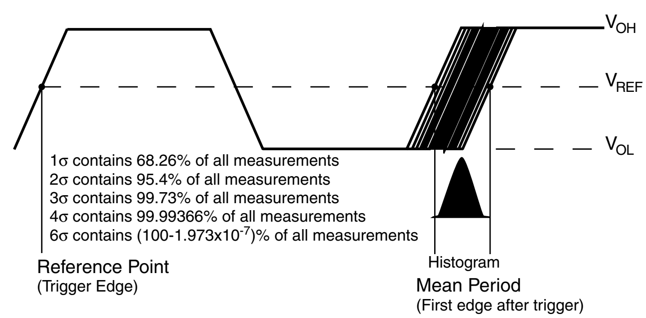
3.3V Core/3.3V Output Load AC Test Circuit FOUTA0/nFOUTA0, FOUTB0/nFOUTB0



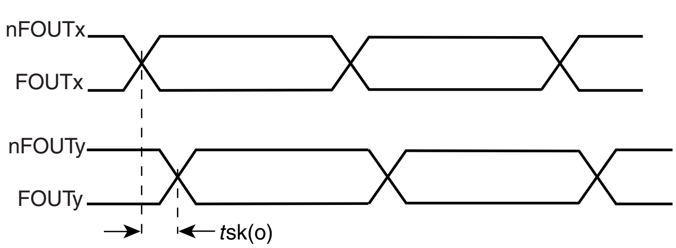
3.3V Core/2.5V Output Load AC Test Circuit FOUTA0/nFOUTA0, FOUTB0/nFOUTB0



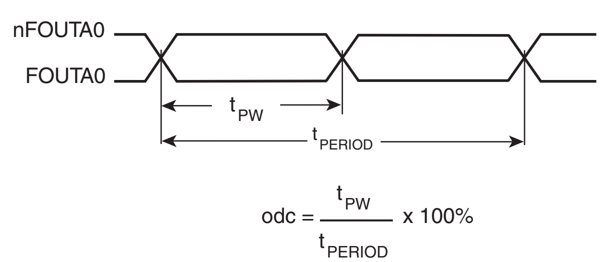
3.3VCore/3.3V REF_CLK Output Load AC Test Circuit



Period Jitter

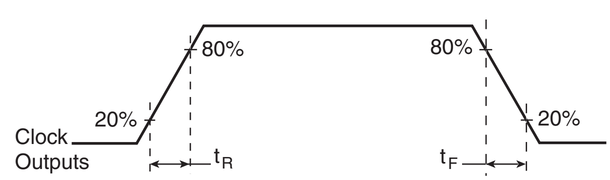


Output Skew



Output Duty Cycle/Output Pulse Width/Period

LVPECL Output Rise/Fall Time



LVCMOS Output Rise/Fall Time

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843034 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO_x} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

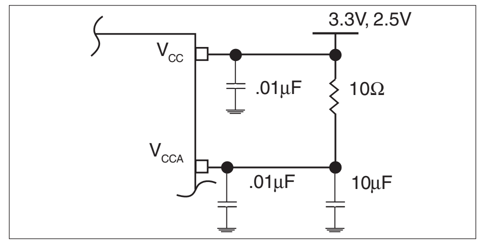


Figure 2. Power Supply Filtering

Wiring the Differential Input to Accept Single Ended LVCMOS/LVTTL Levels

Figure 3 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{cc}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{cc} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

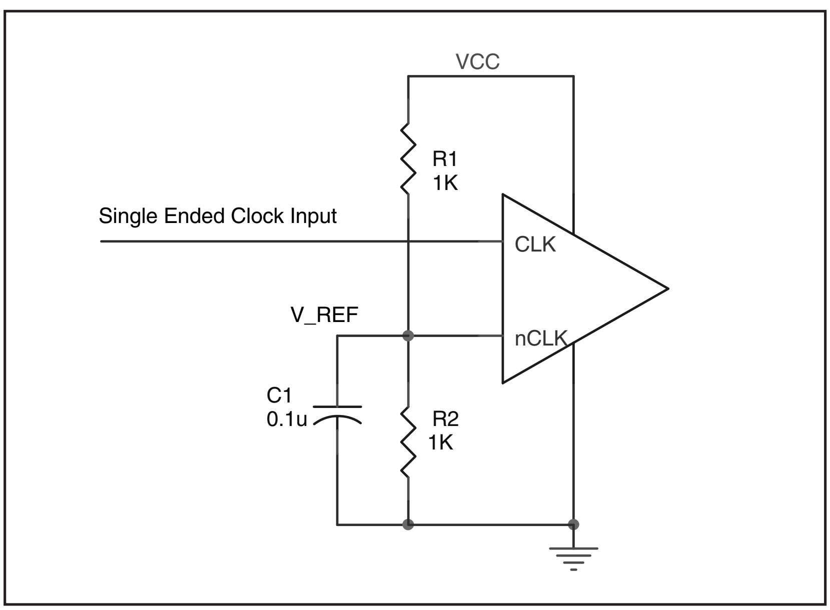


Figure 3. Single Ended Signal Driving Differential Input

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 4A to 4D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A,* the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

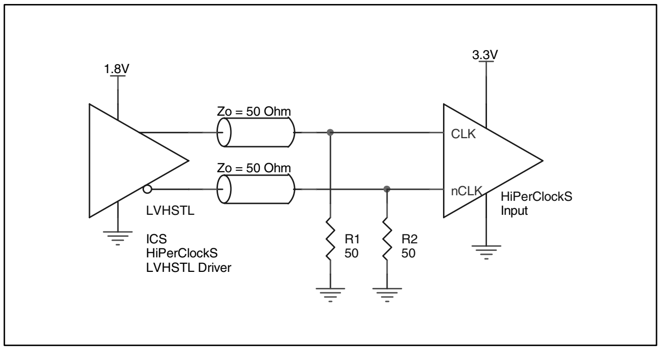


FIGURE 4A. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY IDT HIPERCLOCKS LVHSTL DRIVER

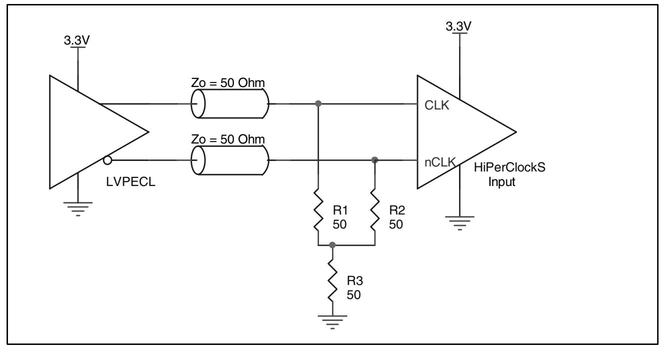


FIGURE 4B. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

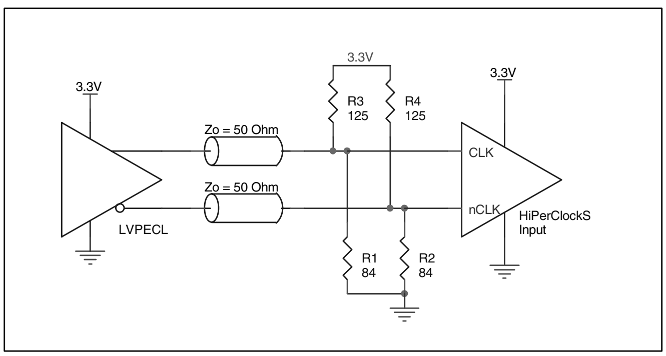


FIGURE 4C. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

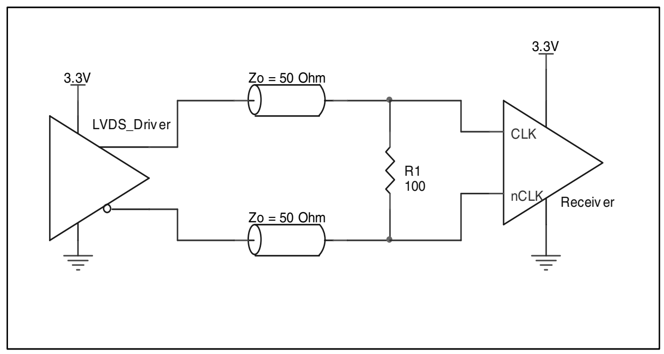


FIGURE 4D. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

TEST_CLK INPUT:

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST_CLK to ground.

SELECT PINS:

All select pins have internal pull-ups and pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The ICS843034 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 5* below were determined using a 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

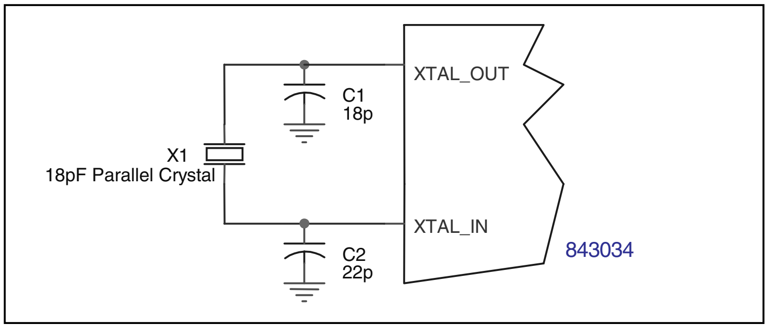


Figure 5. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 6*. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

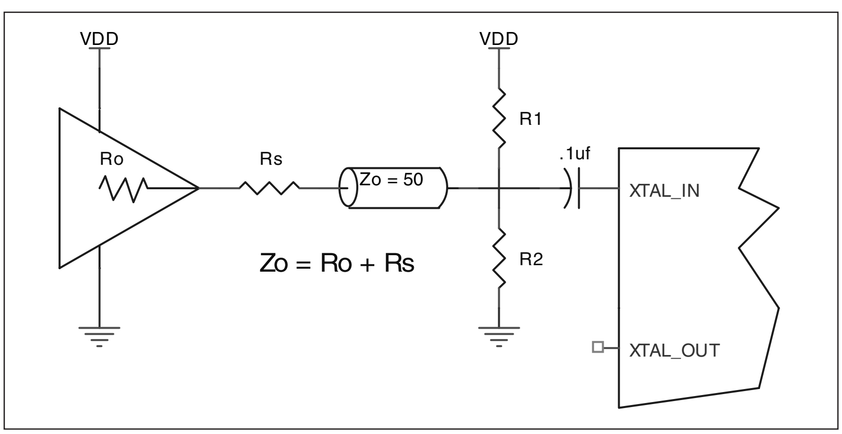


Figure 6. General Diagram for LVCMOS Driver to XTAL Input Interface

Termination for 3.3V LVPECL Output

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUTx and nFOUTx are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 7A and 7B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

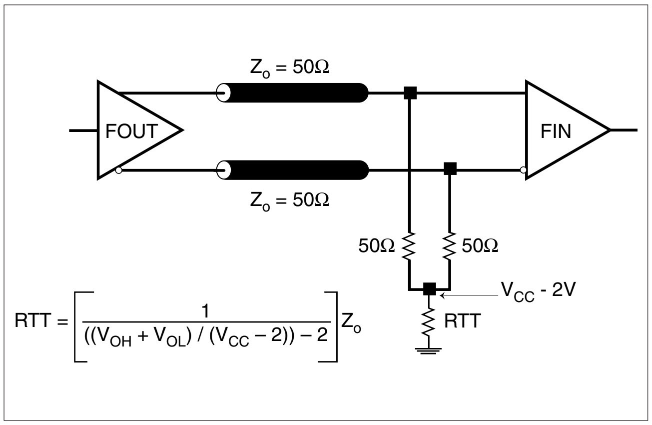


Figure 7A. LVPECL Output Termination

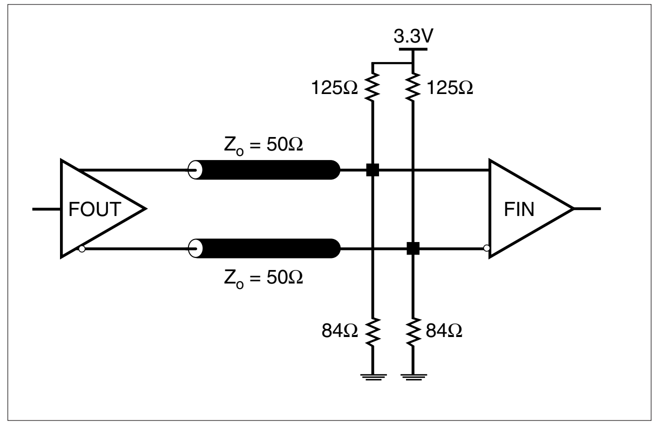


Figure 7B. LVPECL Output Termination

Termination for 2.5V LVPECL Output

Figure 8A and *Figure 8B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in *Figure 8B* can be eliminated and the termination is shown in *Figure 8C.*

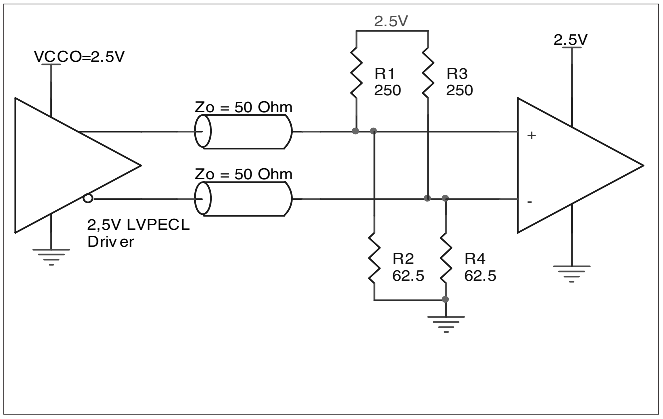


Figure 8A. 2.5V LVPECL Driver Termination Example

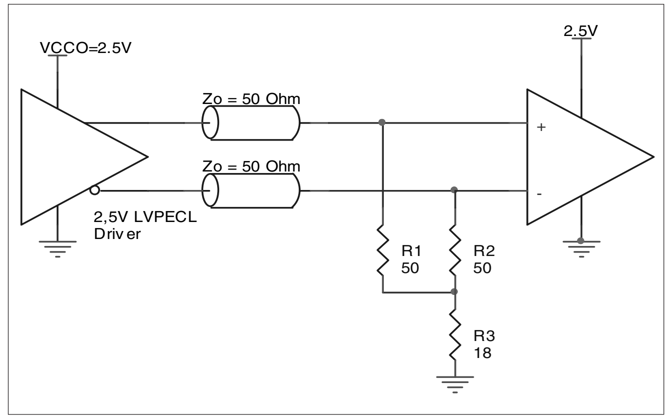


Figure 8B. 2.5V LVPECL Driver Termination Example

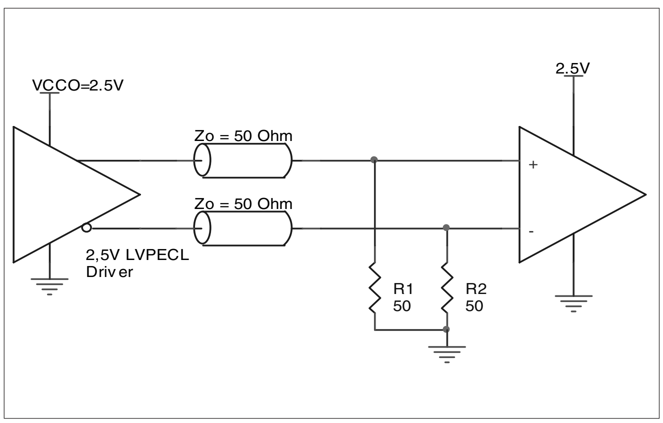


Figure 8C. 2.5V LVPECL Termination Example

Application Schematic Example

*Figure 9*shows a schematic example of using an ICS843034. In this example, the CLK/nCLK input is driven by a 3.3V LVPECL driver. The data sheet also shows the CLK/nCLK input driven by various types of drivers. The crystal inputs are parallel resonant crystal with load capacitor CL=18pF. The frequency fine tuning capacitors C1 and C2 are 22pF. This schematic example shows hardwired logic control input handling. The logic inputs can also be driven by 3.3V LVCMOS drivers. It is recommended to have one decouple capacitor per power pin. In general, the decoupling capacitor values are ranged from 0.01uF to 0.1uF. Each decoupling capacitor should be located as close as possible to the power pin. The low pass filter R9, C11 and C16 for clean analog supply should also be located as close to the VCCA pin as possible. Only two examples of 3.3V LVPECL termination are shown in this schematic example. Additional LVPECL terminations can be found in the LVPECL Termination Application Note. The data sheet also shows 2.5V LVPECL terminations. The REF_CLK is LVCMOS driver with 7Ω output impedance. Series termination for REF_CLK is shown in the example. Additional LVCMOS termination can be found in the LVCMOS Application Note. If the REF_CLK is not used, it is recommended to disable this output by setting REF_OE to logic low. To disable REF_CLK, REF_OE pin can be left floating (default logic low by internal 51K pull down) or pull down using an external 1kΩ resistor.

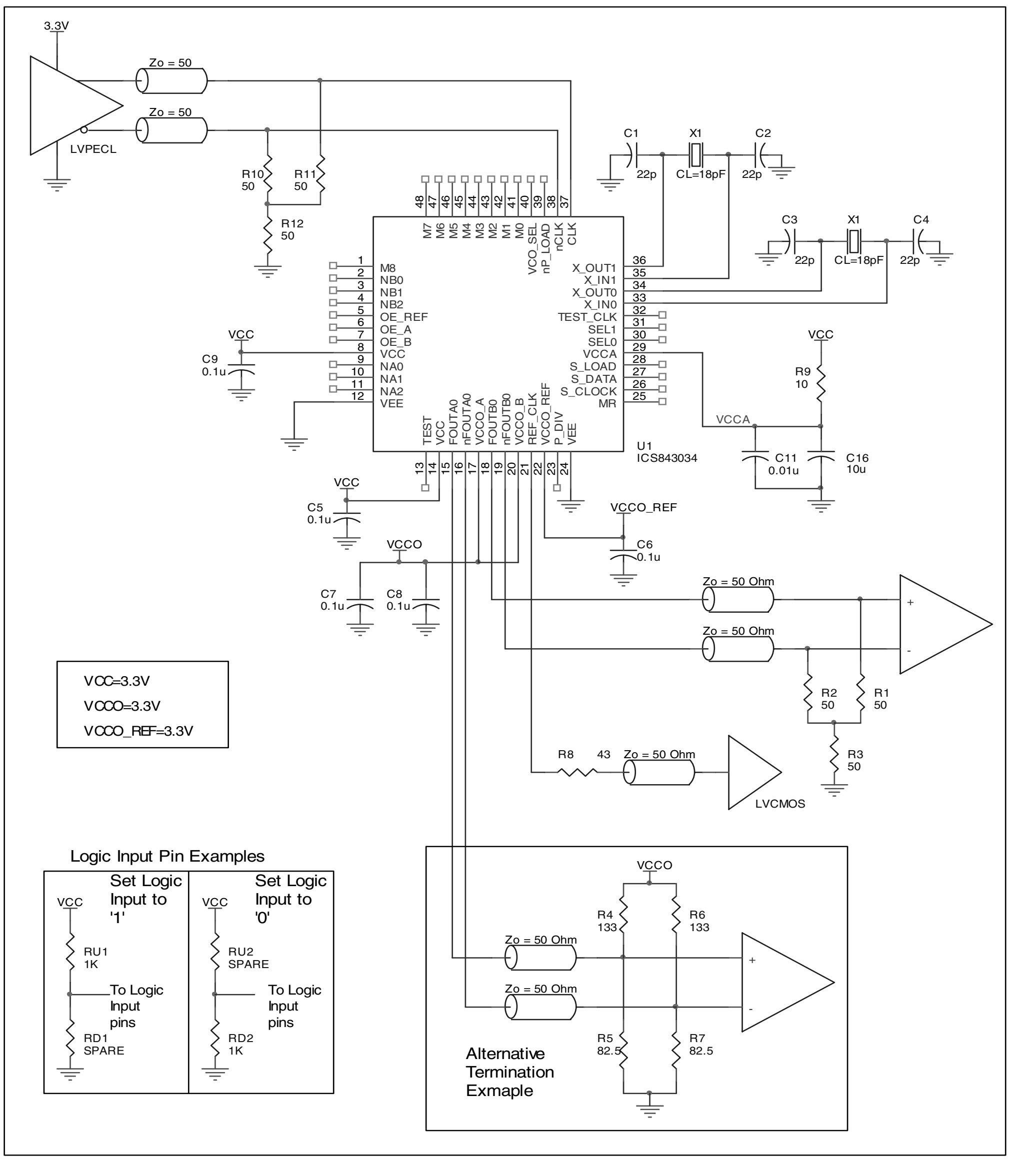


Figure 9. ICS843034 Application Schematic Example

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843034. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843034 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 185mA = **641mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 641mW + 60mW = **701mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.701W * 42.1°C/W = 99.5°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 8. THERMAL RESISTANCE θ_{JA} FOR 48-PIN LQFP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 10.*

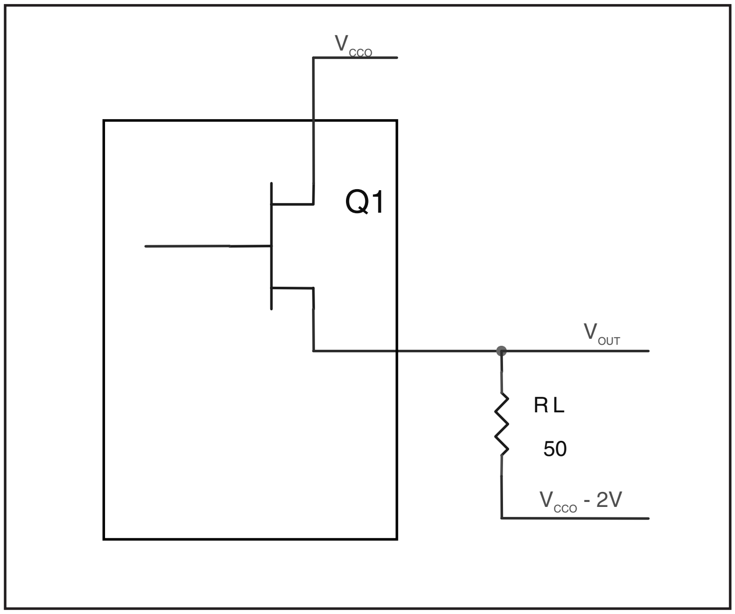


FIGURE 10. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination
voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 9. θ_{JA} vs. Air Flow Table for 48 Lead LQFP

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for ICS843034 is: 11,748

Package Outline - Y Suffix for 48 Lead LQFP

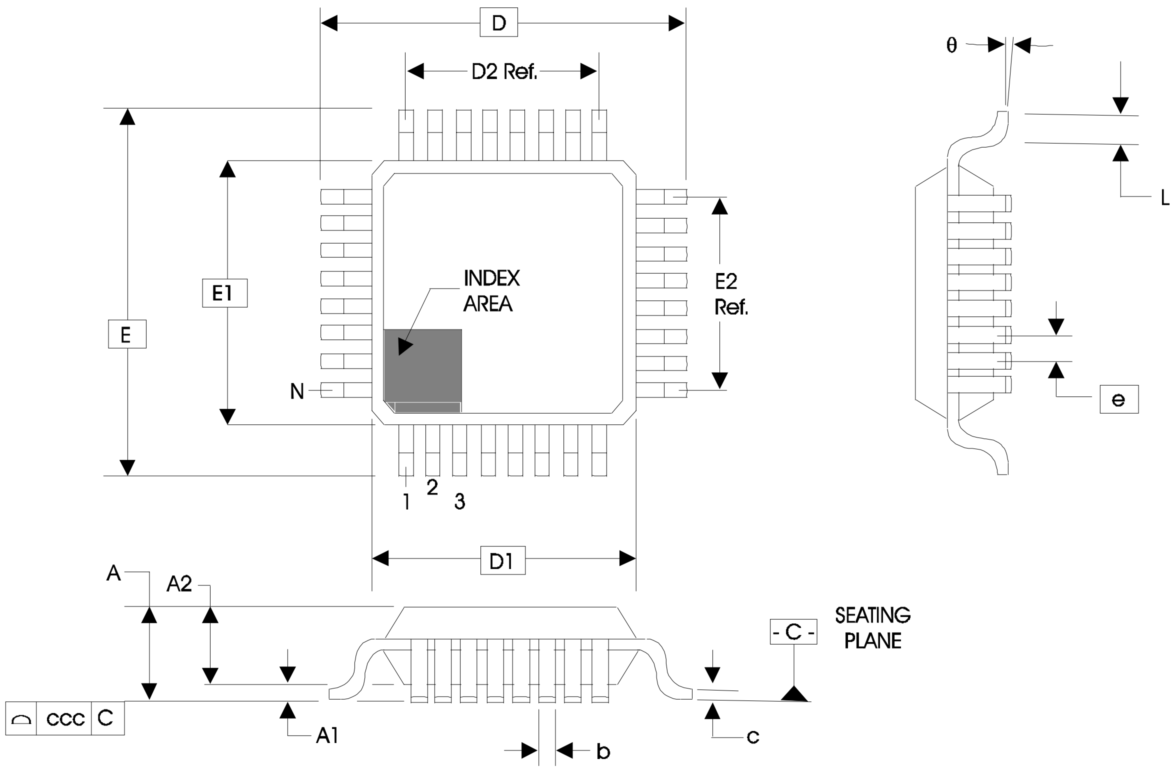


Table 10. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	**BBC**		
	MINIMUM	**NOMINAL**	**MAXIMUM**
N	48		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.50 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.50 Ref.		
e	0.50 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843034AY	ICS843034AY	48 Lead LQFP	tray	0°C to 70°C
ICS843034AYT	ICS843034AY	48 Lead LQFP	1000 tape & reel	0°C to 70°C
ICS843034AYLF	ICS843034AYL	48 Lead "Lead-Free" LQFP	tray	0°C to 70°C
ICS843034AYLFT	ICS843034AYL	48 Lead "Lead-Free" LQFP	1000 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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