*PRELIMINARY*
*CUSTOMER PROCUREMENT SPECIFICATION*

# Z86L88/L81/L86

## INFRARED REMOTE CONTROLLERS

## FEATURES

| Part | ROM (KB) | RAM* (Bytes) | I/O | 28-pin DIP, SOIC |
|---|---|---|---|---|
| Z86L88 | 16 | 237 | 24 | X |
| Z86L81 | 24 | 237 | 24 | X |
| Z86L86 | 32 | 237 | 24 | X |

*General-Purpose

- 2.0V to 3.9V Operating Range (8.0 MHz)
- Three Standby Modes (Typical)
  - STOP - 2 µA
  - HALT - 0.8 mA
  - Low-Voltage Standby (< VLV)
- Expanded Register File Control Registers
- Special Architecture to Automate Both Generation and Reception of Complex Pulses or Signals:
  - One Programmable 8-Bit Counter/Timer with Two Capture Registers
  - One Programmable 16-Bit Counter/Timer with One Capture Register
  - Programmable Input Glitch Filter for Pulse Reception
- Five Priority Interrupts
- Low-Voltage Detection and Protection
- Watch-Dog Timer (WDT)/Power-On Reset (POR)
- Two Independent Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive
- Mask Selectable 200 kOhms Pull-Ups on Ports 0, 2, 3
  - All Eight Port 2 Bits at One Time or Not
  - Pull-Ups Automatically Disabled Upon Selecting Individual Pins as Outputs
- Maskable 0.4 $V_{DD}$ Single Trip Point Inputs on P00 Through P03 for Direct Mouse/Trackball IR Sensor Interface
- Low-Voltage Standby Mode

## GENERAL DESCRIPTION

The Z86L8X family of infrared (IR) consumer controller processors are ROM-based members of the Z8® single-chip microcontroller family offering a unique register-to-register architecture that avoids accumulator bottlenecks and offers fast execution of code.

Zilog's CMOS microcontrollers feature fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and easy hardware/software system expansion along with low-cost and low-power consumption.

The Z86L8X family architecture is based on Zilog's 8-bit microcontroller core with an Expanded Register File (ERF) to allow access to register mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The Z86L8X offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery operated hand-held applications.

## GENERAL DESCRIPTION (Continued)

For applications demanding powerful I/O capabilities, the Z86L8X fulfills this with two package options in which 24 pins of dedicated input and output are grouped into three ports. Each port consists of eight lines and is configurable under software control to provide timing, status signals, and parallel I/O.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File, and Expanded Register File. (ERF). The Register File is composed of 256 bytes of RAM. It includes four I/O port registers, 15 control and status registers, and the rest are general purpose registers. The ERF consists of two register groups (Banks D and F).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86L8X offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes, and two on-board comparators to process analog signals with separate reference voltages (Figure 2).

**Notes:**
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

| Connection | Circuit | Device |
|---|---|---|
| Power | $V_{CC}$ | $V_{DD}$ |
| Ground | GND | $V_{SS}$ |

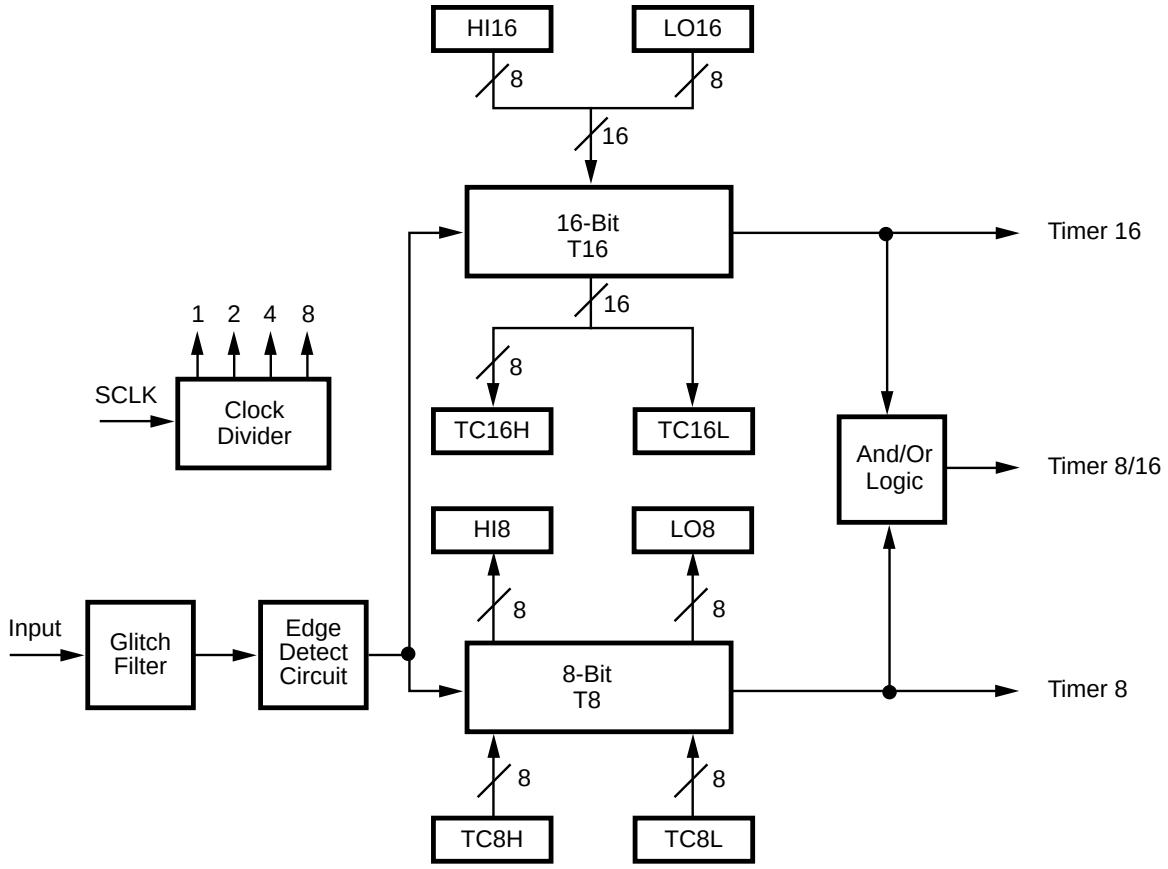


**Figure 1. Counter/Timer Block Diagram**

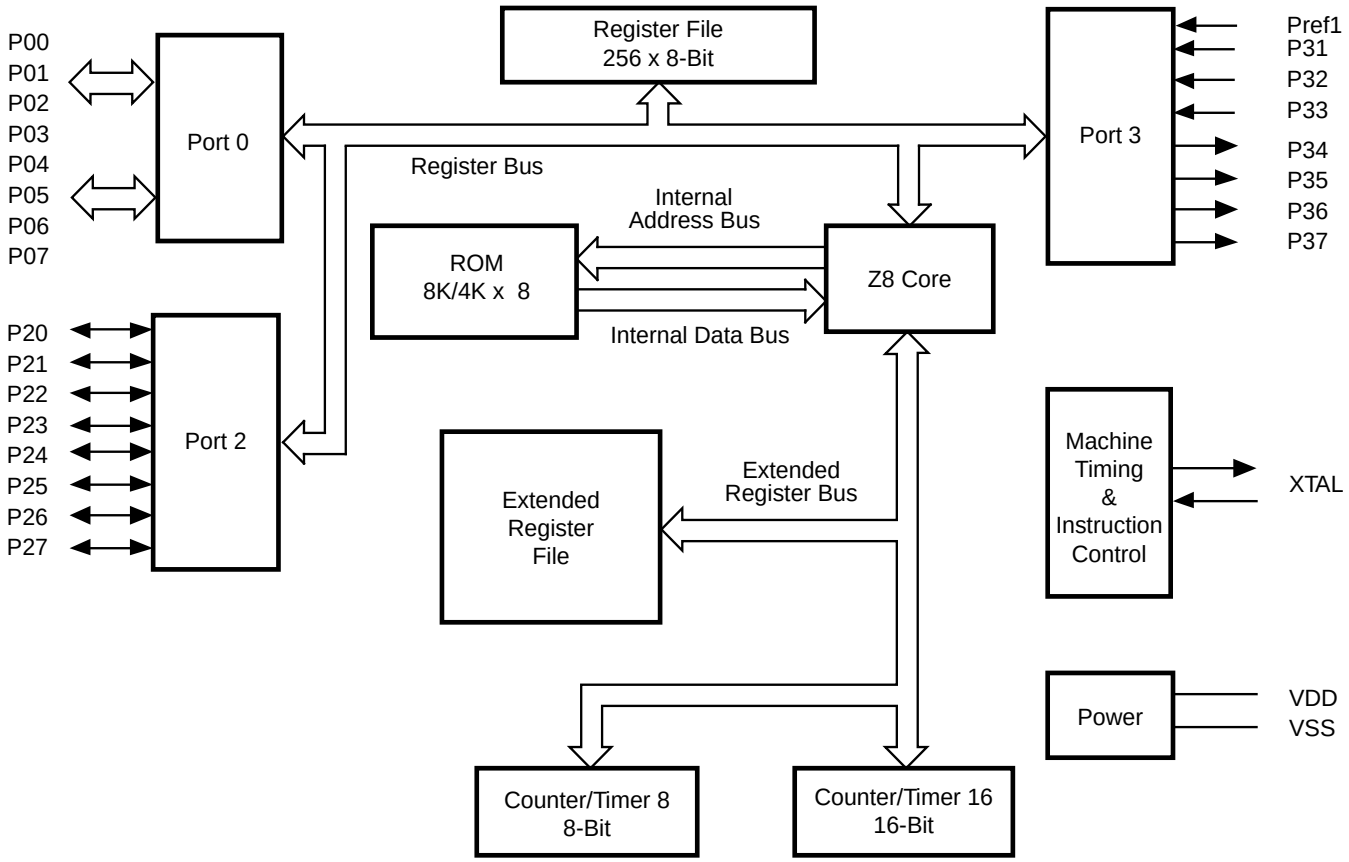


**Figure 2. Functional Block Diagram**

## PIN DESCRIPTION

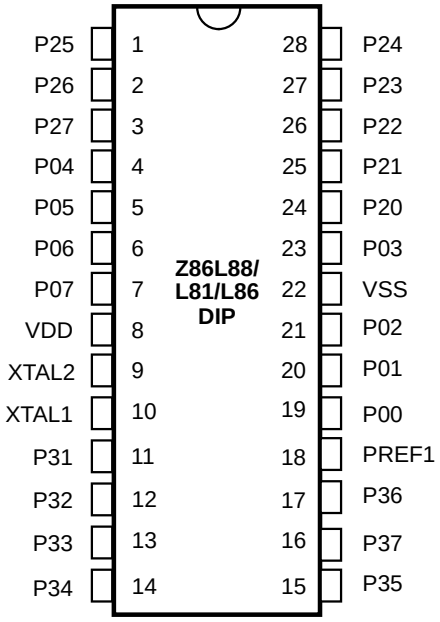


**Figure 3. 28-Pin DIP Pin Assignments**

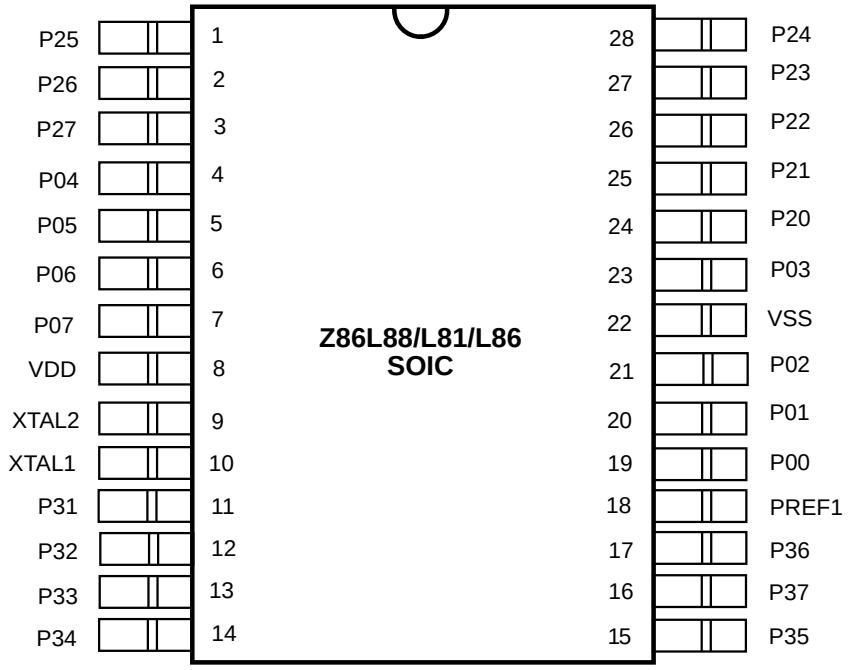


**Figure 4. 28-Pin SOIC Pin Assignments**

## PIN DESCRIPTION (Continued)

**Table 1. Pin Identification**

| 28-Pin DIP & SOIC # | Symbol | Direction | Description |
|---|---|---|---|
| 1 | P25 | Input/Output | |
| 2 | P26 | Input/Output | |
| 3 | P27 | Input/Output | |
| 4 | P04 | Input/Output | Port 0 can be configured as a mouse/trackball input. |
| 5 | P05 | Input/Output | |
| 6 | P06 | Input/Output | |
| 7 | P07 | Input/Output | |
| 8 | $V_{DD}$ | | Power Supply |
| 9 | XTAL2 | Output | Crystal, Oscillator Clock |
| 10 | XTAL1 | Input | Crystal, Oscillator Clock |
| 11 | P31 | Input | IRQ2/Modulator Input/Comparator 1 Input |
| 12 | P32 | Input | IRQ0/Comparator 2 Input |
| 13 | P33 | Input | IRQ1/Comparator 2 Ref |
| 14 | P34 | Output | T8 Output |
| 15 | P35 | Output | T16 Output |
| 16 | P37 | Output | |
| 17 | P36 | Output | T8/T16 Output |
| 18 | Pref1 | Input | Analog Ref Input (Comparator 1) |
| 19 | P00 | Input/Output | Port 0 is Nibble Programmable. |
| 20 | P01 | Input/Output | Port 0 can be configured as A15-A8 external program. |
| 21 | P02 | Input/Output | |
| 22 | $V_{SS}$ | | Ground |
| 23 | P03 | Output | ROM Address Bus |
| 24 | P20 | Input/Output | Port 2 pins are individually configurable as input or output. |
| 25 | P21 | Input/Output | |
| 26 | P22 | Input/Output | |
| 27 | P23 | Input/Output | |
| 28 | P24 | Input/Output | |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage (*) | –0.3 | +7.0 | V |
| $T_{STG}$ | Storage Temp. | –65° | +150° | C |
| $T_A$ | Oper. Ambient Temp. | | † | C |

**Notes:**
* Voltage on all pins with respect to GND.
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 5).

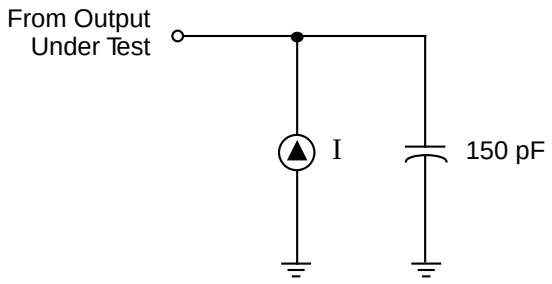


**Figure 5. Test Load Diagram**

## CAPACITANCE

$T_A$ = 25°C, $V_{CC}$ = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

| Parameter | Max |
|---|---|
| Input capacitance | 12 pF |
| Output capacitance | 12 pF |
| I/O capacitance | 12 pF |

## DC CHARACTERISTICS

| Sym | Parameter | $V_{CC}$ | $T_A$ = 0°C to +70°C Min | Max | Typ @ 25°C | Units | Conditions | Notes [3] |
|---|---|---|---|---|---|---|---|---|
| | Max Input Voltage | 2.0V | | 7 | | V | $I_{IN}$ <250µA | |
| | | 3.9V | | 7 | | V | $I_{IN}$ <250µA | |
| $V_{CH}$ | Clock Input High Voltage | 2.0V | $0.9V_{CC}$ | $V_{CC}$+0.3 | | V | Driven by External Clock Generator | |
| | | 3.9V | $0.9\,V_{CC}$ | $V_{CC}$+0.3 | | V | Driven by External Clock Generator | |
| $V_{CL}$ | Clock Input Low Voltage | 2.0V | $V_{SS}$–0.3 | $0.2V_{CC}$ | | V | Driven by External Clock Generator | |
| | | 3.9V | $V_{SS}$–0.3 | $0.2V_{CC}$ | | V | Driven by External Clock Generator | |
| $V_{IH}$ | Input High Voltage | 2.0V | $0.7V_{CC}$ | $V_{CC}$+0.3 | 1.3 | V | | |
| | | 3.9V | $0.7V_{CC}$ | $V_{CC}$+0.3 | 2.5 | V | | |
| $V_{IL}$ | Input Low Voltage | 2.0V | $V_{SS}$–0.3 | $0.2V_{CC}$ | 0.5 | V | | |
| | | 3.9V | $V_{SS}$–0.3 | $0.2V_{CC}$ | 0.9 | V | | |
| $V_{OH1}$ | Output High Voltage | 2.0V | $V_{CC}$–0.4 | | 1.7 | V | $I_{OH}$=–0.5mA | † |
| | | 3.9V | $V_{CC}$–0.4 | | 3.7 | V | $I_{OH}$=–0.5mA | |
| $V_{OH2}$ | Output High Voltage | 2.0V | $V_{CC}$–0.7 | | 1.5 | V | $I_{OH}$=–7mA | [10] |
| | (P36, P37) | 3.9V | $V_{CC}$–0.7 | | 3.5 | V | $I_{OH}$,=–7mA | [10] |
| $V_{OL1}$ | Output Low Voltage | 2.0V | | 0.4 | 0.1 | V | $I_{OL}$=1.0 mA | * |
| | | 3.9V | | 0.4 | 0.2 | V | $I_{OL}$=4.0 mA | |
| $V_{OL2}$ | Output Low Voltage | 2.0V | | 0.8 | 0.6 | V | $I_{OL}$=5.0mA | * |
| | | 3.9V | | 0.8 | 0.3 | V | $I_{OL}$=7.0mA | |
| $V_{OL2}$ | Output Low Voltage | 2.0V | | 0.8 | 0.3 | V | $I_{OL}$=10mA | [9] |
| | (P00, P01, P36, P37) | 3.9V | | 0.8 | 0.2 | V | $I_{OL}$=10mA | [9] |
| $V_{OFFSET}$ | Comparator Input Offset Voltage | 2.0V | | 25 | 10 | mV | | |
| | | 3.9V | | 25 | 10 | mV | | |
| $I_{IL}$ | Input Leakage | 2.0V | –1 | 1 | <1 | µA | $V_{IN}$=0V,$V_{CC}$ | |
| | | 3.9V | –1 | 1 | <1 | µA | $V_{IN}$=0V,$V_{CC}$ | |
| $I_{OL}$ | Output Leakage | 2.0V | –1 | 1 | <1 | µA | $V_{IN}$=0V,$V_{CC}$ | |
| | | 3.9V | –1 | 1 | <1 | µA | $V_{IN}$=0V,$V_{CC}$ | |
| $I_{IR}$ | Reset Input Current | 2.0V | | –45 | –20 | µA | | |
| | | 3.9V | | –55 | –30 | µA | | |
| $I_{CC}$ | Supply Current | 2.0V | | 10 | 4 | mA | @8.0MHz | [4,5] |
| | | 3.9V | | 15 | 10 | mA | @8.0MHz | [4,5] |
| | | 2.0V | | 100 | 10 | µA | @32kHz | [4,5,11] |
| | | 3.9V | | 300 | 10 | µA | @32kHz | [4,5,11] |

## DC CHARACTERISTICS (Continued)

| Sym | Parameter | $V_{CC}$ | $T_A$ = 0°C to +70°C Min | Max | Typ @ 25°C | Units | Conditions | Notes [3] |
|---|---|---|---|---|---|---|---|---|
| $I_{CC1}$ | Standby Current (WDT Off) | 2.0V | | 3 | 1 | mA | HALT Mode $V_{IN}$=0V, $V_{CC}$ @8.0MHz | [4,5] |
| | | 3.9V | | 5 | 4 | mA | HALT Mode $V_{IN}$=0V, $V_{CC}$ @8.0MHz | [4,5] |
| | | 2.0V | | 2 | 0.8 | mA | Clock Divide-by-16 @8.0MHz | [4,5] |
| | | 3.9V | | 4 | 2.5 | mA | Clock Divide-by-16 @8.0MHz | [4,5] |
| $I_{CC2}$ | Standby Current | 2.0V | | 8 | 2 | µA | STOP Mode $V_{IN}$=0V, $V_{CC}$ WDT is not Running | [6,8] |
| | | 3.9V | | 10 | 3 | µA | STOP Mode $V_{IN}$=0V, $V_{CC}$ WDT is not Running | [6,8] |
| | | 2.0V | | 500 | 310 | µA | STOP Mode $V_{IN}$=0V, $V_{CC}$ WDT is Running | [6,8] |
| | | 3.9V | | 800 | 600 | µA | STOP Mode $V_{IN}$=0V, $V_{CC}$ WDT is Running | [6,8] |
| $T_{POR}$ | Power-On Reset | 2.0V | 7.5 | 75 | 13 | ms | | |
| | | 3.9V | 2.5 | 20 | 7 | ms | | |
| $V_{LV}$ | $V_{CC}$ Low Voltage Protection | | | 2.15 | 1.7 | V | 8MHz max Ext. CLK Freq. | [7] |

**Notes:**

[1] $I_{cc1}$

| | Typ | Max | Unit | Frequency |
|---|---|---|---|---|
| Crystal/Resonator | 4.0 mA | 5 | mA | 8.0 MHz |
| External Clock Drive | 0.3 mA | 5 | mA | 8.0 MHz |

[2] GND = 0V
[3] 2.0V to 3.9V
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1 = CL2 = 100 pF
[6] Same as note [4] except inputs at $V_{CC}$.
[7] The $V_{LV}$ increases as the temperature decreases.
[8] Oscillator stopped.
[9] Two outputs at a time, independent to other outputs.
[10] One at a time.
[11] 32 kHz clock driver input.
† All outputs excluding P36, P37.
* All outputs excluding P36, P37, P00, and P01.

## AC CHARACTERISTICS

Additional Timing Diagram

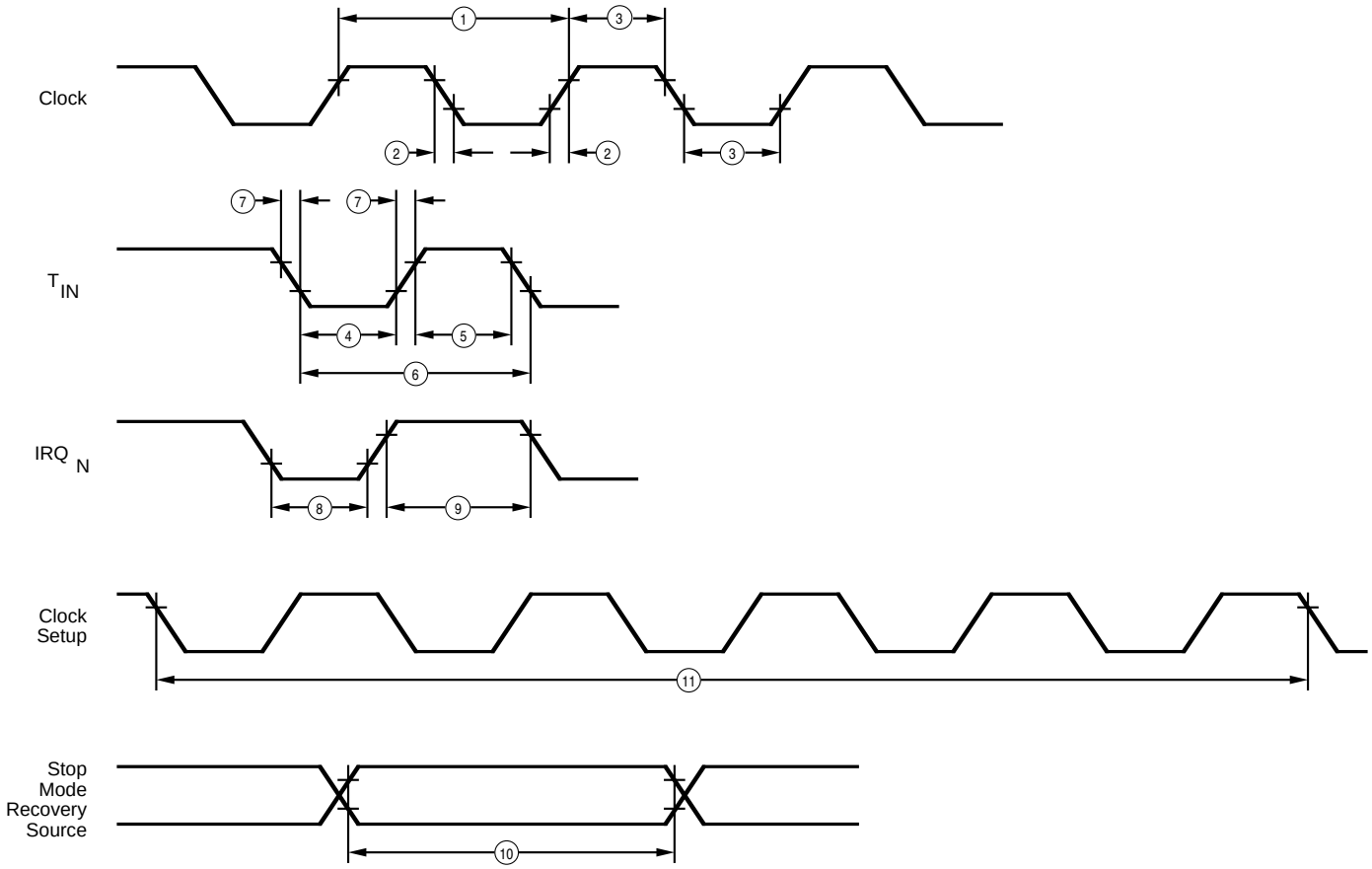


**Figure 6. Additional Timing**

## AC CHARACTERISTICS

Additional Timing Table

| No | Symbol | Parameter | | $V_{CC}$ Note [3] | $T_A$ = 0°C to +70°C 8.0MHz Min | Max | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| 1 | TpC | Input Clock Period | | 2.0V | 121 | DC | ns | [1] |
| | | | | 3.9V | 121 | DC | ns | [1] |
| 2 | TrC,TfC | Clock Input Rise | | 2.0V | | 25 | ns | [1] |
| | | and Fall Times | | 3.9V | | 25 | ns | [1] |
| 3 | TwC | Input Clock Width | | 2.0V | 37 | | ns | [1] |
| | | | | 3.9V | 37 | | ns | [1] |
| 4 | TwTinL | Timer Input | | 2.0V | 100 | | ns | [1] |
| | | Low Width | | 3.9V | 70 | | ns | [1] |
| 5 | TwTinH | Timer Input | | 2.0V | 3TpC | | | [1] |
| | | High Width | | 3.9V | 3TpC | | | [1] |
| 6 | TpTin | Timer Input Period | | 2.0V | 8TpC | | | [1] |
| | | | | 3.9V | 8TpC | | | [1] |
| 7 | TrTin,TfTin | Timer Input Rise | | 2.0V | | 100 | ns | [1] |
| | | and Fall Timers | | 3.9V | | 100 | ns | [1] |
| 8A | TwIL | Interrupt Request | | 2.0V | 100 | | ns | [1,2] |
| | | Low Time | | 3.9V | 70 | | ns | [1,2] |
| 8B | TwIL | Int. Request | | 2.0V | 3TpC | | | [1,3] |
| | | Low Time | | 3.9V | 3TpC | | | [1,3] |
| 9 | TwIH | Interrupt Request | | 2.0V | 3TpC | | | [1,2] |
| | | Input High Time | | 3.9V | 3TpC | | | [1,2] |
| 10 | Twsm | Stop-Mode Recovery | | 2.0V | 12 | | ns | [8] |
| | | Width Spec | | 3.9V | 12 | | ns | [8] |
| | | | | 2.0V | 5TpC | | | [7] |
| | | | | 3.9V | 5TpC | | | [7] |
| 11 | Tost | Oscillator | | 2.0V | | 5TpC | | [4] |
| | | Start-up Time | | 3.9V | | 5TpC | | [4] |
| 12 | Twdt | Watch-Dog Timer | (5ms) | 2.0V | 12 | 75 | ms | D0=0 [5] |
| | | Delay Time | | 3.9V | 5 | 20 | ms | D1=0 [5] |
| | | | (15ms) | 2.0V | 25 | 150 | ms | D0=1 [5] |
| | | | | 3.9V | 10 | 40 | ms | D1=0 [5] |
| | | | (25ms) | 2.0V | 50 | 300 | ms | D0=0 [5] |
| | | | | 3.9V | 25 | 80 | ms | D1=1 [5] |
| | | | (100ms) | 2.0V | 225 | 1200 | ms | D0=1 [5] |
| | | | | 3.9V | 100 | 320 | ms | D1=1 [5] |

**Notes:**

[1] Timing Reference uses 0.9 $V_{CC}$ for a logic 1 and 0.1 $V_{CC}$ for a logic 0.
[2] Interrupt request through Port 3 (P33-P31).
[3] Interrupt request through Port 3 (P30).
[4] SMR – D5 = 0
[5] Reg. WDTMR
[6] 2.0V to 3.9V
[7] Reg. SMR – D5 = 0
[8] Reg. SMR – D5 = 1

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