APPLICATION NOTE
A V A I L A B L E
AN76 • AN78 • AN81 • AN87

64K/32K/16K X24F064/032/016 8K/4K/2K x 8 Bit

SerialFlash™ Memory with Block Lock™ Protection

FEATURES

- **1.8V to 3.6V or 5V "Univolt" Read and Program Power Supply Versions**
- **Low Power CMOS**
  - **—Active Read Current Less Than 1mA**
  - **—Active Program Current Less Than 3mA**
  - **—Standby Current Less Than 1μA**
- **Internally Organized 8K/4K/2K x 8**
- **New Programmable Block Lock Protection**
  - **—Software Write Protection**
  - **—Programmable hardware Write Protect**
- **Block Lock (0, 1/4, 1/2, or all of the Flash Memory array)**
- **2 Wire Serial Interface**
- **Bidirectional Data Transfer Protocol**
- **32 Byte Sector Programming**
- **Self Timed Program Cycle**
  - **—Typical Programming Time of 5ms Per Sector**
- **High Reliability**
  - **—Endurance: 100,000 cycles per byte**
  - **—Data Retention: 100 Years**
- **Available Packages**
  - **—8-Lead PDIP**
  - **—8-Lead SOIC (JEDEC)**
  - **—14-Lead TSSOP (X24F032/016)**
  - **—20-Lead TSSOP (X24F064)**

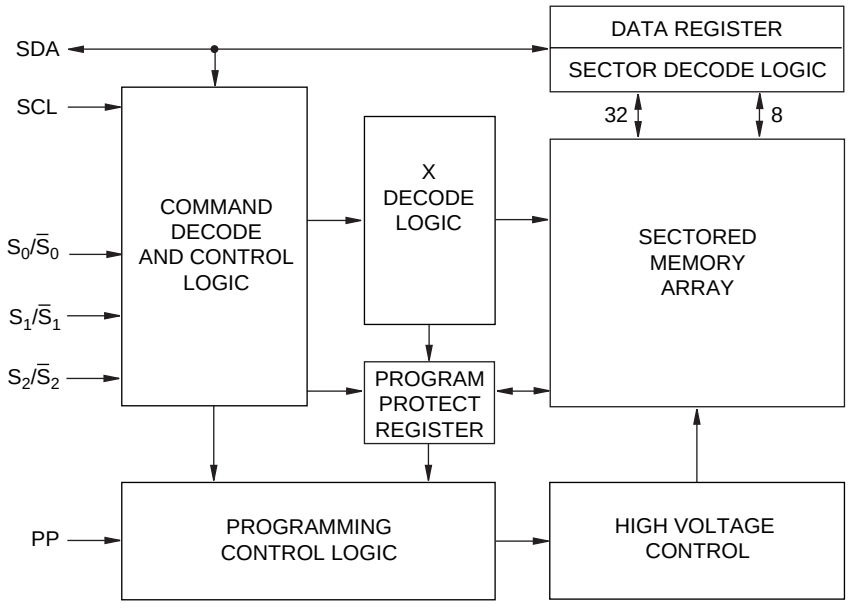
DESCRIPTION

The X24F064/032/016 is a CMOS SerialFlash Memory Family, internally organized 8K/4K/2K x 8. The family features a serial interface and software protocol allowing operation on a simple two wire bus.

Device select inputs (S_0, S_1, S_2) allow up to eight devices to share a common two wire bus.

A Program Protect Register accessed at the highest address location, provides three new programming protection features: Software Programming Protection, Block Lock Protection, and Hardware Programming Protection. The Software Programming Protection feature prevents any nonvolatile writes to the device until the WEL bit in the program protect register is set. The Block Lock™ Protection feature allows the user to individually protect four blocks of the array by programming two bits in the programming protect register. The Programmable Hardware Program Protect feature allows the user to install each device with PP tied to V_{CC}, program the entire memory array in place, and then enable the hardware programming protection by programming a PPEN bit in the program protect register. After this, selected blocks of the array, including the program protect register itself, are permanently protected from being programmed.

FUNCTIONAL DIAGRAM



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Xicor SerialFlash Memories are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the pull-up resistor selection graph at the end of this data sheet.

Device Select (S_0, $\overline{S}_0$, S_1, $\overline{S}_1$, S_2, $\overline{S}_2$)

The device select inputs are used to set the device select bits of the 8-bit slave address. This allows multiple devices to share a common bus. These inputs can be static or actively driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If actively driven, they must be driven with CMOS levels (driven to V_{CC} or V_{SS}).

Program Protect (PP)

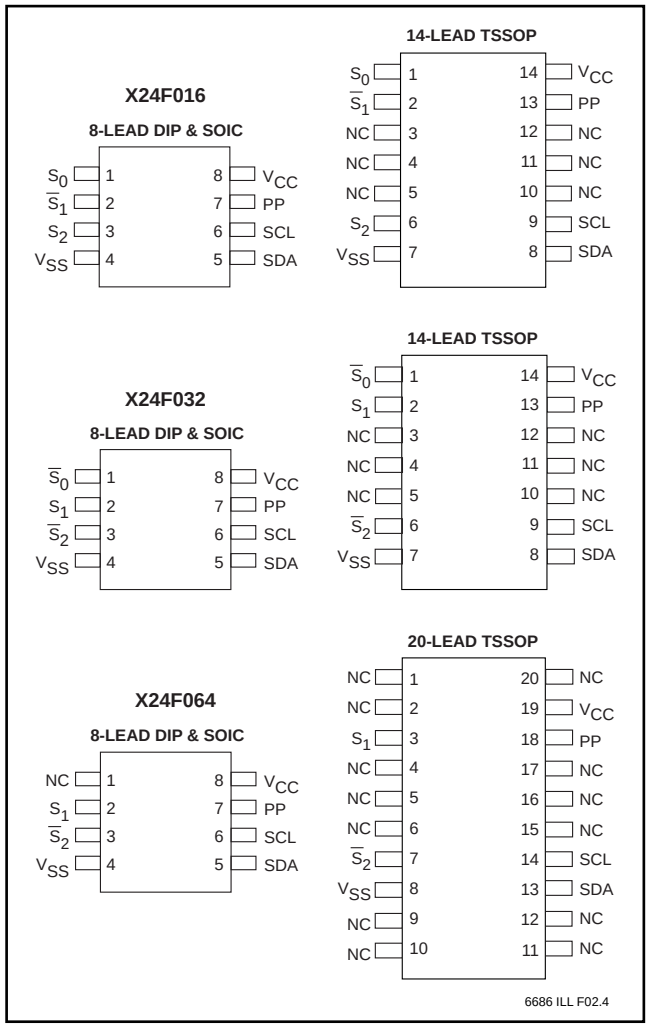
The program protect input controls the hardware program protect feature. When held LOW, hardware program protection is disabled and the X24F064/032/016 can be programmed normally. When this input is held HIGH, and the PPEN bit in the program protect register is set HIGH, program protection is enabled, and nonvolatile writes are disabled to the selected blocks as well as the program protect register itself.

PIN NAMES

Symbol	Description
S_0, $\overline{S}_0$, S_1, $\overline{S}_1$, S_2, $\overline{S}_2$	Device Select Inputs
SDA	Serial Data
SCL	Serial Clock
PP	Program Protect
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

6686 FRM T01.1

PIN CONFIGURATION



DEVICE OPERATION

The X24F064/032/016 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24F064/032/016 will be considered a slave in all applications.

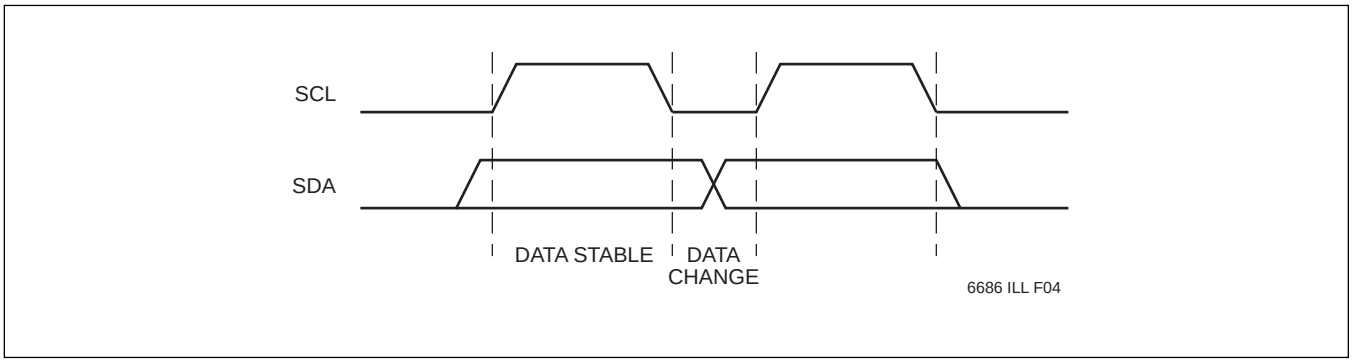
Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

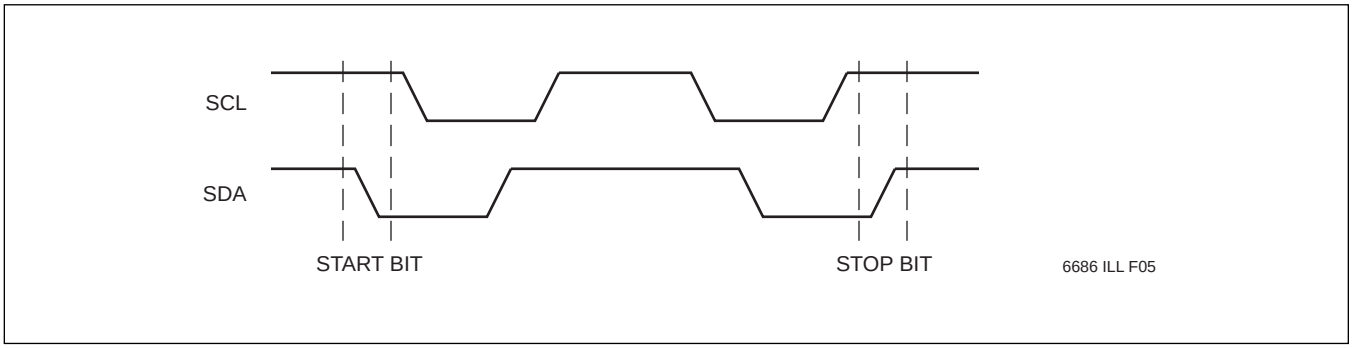
All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24F064/032/016 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Figure 1. Data Validity



Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage (2.7V)
(6) t_{PR} is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal program operation.

Figure 2. Definition of Start and Stop



Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

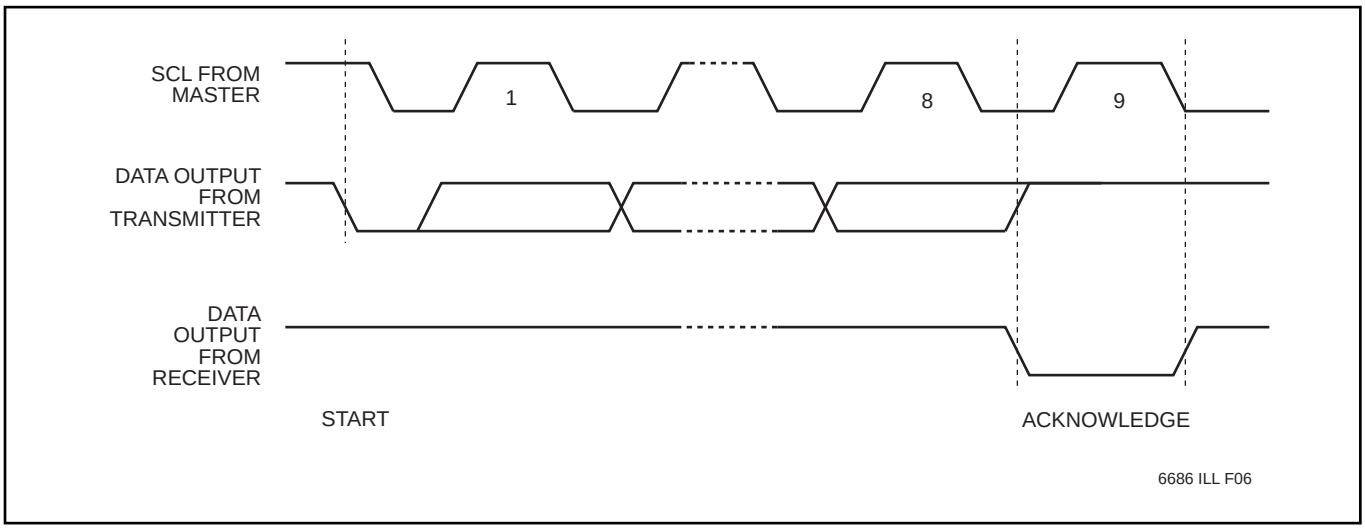
Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24F064/032/016 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24F064/032/016 will respond with an acknowledge after the receipt of each subsequent eight-bit word.

In the read mode the X24F064/032/016 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24F064/032/016 will continue to transmit data. If an acknowledge is not detected, the device will terminate further data transmissions. The master must then issue a stop condition to return the X24F064/032/016 to the standby power mode and place the device into a known state.

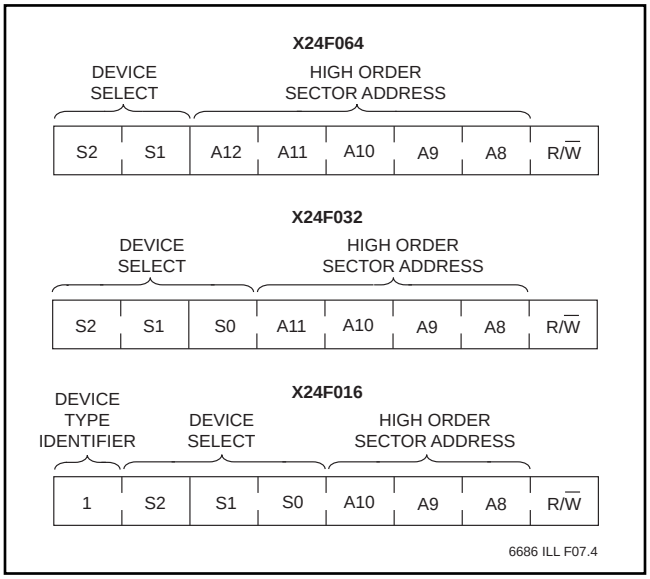
Figure 3. Acknowledge Response From Receiver



DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing (see Figure 4). The next two bits are the device select bits. A system could have up to eight X24F032/016's on the bus or up to four 24F064's on the bus. The device addresses are defined by the state of the S_0, S_1, and S_2 inputs. Note some of the slave addresses must be the inverse of the corresponding input pin.

Figure 4. Slave Address



Also included in the slave address is an extension of the array's address which is concatenated with the eight bits of address in the sector address field, providing direct access to the entire SerialFlash Memory array.

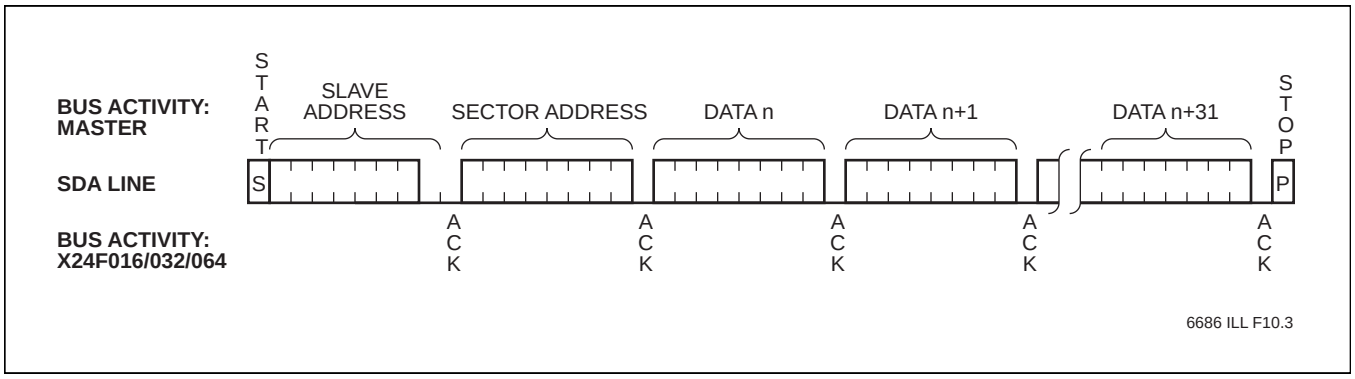
The last bit of the slave address defines the operation to be performed. When set HIGH a read operation is selected, when set LOW a program operation is selected.

Following the start condition, the X24F064/032/016 monitors the SDA bus comparing the slave address being transmitted with its slave address device type identifier. Upon a correct comparison of the device select inputs, the X24F064/032/016 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the X24F064/032/016 will execute a read or program operation.

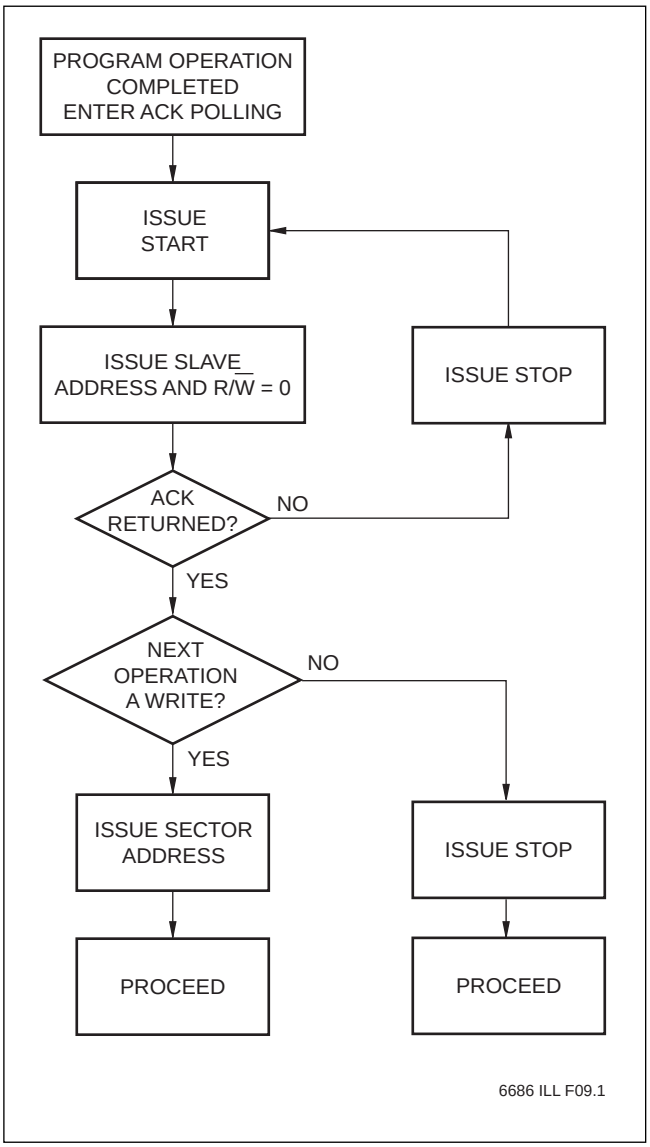
PROGRAMMING OPERATIONS

The X24F064/032/016 offers a 32-byte sector programming operation. For a program operation, the X24F064/032/016 requires a second address field. This field contains the address of the first byte in the sector. Upon receipt of the address, comprised of eight bits, the X24F064/032/016 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. The master then transmits 31 more bytes. After the receipt of each byte, the X24F064/032/016 will respond with an acknowledge.

Figure 5. Sector Programming



Flow 1. ACK Polling Sequence



After the receipt of each byte, the five low order address bits are internally incremented by one. The high order bits of the sector address remain constant. If the master should transmit more or less than 32 bytes prior to generating the stop condition, the contents of the sector cannot be guaranteed. All inputs are disabled until completion of the internal program cycle. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The Max Write Cycle Time can be significantly reduced using Acknowledge Polling. To initiate Acknowledge Polling, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the device is still busy with the high voltage cycle, then no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the read or write operation. Refer to Flow 1.

READ OPERATIONS

Read operations are initiated in the same manner as program operations with the exception that the R/$\overline{W}$ bit of the slave address is set HIGH. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Current Address Read

Internally, the X24F064/032/016 contains an address counter that maintains the address of the last byte read, incremented by one byte. Therefore, if the last read was from address n, the next read operation accesses data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ set HIGH, the X24F064/032/016 issues an acknowledge and transmits the eight-bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 6 for the sequence of address, acknowledge and data transfer.

Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set HIGH, the master must first perform a “dummy” write operation. The master issues the start condition, and the slave address with the R/$\overline{W}$ bit set LOW, followed by the byte address it is to read. After the byte address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set HIGH. This will be followed by an acknowledge from the X24F064/032/016 and then by the eight-bit byte. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the address, acknowledge and data transfer sequence.

Figure 6. Current Address Read

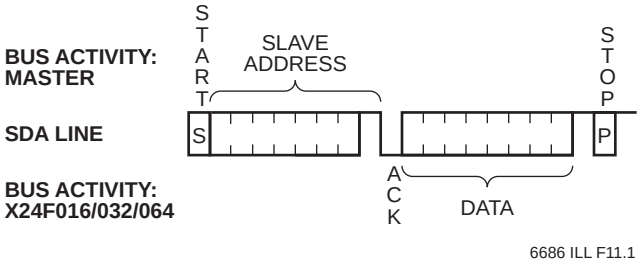
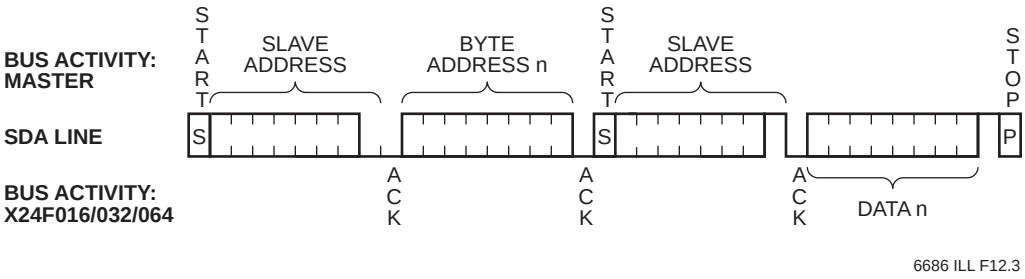


Figure 7. Random Read



Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first byte is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24F064/032/016 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space, the counter “rolls over” to 0 and the X24F064/032/016 continues to output data for each acknowledge received. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Figure 8. Sequential Read

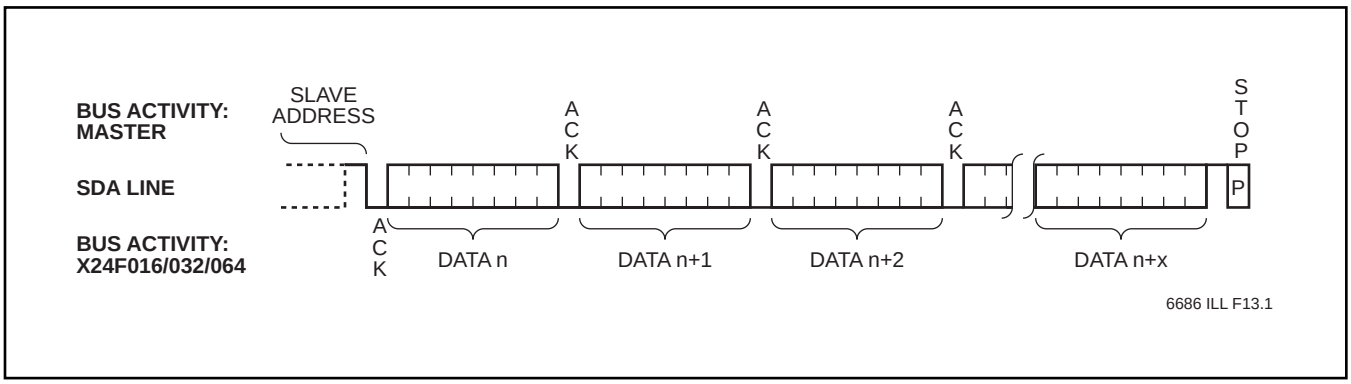
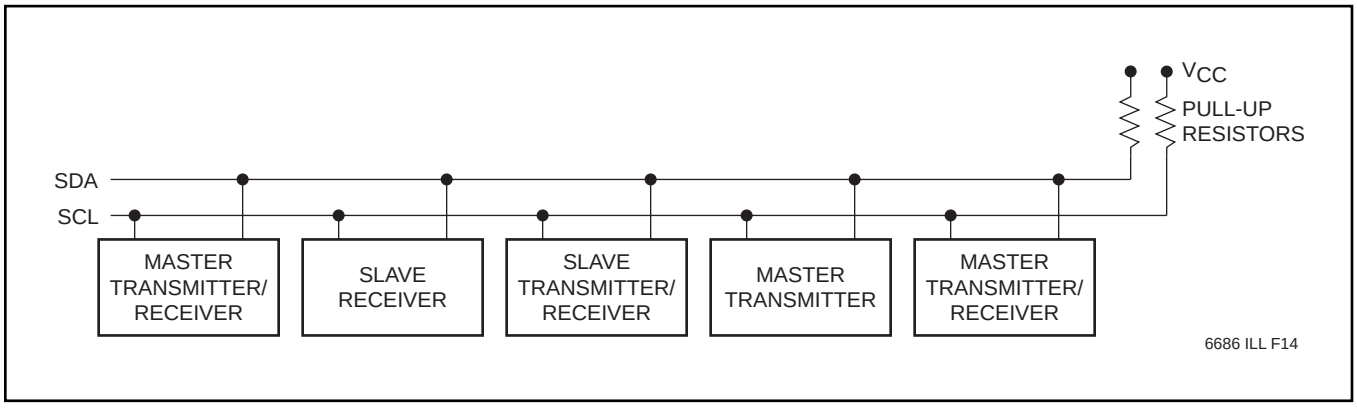


Figure 9. Typical System Configuration



PROGRAM PROTECT REGISTER

The Program Protect Register (PPR) is accessed at the highest address of each device:

X24F064 = 1FFF
X24F032 = 0FFF
X24F016 = 07FF

Figure 10. Program Protect Register

7	6	5	4	3	2	1	0
PPEN	0	0	BL1	BL0	RWEL	WEL	0

6686 ILL F15

PPR.1 = WEL

– Write Enable Latch (Volatile)
0 = Write enable latch reset, programming disabled
1 = Write enable latch set, programming enabled

If WEL = 0 then “no ACK” after first byte of input data.

PPR.2 = RWEL
– Register Write Enable Latch (Volatile)
0 = Register write enable latch reset, programming disabled
1 = Register write enable latch set, programming enabled

PPR.3, PPR.4 = BL0, BL1
– Block Lock Bits (Nonvolatile)
(See Block Lock Bits section for definition)

PPR.7 = PPEN
– Programming Protect Enable Bit (Nonvolatile)
(See Programmable Hardware Program Protect section for definition)

Writing to the Program Protect Register

The Program Protect Register is written by performing a write of one byte directly to the highest address location. During normal Sector Programming, the byte in the array at the highest address will be written instead of the Program Protect Register (assuming programming is not disabled by the Block Lock register).

The state of the Program Protect Register can be read by performing a random read at the highest address location at any time. If a sequential read starting at any other address than the highest address location is performed, the contents of the byte in the array at the highest address location is read out instead of the Program Protect Register.

WEL and RWEL are volatile latches that power-up in the LOW (disabled) state. A write to any address other than the highest address location, where the Program Protect Register is located, will be ignored (no ACK) until the WEL bit is set HIGH. The WEL bit is set by writing 0000001x to the highest address location. Once set, WEL remains HIGH until either reset (by writing 00000000 to the highest address location) or until the part powers-up again. The RWEL bit controls writes to the Block Lock bits. RWEL is set by first setting WEL = 1 and then writing 0000011x to the highest address location. RWEL must be set in order to change the Block Lock bits (BL0 and BL1) or the PPEN bit. RWEL is reset when the Block Lock or PPEN bits are changed, or when the part powers-up again.

Programming the BL or PPEN Bits

A three step sequence is required to change the nonvolatile Block Lock or Program Protect Enable:

1) Set WEL = 1 (write 00000010 to the highest address location, volatile write cycle)

(Start)

2) Set RWEL = 1 (write 00000110 to the highest address location, volatile write cycle)

(Start)

3) Set BL1, BL0, and/or PPEN bits (Write w00yz010 to the highest address location)

w = PPEN, y = BL1, Z = BL0,

(Stop)

Step 3 is a nonvolatile program cycle, requiring 10ms to complete. RWEL is reset (0) by this program cycle, requiring another program cycle to set RWEL again before the Block Lock bits can be changed. RWEL must be 0 in step 3; if w00yz110 is written to the highest address location, RWEL is set but PPEN, BL1 and BL0 are not changed (the device remains at step 2).

Block Lock Bits

The Block Lock Bits BL0 and BL1 determine which blocks of the memory are write-protected:

Table 1. Block Lock Bits

BL1	BL0	Array Locked
0	0	None
0	1	Upper 1/4
1	0	Upper 1/2
1	1	Full Array (WPR not included)

6686 FRM T02

Programmable Hardware Program Protect

The Program Protect (PP) pin and the Program Protect Enable (PPEN) bit in the Program Protect Register control the programmable hardware program protect feature. Hardware program protection is enabled when the PP pin and the PPEN bit are both HIGH, and disabled when either the PP pin is LOW or the PPEN bit is LOW. When the chip is hardware program-protected, nonvolatile programming is disabled, including the Program Protect Register, the BL bits and the PPEN bit itself, as well as to Block Locked sections in the memory array. Only the sections of the memory array that are not Block Locked can be written. Note that since the PPEN bit is program-protected, it cannot be changed back to a LOW state, and program protection is disabled as long as the PP pin is held HIGH. Table 2 defines the program protection status for each state of PPEN and PP.

Table 2. Program Protect Status Table

PP	PPEN	Memory Array (Not Block Locked)	Memory Array (Block Locked)	BL Bits	PPEN Bit
0	X	Programmable	Locked	Programmable	Programmable
X	0	Programmable	Locked	Programmable	Programmable
1	1	Programmable	Locked	Locked	Locked

6686 FRM T03

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X24F064/032/016 ..... –65°C to +135°C
Storage Temperature..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS}..... –1V to +7V
D.C. Output Current.....5mA
Lead Temperature (Soldering, 10 Seconds)..... 300°C

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Extended	–20°C	+85°C
Industrial	–40°C	+85°C

6686 FRM T04.2

Supply Voltage	Limits
X24F064/032/016	1.8V to 3.6V
X24F064/032/016–5	4.5V to 5.5V

6686 FRM T05.2

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	SCL = V_{CC} X 0.1/V_{CC} X 0.9 Levels @ 100KHz, SDA = Open, All Other Inputs = V_{SS} or V_{CC} – 0.3V
I_{CC2}	V_{CC} Supply Current (Write)		3	mA	
I_{SB1}(1)	V_{CC} Standby Current		1	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC} – 0.3V, V_{CC} = 3.6V
I_{SB2}(1)	V_{CC} Standby Current		10	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC} – 0.3V, V_{CC} = 5V ±10%
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(2)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(2)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 3mA

6686 FRM T06.4

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 2.7V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (S_1, $\overline{S}_2$, SCL)	6	pF	V_{IN} = 0V

6686 FRM T07

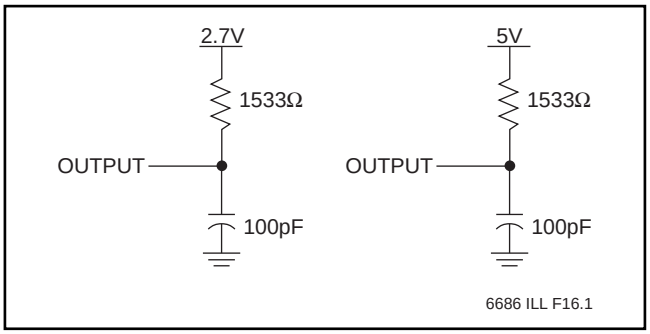
Notes: (1) Must perform a stop command prior to measurement.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not 100% tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} X 0.5

6686 FRM T08

EQUIVALENT A.C. LOAD CIRCUIT



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A.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL LOW to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4		µs
t_{LOW}	Clock LOW Period	4.7		µs
t_{HIGH}	Clock HIGH Period	4		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

6686 FRM T09.1

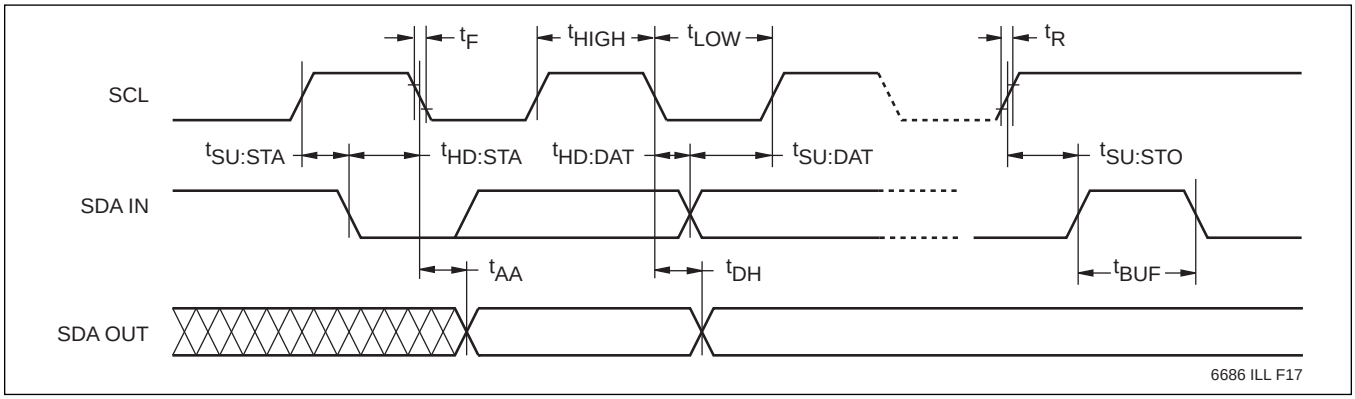
POWER-UP TIMING(4)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	5	ms

6686 FRM T10

Notes: (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Bus Timing



Program Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{PR}(6)	Program Cycle Time		5	10	ms

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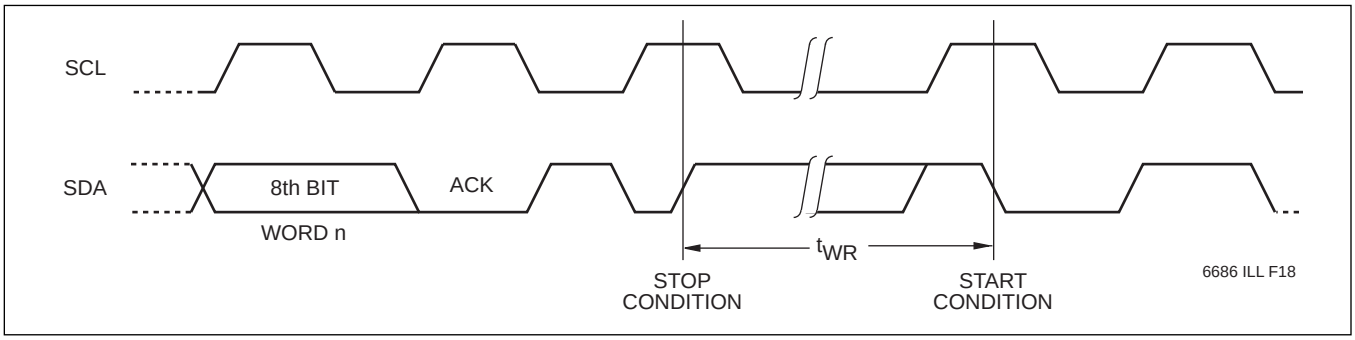
The program cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the program cycle, the X24F064/032/016 bus interface circuits are disabled, SDA is allowed to remain HIGH, and the device does not respond to its slave address.

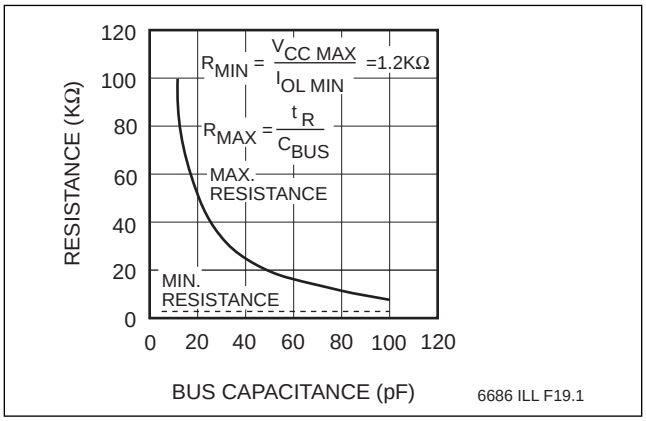
Bus Timing



Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage (2.7V).

(6) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal program operation.

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors

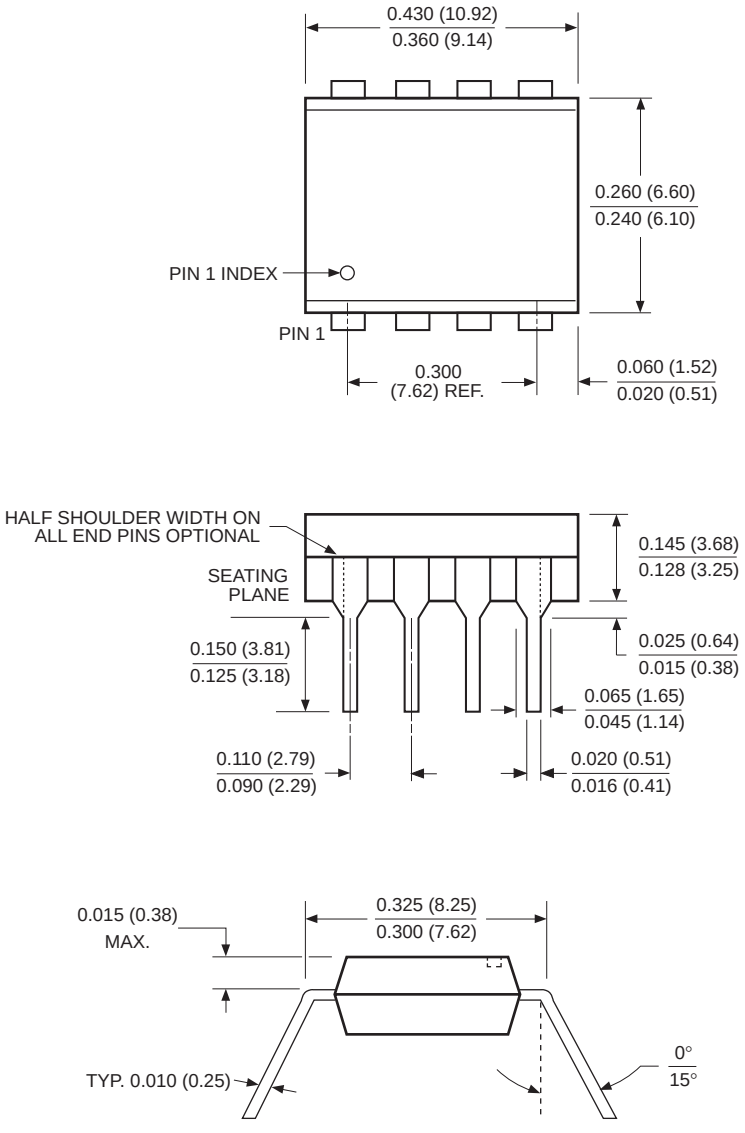


SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



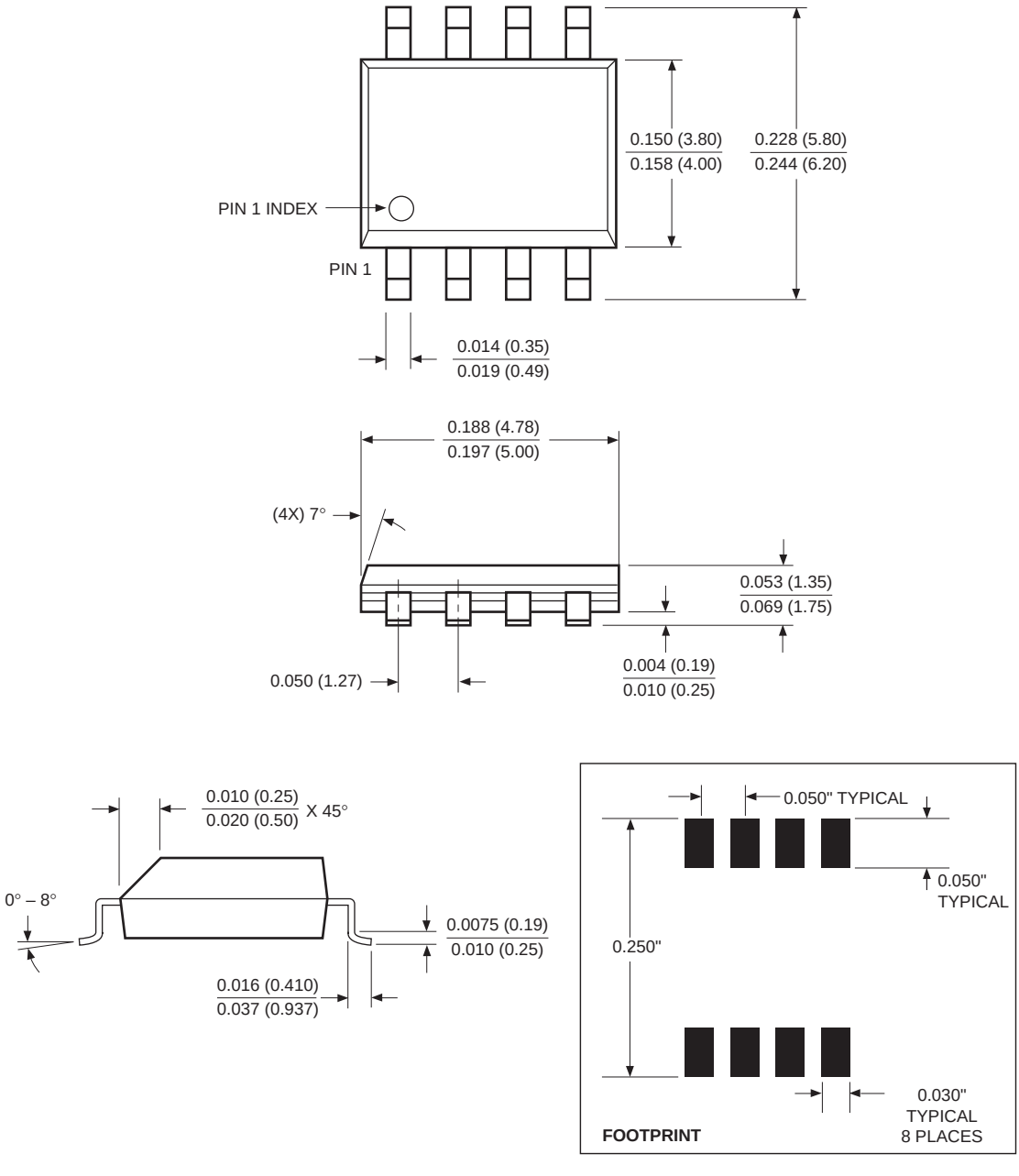
NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F01

PACKAGING INFORMATION

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

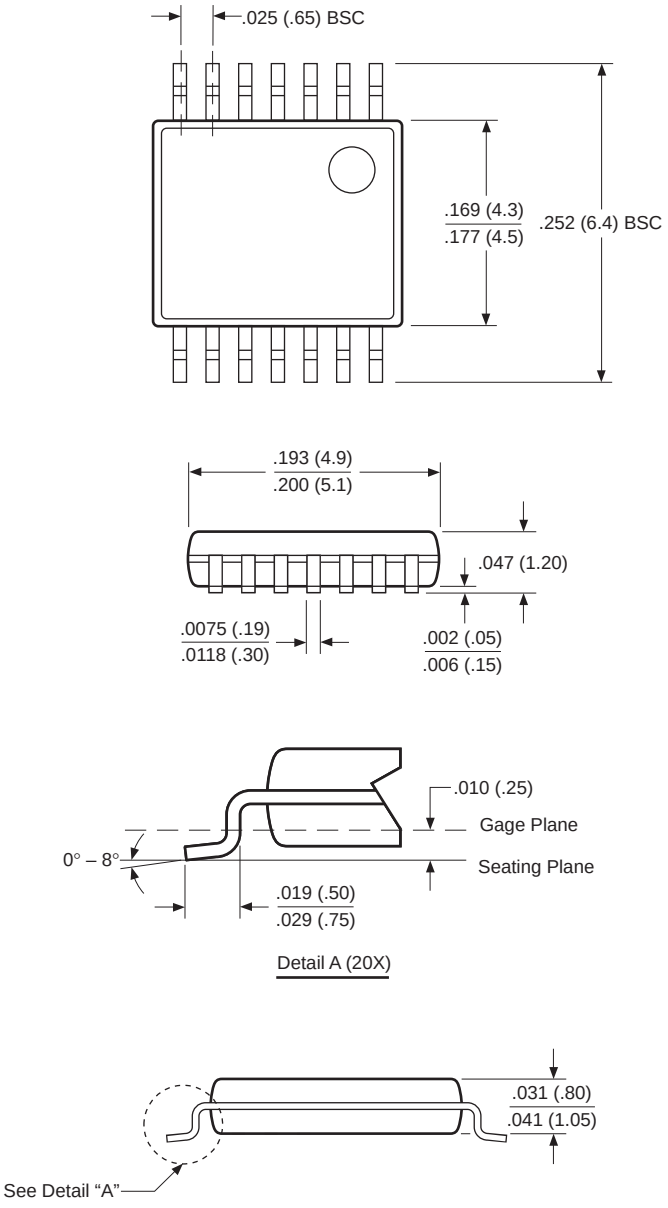


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F22.1

PACKAGING INFORMATION

14-LEAD PLASTIC, TSSOP PACKAGE TYPE V

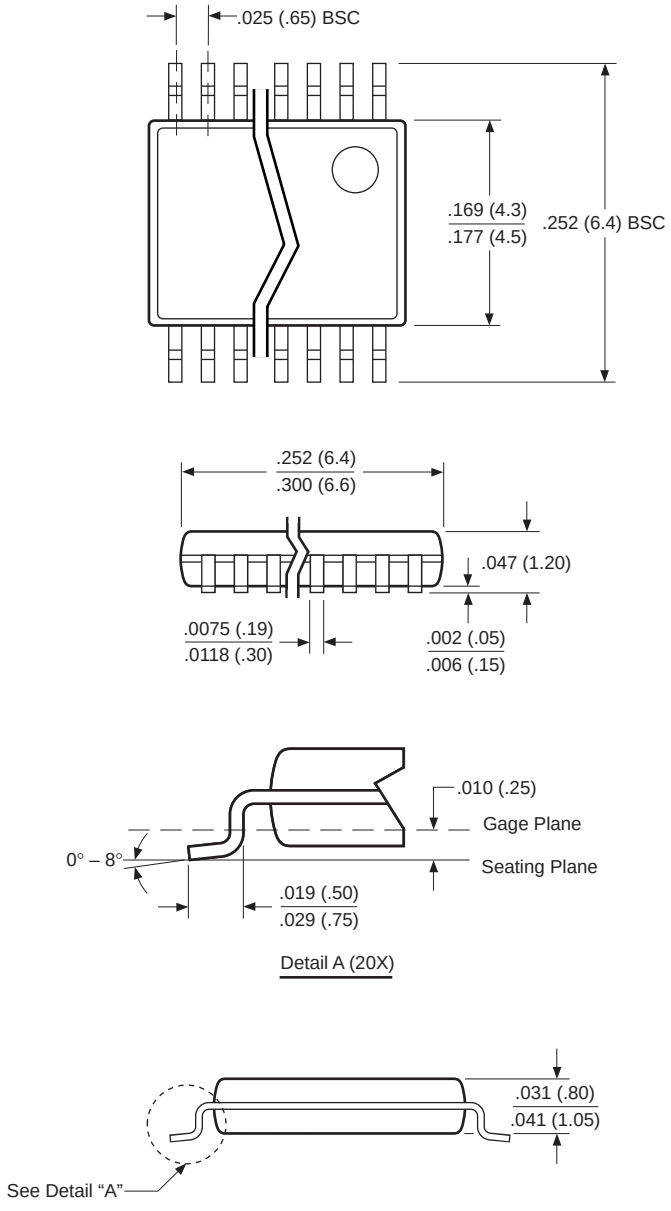


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F32

PACKAGING INFORMATION

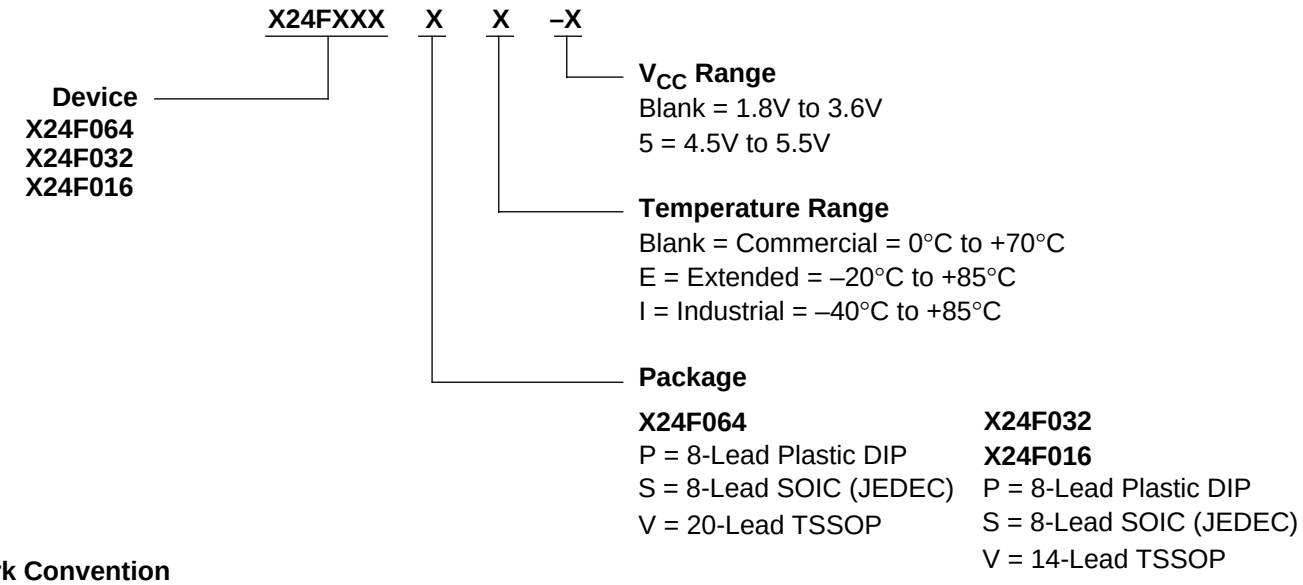
20-LEAD PLASTIC, TSSOP PACKAGE TYPE V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F45

ORDERING INFORMATION



Part Mark Convention