Simple Solution for Dynamically Programming the Output Voltage of DC-DC Converters

INTRODUCTION

Figure 1 shows a typical dc-to-dc converter configuration. As in many PWM controllers, the non-inverting input of the voltage feedback error amplifier is internally connected to the reference voltage, V_r. The output voltage of the converter is set by a resistor divider network R1 and R2. This configuration enables a fixed output voltage that is equal to or greater than the reference voltage. But in many power conversion designs, it is useful to vary the output to a value lower than the reference voltage and to dynamically adjust the output voltage. The op-amp circuit shown in Figure 3 gives designers a simple way to do this. Scaling the output voltage with respect to a control voltage V_C is totally flexible. This application note describes how to use this simple solution and provides a step-by-step design procedure to assist designers in calculating the specific parameters required by their circuits.

DESIGN REQUIREMENT

Reference voltage, V_r
Control voltage: $V_C = V_{C1}$ to V_{C2}
Output voltage: $V_O = V_{O1}$ at $V_C = V_{C1}$, $V_O = V_{O2}$ at $V_C = V_{C2}$, and V_O is linear for any value of V_C in its range.

These design requirements are shown in Figure 2. The output voltage is a linear function with respect to the control voltage. The function crosses two end points A = (V_{C1}, V_{O1}) and B = (V_{C2}, V_{O2}).

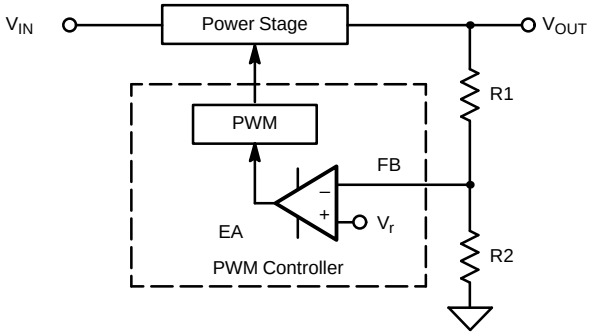


FIGURE 1. Typical DC/DC Converter Configuration

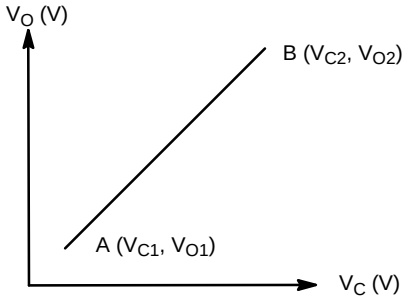


FIGURE 2. Output Voltage vs Control Voltage Requirement

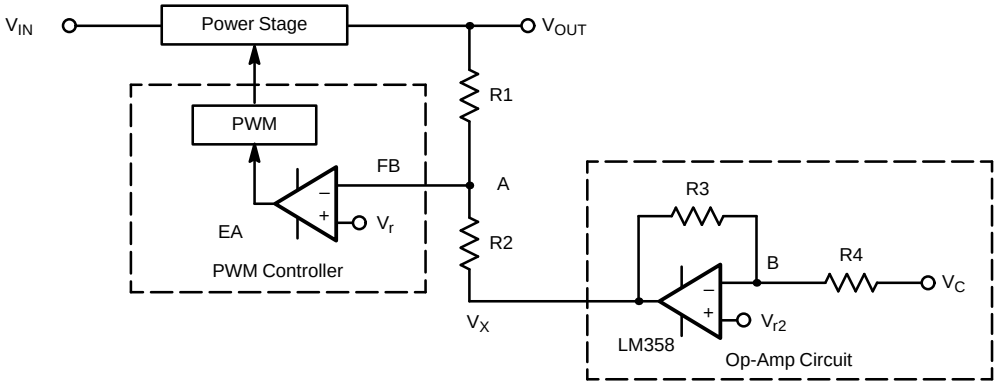


FIGURE 3. Op-Amp Circuit Offers Programmable Output Function

CIRCUIT ANALYSIS

In a closed-loop power supply, node A will servo to attain a voltage equal to V_R. Node B will servo to attain a voltage equal to V_{r2}. Assuming an ideal op-amp and using Kirchkorf's current law at node A and B, we have:

$$\frac{(Vo - Vr)}{R1} = \frac{(Vr - Vx)}{R2}$$

and (1)

$$\frac{(Vx - Vr2)}{R3} = \frac{(Vr2 - Vc)}{R4}$$

Let:

$$M1 = \frac{R2}{R1}$$

and (2)

$$M2 = \frac{R3}{R4}$$

Solve for V_X,

$$Vx = (1 + m1)Vr - m1Vo$$

and (3)

$$Vx = (1 + m2)Vr2 - m2Vc$$

Equate the above two equations and solve for V_O:

$$Vo = \left(\frac{1}{m1} + 1\right)Vr - \left(\frac{1 + m2}{m1}\right)Vr2 + \frac{m2}{m1}Vc = b + aVc \quad (4)$$

Where:

$$a = \frac{m2}{m1}$$

and (5)

$$b = \left(\frac{1}{m1} + 1\right)Vr - \left(\frac{1 + m2}{m1}\right)Vr2$$

So, V_O is a linear function with respect to V_C. The function has slope a and y intercept b.

A curve-fitting technique is used to force the equation (4) to follow the requirement. This is done in two steps:

Matching the slope:

$$a = \frac{Vo2 - Vo1}{Vc2 - Vc1} = \frac{m2}{m1} \quad (6)$$

Matching one point: Pick point B $\rightarrow V_{O2} = b + aV_{C2}$

$$\rightarrow b = Vo2 - aVc2 = \left(\frac{1}{m1} + 1\right)Vr - \left(\frac{1}{m1} + a\right)Vr2 \quad (7)$$

Equate (4) and (5) and solve for m1

$$m1 = \frac{Vr - Vr2}{Vo2 + a(Vr2 - Vc2) - Vr} \quad (8)$$

Note:

$$m1 = \frac{R2}{R1} \quad (9)$$

Since m1 is the ratio of 2 real resistors, it must be a positive number. Furthermore, m1 should not be too small or too large to have realistic resistor values for R1 and R2. There are two valid scenarios:

1. $Vr - Vr2 > 0$ and $Vo2 + a(Vr2 - Vc2) - Vr > 0$ or,
2. $Vr - Vr2 < 0$ and $Vo2 + a(Vr2 - Vc2) - Vr < 0$

Both of these present a restricted range of values for V_{r2} to give a meaningful value of m1. Once V_{r2} is chosen correctly, m1 and the rest of the parameter values can be determined.

DESIGN PROCEDURE AND EXAMPLE

Given:

$A = (V_{C1}, V_{O1}) = (0.2\ V, 0.4\ V)$, $B = (V_{C2}, V_{O2}) = (2.7\ V, 3.4\ V)$
$V_r = 1.3\ V$, $R1 = 22.1\ k\Omega$. Also, $1\ V < V_X < 3\ V$.

Calculate the slope, a:

$$a = \frac{Vo2 - Vo1}{Vc2 - Vc1} = \frac{3.4 - 0.4}{2.7 - 0.2} = 1.2 \quad (10)$$

Determine V_{r2}:

Choose a sensible value of V_{r2} to satisfy either (1) or (2) above. Since it is easier to derive a value for V_{r2} that is smaller than V_r (by using a simple resistor voltage divider), scenario (1) is used here.

$$Vr - Vr2 > 0 \Rightarrow Vr2 < Vr = 1.3\ V$$

and,

$$Vo2 + a(Vr2 - Vc2) - Vr > 0 \Rightarrow Vr2 > \frac{Vr - Vo2}{a} + Vc2 = \frac{1.3\ V - 3.4\ V}{1.2} + 2.7 = 0.95V \quad (11)$$

To limit the common mode range of V_X, the following equations can be used:

1. To keep V_X equal or greater than a minimum value, V_{Xm}= 1 V:

$$Vr2 \geq \frac{Vxm(Vo2–Vr–aVc2) + aVc2Vr}{Vo2 + a(Vr–Vxm)–Vr} = \frac{1(3.4–1.3–1.2 \times 2.7) + 1.2 \times 2.7 \times 1.3}{3.4 + 1.2(1.3–1)–1.3} = 1.249 \quad (12)$$

2. To keep V_X equal or less than a maximum value, V_{Xm} = 3 V:

$$Vr2 \geq \frac{VxM(Vo2–Vr–aVc2) + aVc1Vr}{Vo2 + a(Vr–VxM–Vc2 + Vc1)–Vr} = \frac{2(3.4–1.3–1.2 \times 2.7) + 1.2 \times 0.2 \times 1.3}{3.4 + 1.2(1.3–2–2.7 + 0.2)–1.3} = 1.13\ V \quad (13)$$

So, V_{r2} can be any value between 1.249 V and 1.3 V. Choose V_{r2} = 1.25 V.

Calculate m1 and then R2:

$$m1 = \frac{Vr–Vr2}{Vo2 + a(Vr2–Vc2)–Vr} = \frac{1.3–1.25}{3.4 + 1.2(1.25–2.7)–1.3} = 0.139 \quad (14)$$

$$m1 = \frac{R2}{R1} \Rightarrow R2 = m1R1 = 0.139 \times 22.1\ k = 3.07\ k\Omega$$

Choose R2 = 3.01 kΩ as a practical value

Calculate R3 and R4:

$$a = \frac{m2}{m1} = \frac{R3}{m1R4} \Rightarrow R3 = am1R4 \quad (15)$$

Choose R4, then calculate R3. The value of R4 should be large enough such that the current going through it will not be so large as to cause excessive power dissipation under extreme conditions. On the other hand, R4 should be small enough that its current will not be overly sensitive to noise and op-amp bias current.

If R4 is set at 22.1k, then R3 = 3.68 k, and we can choose R3 = 3.60 k as a practical value.

Express V_O as a function of V_C, using practical values of R's:

$$a = \frac{m2}{m1} = \frac{R1R3}{R2R4} = \frac{22.1kx3.68k}{3.01kx22.1k} = 1.223$$

$$b = \left(\frac{1}{m1} + 1\right)Vr–\left(\frac{1}{m1} + a\right)Vr2 = \left(\frac{R1}{R2} + 1\right)Vr–\left(\frac{R1}{R2} + a\right)Vr2 \quad (16)$$

$$b = \left(\frac{22.1k}{3.01k} + 1\right)1.3–\left(\frac{22.1k}{3.01k} + 1.223\right)1.25 = 0.1389$$

The final result: $V_O = aV_C + b = 1.223 \times V_C + 0.1389$

EXPERIMENTAL RESULTS

A circuit was built and tested (see Figure 5). The result is tabulated in Table 1 and plotted in Figure 4:

TABLE 1

	V_X	V_O		
V_C	Measured	Calculated	Measured	Required
0.1	1.43	0.26	0.32	
0.2	1.42	0.38	0.42	0.40
0.4	1.38	0.63	0.68	0.64
0.8	1.32	1.12	1.16	1.12
1.2	1.25	1.61	1.66	1.60
1.6	1.19	2.10	2.12	2.08
2.0	1.11	2.58	2.68	2.56
2.4	1.05	3.07	3.11	3.04
2.6	1.02	3.32	3.33	3.28
2.7	1.00	3.44	3.46	3.40
2.8	0.99	3.56	3.58	
3.0	0.96	3.81	3.78	

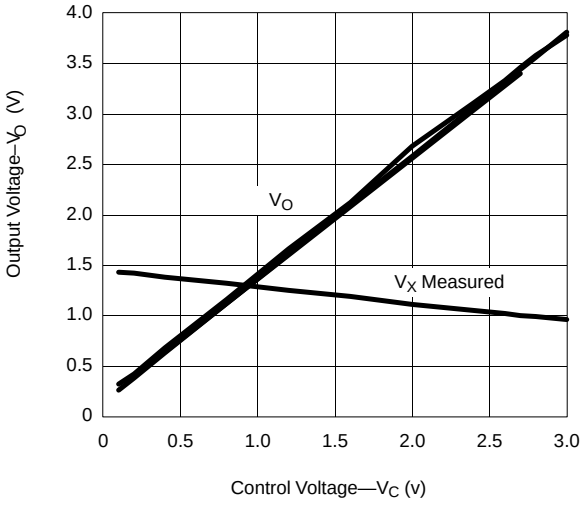


FIGURE 4.

The measured values are very much in agreement with the calculated and required values. A negligible error results from the difference between an ideal op-amp and the actual circuit with its finite offset voltage and bias current.

DYNAMIC RESPONSE PERFORMANCE

Figures 7 and 8 show the dynamic response of the output voltage with different dynamic control voltages. The V_O response and settling time depend on the following factors:

1. the bandwidth of the converter control loop: the larger the bandwidth, the faster V_O response time
2. the large signal response slew rate of the converter: the faster the slew rate, the faster the response
3. the slew rate of the converter control loop error amplifier
4. the bandwidth of the difference amplifier.

The bandwidth of the converter control loop is the most important parameter. The maximum attainable bandwidth of a converter control loop is 1/(2*pi) times the switching frequency. For a converter switching at 100 kHz, the control bandwidth is limited to 16 kHz. Vishay Siliconix high-frequency switching regulators (including the Si9165, Si9169, and Si9170) offer switching frequencies up to 2 MHz and have a theoretical bandwidth limit of 318 kHz. Thus they would be good candidates for this kind of application. Figure 5 shows a complete example of a dc-to-dc converter using the Si9165 controller IC and the op-amp circuit. The output voltage can be programmed from 0.4 V to 3.4 V with a control voltage from 0.2 V to 2.7 V. Figure 6 shows a similar example using the Si9166 controller.

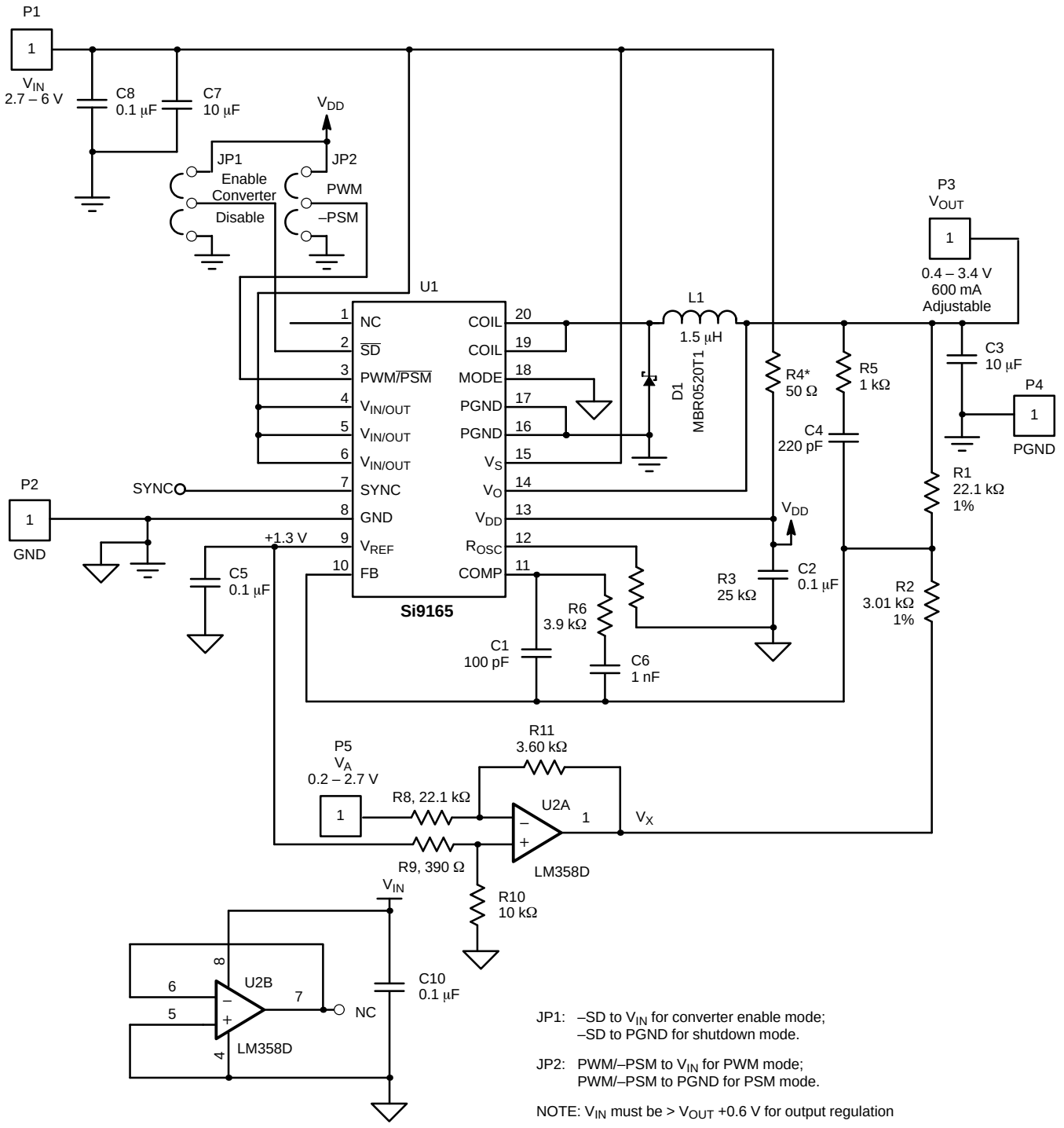
The signal response slew rate of the converter dictates how fast the converter can slew its output voltage up or down given an infinitely large control loop bandwidth. The converter slew rate depends on the converter output averaging LC filter. The smaller the LC, the faster the slew rate.

With respect to the slew rate of the converter control loop error amplifier, most of the converter control loop is figured as an integrator. The error amplifier often drives a fairly large integrator capacitor. The slew rate of the op-amp should be sized adequately.

The bandwidth of the difference amplifier requires the difference amplifier to have its unity gain bandwidth a decade or more larger than the control loop bandwidth.

CONCLUSION

A simple op-amp circuit is used to program the output voltage of a typical dc-to-dc converter. The circuit offers flexible voltage scaling using a linear control voltage. The control voltage can be hard-wired for fixed-voltage operation. When used together with a wide bandwidth dc-to-dc converter, the circuit offers a simple solution for controlling the output voltage dynamically.



JP1: –SD to V_{IN} for converter enable mode;
–SD to PGND for shutdown mode.

JP2: PWM/–PSM to V_{IN} for PWM mode;
PWM/–PSM to PGND for PSM mode.

NOTE: V_{IN} must be > V_{OUT} +0.6 V for output regulation

* = Optional

FIGURE 5. Schematic of Design Example, Using Si9165 Converter

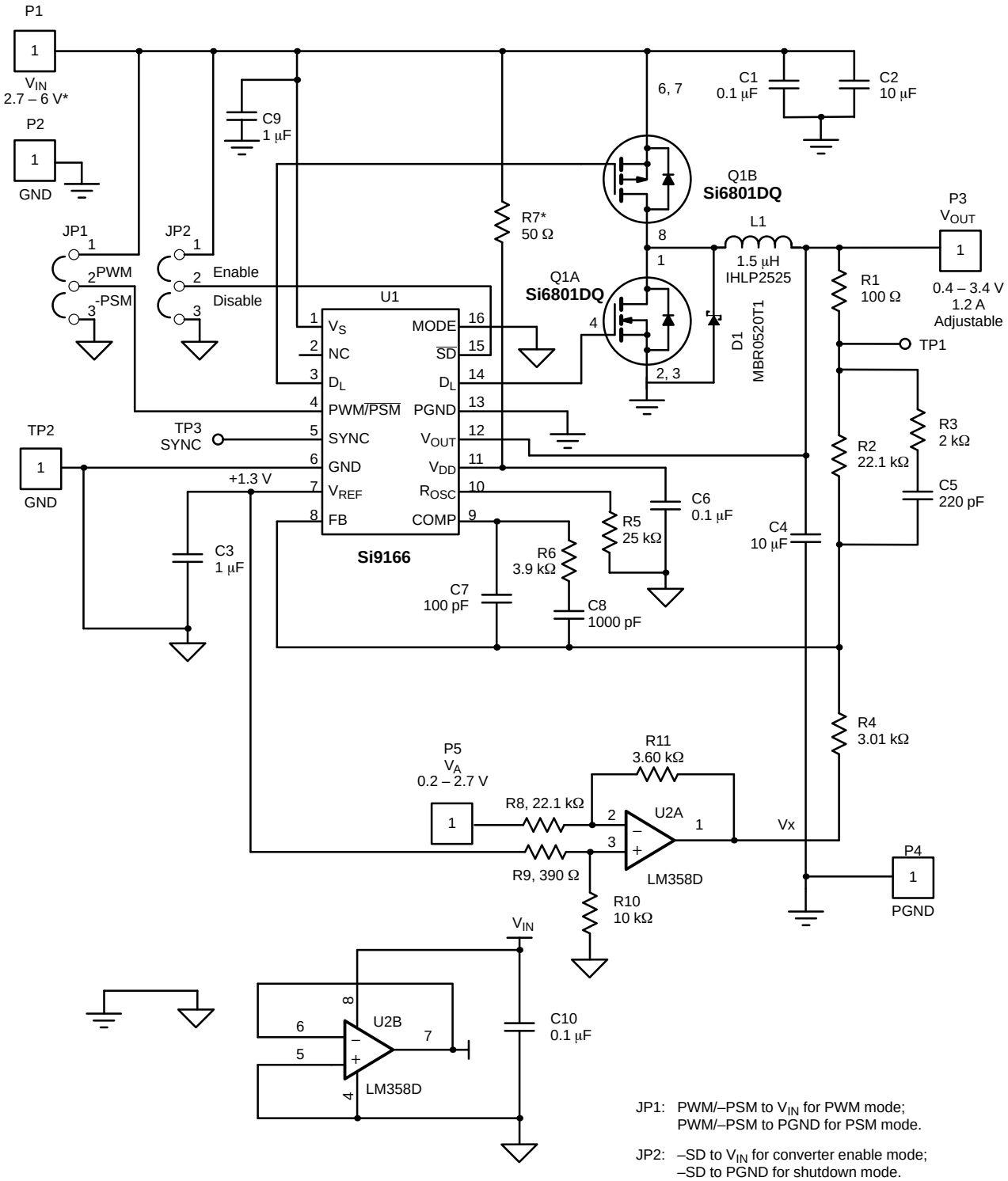
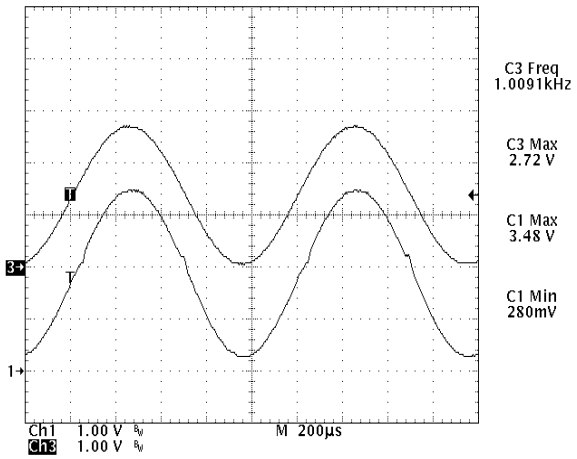
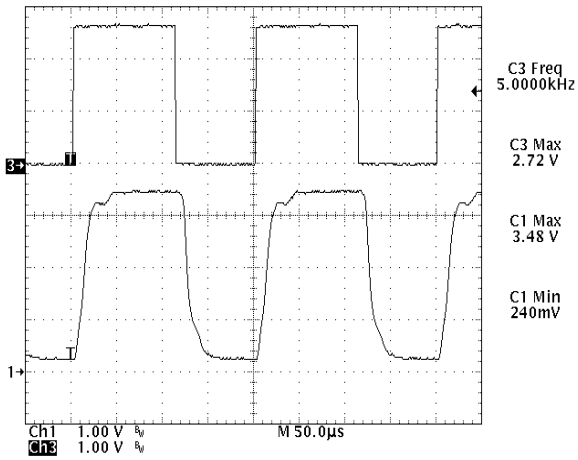


FIGURE 6. Example Circuit Using Si9166 Controller



Sine Wave Control Voltage, 1 kHz
Ch3: Control Voltage
Ch1: Output Voltage
V_{IN} = 5 V, I_O = 300 mA

FIGURE 7. Output Voltage vs Control Voltage



Square Wave Control Voltage, 5 kHz
Ch3: Control Voltage
Ch1: Output Voltage
V_{IN} = 5 V, I_O = 300 mA

FIGURE 8. Output Voltage vs Control Voltage