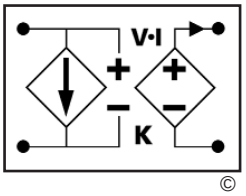
V•I Chip™ – VTM
Voltage Transformation Module

V048K015T80[1]



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V_f = 32 - 57.6 V
V_{OUT} = 1.0 - 1.8 V
I_{OUT} = 80 A
K = 1/32
R_{OUT} = 1.5 mΩ max

- 48V to 1.5V V•I Chip Converter
- 80 A (120 A for 1 ms)
- High density – up to 320 A/in³
- Small footprint – 80 A/in²
- Low weight – 0.4 oz (12 g)
- Pick & Place / SMD
- >92% efficiency at 1.5V
- 125°C operation
- 1 µs transient response
- >3.5 million hours MTBF
- No output filtering required
- V•I Chip BGA package

Actual size

Product Description

The V048K015T80 V•I Chip Voltage Transformation Module (VTM) breaks records for speed, density and efficiency to meet the demands of advanced DSP, FPGA, ASIC, processor cores and microprocessor applications at the point of load (POL) while providing isolation from input to output. It achieves a response time of less than 1 µs and delivers up to 80A in a volume of less than 0.25 in³ while converting 48 V to 1.5 V with unprecedented efficiency. It may be paralleled to deliver hundreds of amps at an output voltage settable from 1.0 to 1.8 Vdc.

The VTM V048K015T80's nominal output voltage is 1.5 Vdc from a 48 Vdc input factorized bus, V_f, and is controllable from 1.0 to 1.8 Vdc at no load, and from 0.9 V to 1.7 V at full load, over a V_f input range of 32 to 57.6 Vdc. It can be operated either open- or closed-loop depending on the output regulation needs of the application. Operating open-loop, the output voltage tracks its V_f input voltage with a transformation ratio, K=1/32, and an output resistance, R_{OUT} =1.3 milliohm, to enable applications requiring a programmable low output voltage at high current and high efficiency. Closing the loop back to an input Pre-Regulation Module (PRM) or DC-DC converter may be used to compensate for R_{OUT}.

The 1.5V VTM achieves break-through current density of 320 A/in³ in a V•I Chip package compatible with standard pick-and-place and surface mount assembly processes. The V•I Chip BGA package supports in-board mounting with a low profile of 0.16" (4mm) over the board. A J-lead package option supports on-board surface mounting with a profile of only 0.25" (6mm) over the board. The VTM's fast dynamic response and low noise eliminate the need for bulk capacitance at the load, substantially increasing the POL density while improving reliability and decreasing cost.

Absolute Maximum Ratings

Parameter	Values	Unit	Notes
+In to -In	-1.0 to 60.0	Vdc	
+In to -In	100	Vdc	For 100 ms
PC to -In	-0.3 to 7.0	Vdc	
TM to -In	-0.3 to 7.0	Vdc	
SG to -In	500	mA	
+Out to -Out	-0.5 to 5.0	Vdc	
Isolation voltage	1500	Vdc	Input to Output
Operating junction temperature	-40 to 125	°C	See note 2
Output current	80	A	Continuous
Peak output current	120	A	For 1 ms
Case temperature during reflow	208	°C	
Storage temperature	-40 to 150	°C	
Output power	144	W	Continuous
Peak output power	216	W	For 1 ms

Thermal Resistance

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Junction-to-case	1.1	1.5	°C/W
$R_{\theta JB}$	Junction-to-BGA	2.1	2.5	°C/W
$R_{\theta JA}$	Junction-to-ambient [3]	6.5	7.2	°C/W
$R_{\theta JA}$	Junction-to-ambient [4]	5.0	5.5	°C/W

Notes

1. For complete product matrix, see chart on page 10.
2. The referenced junction is defined as the semiconductor having the highest temperature. This temperature is monitored by the temperature monitor (TM) signal and by a shutdown comparator.
3. V048K015T80 surface mounted in-board to a 2" x 2" FR4 board, 4 layers 2 oz Cu, 300 LFM.
4. V048L015T80 (0.25"H integral Pin Fins) surface mounted on FR4 board, 300 LFM.

INPUT (Conditions are at nominal line, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Input voltage range	32	48	57.6	V	
Input dV/dt			10	V/µs	
Input undervoltage turn-on			32	V	
Input undervoltage turn-off	29.5			V	
Input overvoltage turn-on	57.6			V	
Input overvoltage turn-off			59.0	V	
Input quiescent current		2.0	2.4	mA	PC low
Inrush current overshoot		0.7		A	Using test circuit in Fig.24; See Fig.1
Input current			2.7	A	
Input reflected ripple current		28		mA p-p	Using test circuit in Fig.24; See Fig.4
No load power dissipation		2.5	3.5	W	
Internal input capacitance		1		µF	
Internal input inductance		20		nH	
Recommended external input capacitance	8	100		µF	200 nH maximum source inductance; See Fig.24

INPUT WAVEFORMS

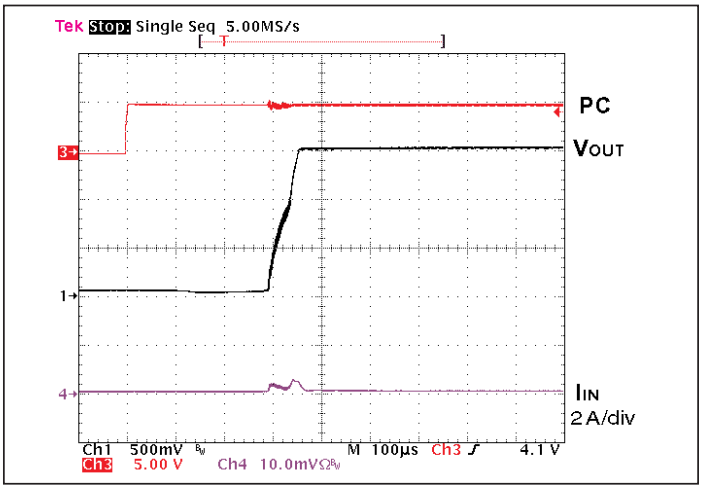


Figure 1— *Inrush transient current at no load and nominal V_{IN} with PC enabled*

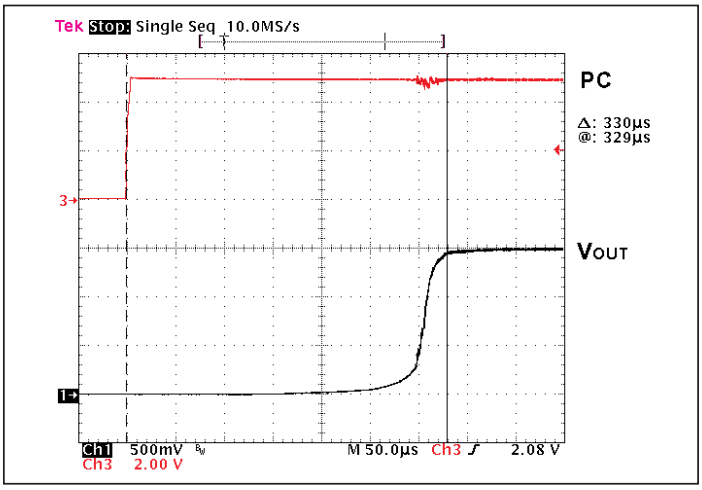


Figure 2— *Output voltage turn-on waveform with PC enabled at full load and nominal V_{IN}*

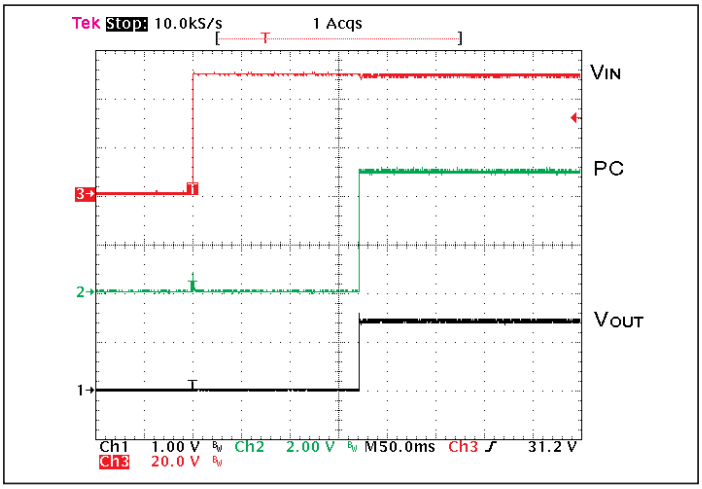


Figure 3—*Output voltage turn-on waveform with input turn-on at full load and nominal V_{IN}*

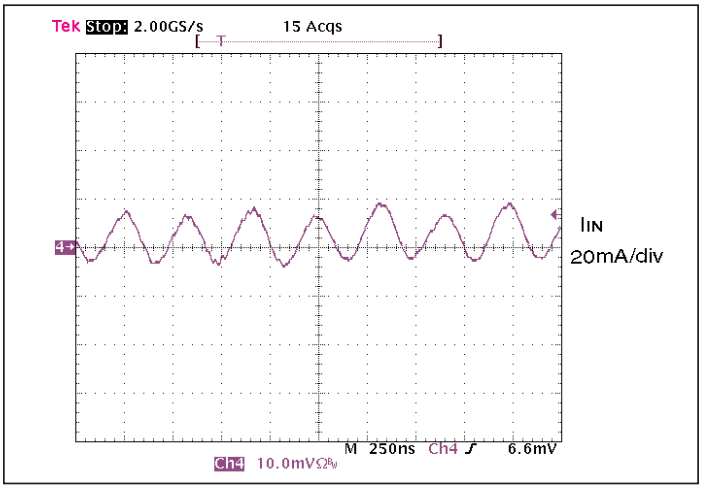


Figure 4— *Input reflected ripple current at full load and nominal V_{IN}*

OUTPUT (Conditions are at nominal line, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Rated DC current	0		80	A	
Peak repetitive current			120	A	Max pulse width 1ms, max duty cycle 10%, baseline power 50%
DC current limit	80	95	120	A	
Current share accuracy		5	10	%	See Parallel Operation on page 11
Efficiency					
Half load	93.0	93.8		%	See Fig.5
Full load	90.8	91.7		%	See Fig.5
Internal output inductance		1.6		nH	
Internal output capacitance		300		µF	Effective value
Load capacitance			100,000	µF	
Output overvoltage setpoint		1.83		V	
Output ripple voltage					
No external bypass		47	70	mV	See Figs.7 and 10
200µF bypass capacitor		2		mV	See Fig.8
Average short circuit current		200		mA	
Effective switching frequency	2.5	3.0	3.6	MHz	Fixed, 1.5 MHz per phase
Line regulation					
K	0.0309	1/32	0.0316		$V_{OUT}=K \bullet V_{IN}$ at no load
Load regulation					
R_{OUT}		1.3	1.5	mΩ	See Figs.9 and 27
Transient response					
Voltage undershoot		10		mV	0-80A load step with 100µF C_{IN}; See Figs.11 and 12
Voltage overshoot		26		mV	80-0A load step with 100µF C_{IN}
Response time		200		ns	See Figs.11 and 12
Recovery time		1		µs	See Figs.11 and 12
Output overshoot					
Input turn-on		0		mV	
PC enable		0		mV	
Output turn-on delay					
From application of power		170	250	ms	No output filter; See Fig.3
From release of PC pin		300		µs	No output filter; See Fig.2

OUTPUT WAVEFORMS

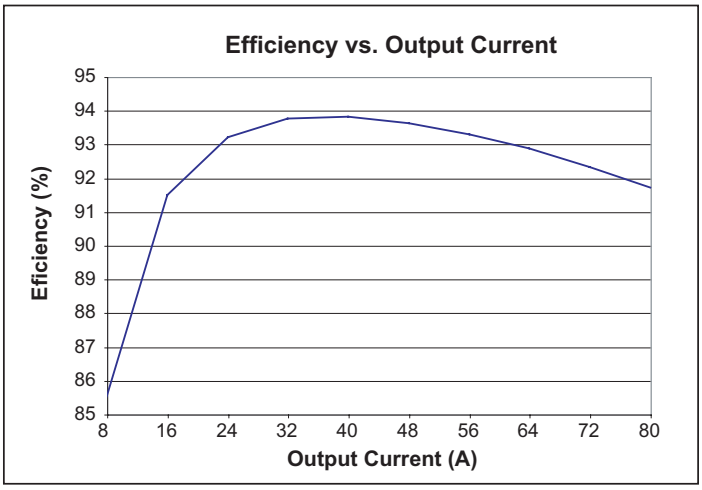


***Figure 5**— Efficiency vs. output current at 1.5V V_{OUT}*

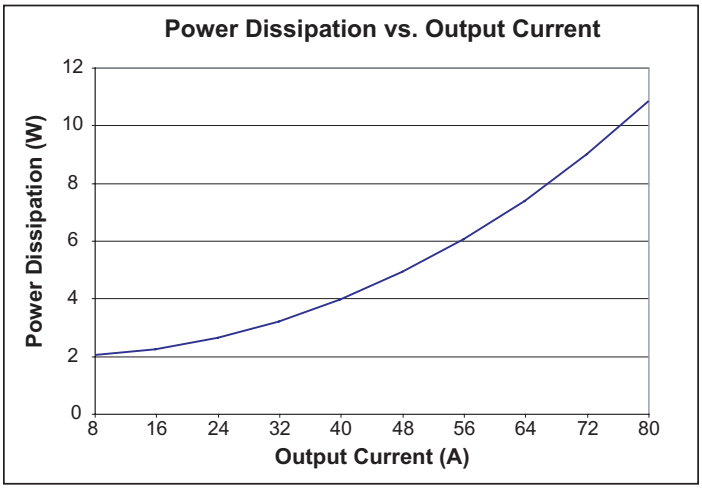


***Figure 6**—Power dissipation as a function of output current at 1.5V V_{OUT}*

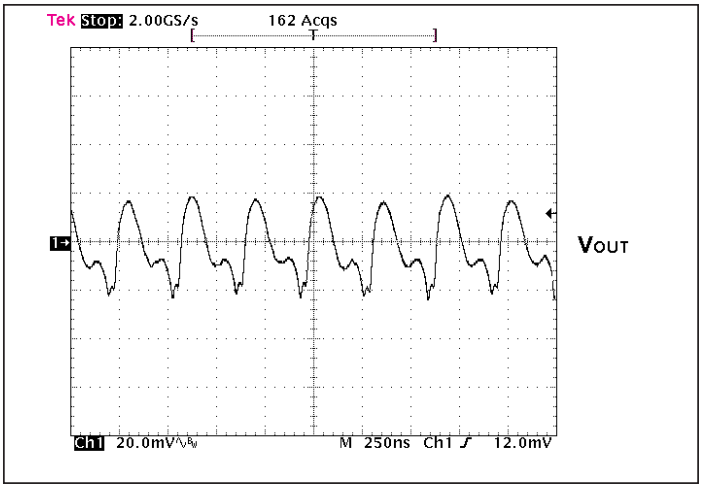


***Figure 7**— Output voltage ripple at full load and nominal V_{IN}; without any external bypass capacitor.*

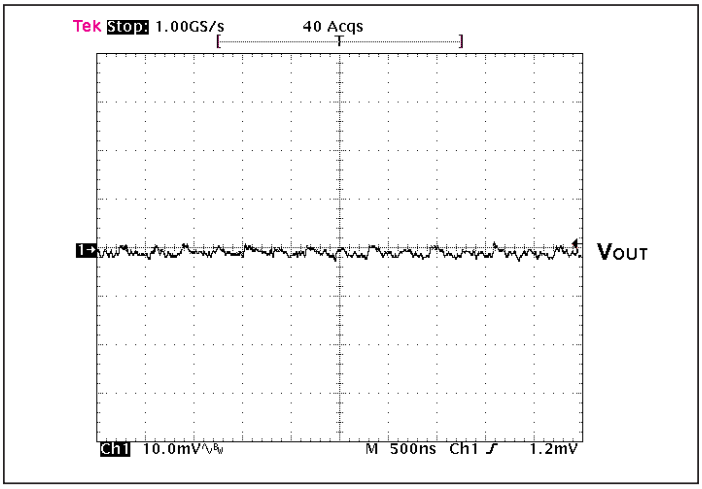


***Figure 8**—Output voltage ripple at full load and nominal V_{IN} with 200 µF ceramic external bypass capacitance.*

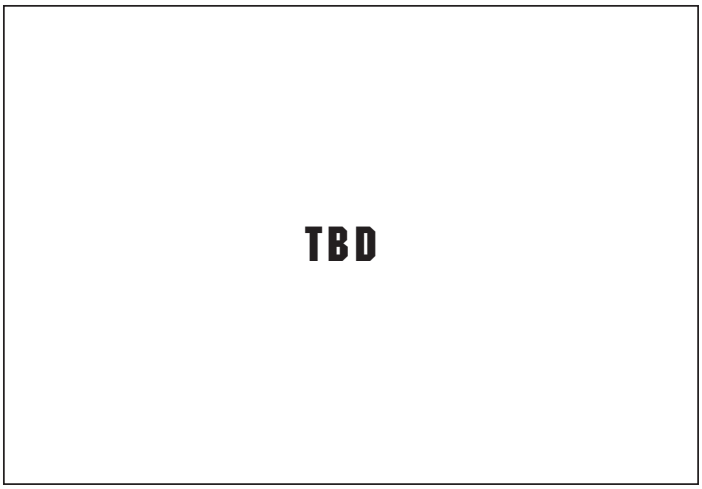


***Figure 9**— Output impedance vs. frequency*

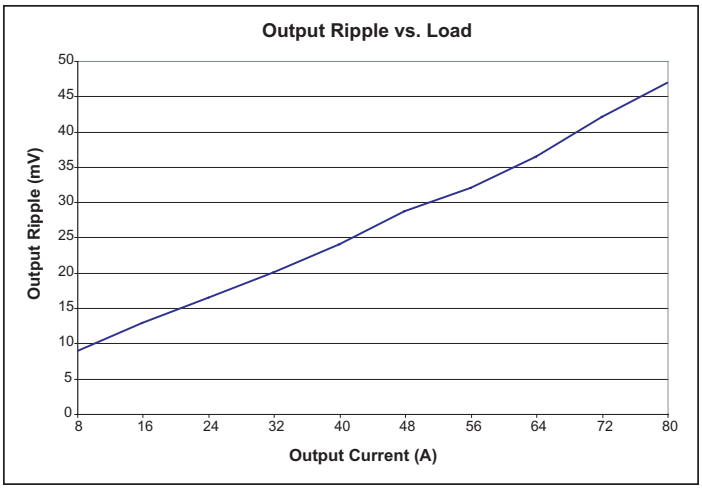


***Figure 10**— Output voltage ripple vs. output current at nominal line with no POL bypass capacitance.*

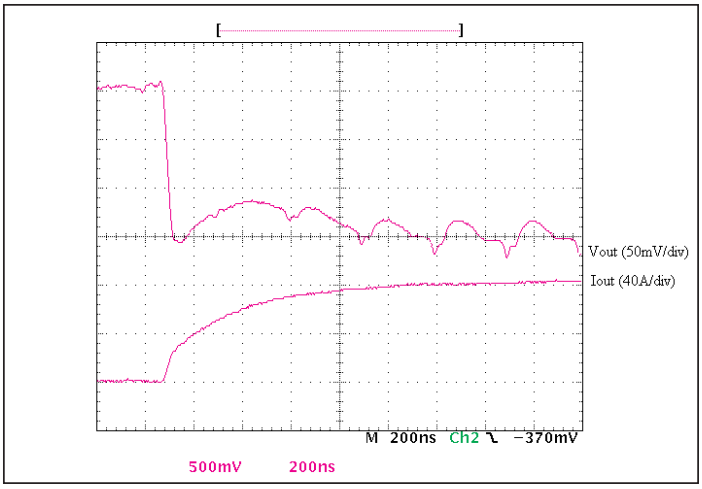


***Figure 11**— 0-80A step load change with 100 µF input capacitance and no output capacitance.*

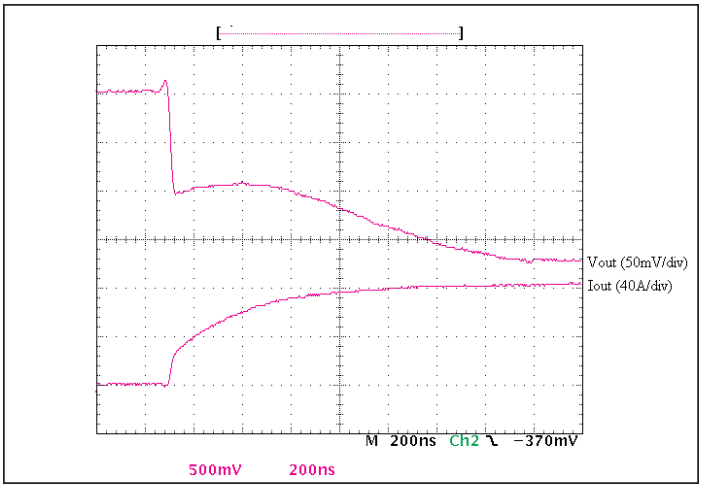


***Figure 12**— 0-80A step load change with 100 µF input capacitance and 100 µF output capacitance.*

GENERAL

Parameter	Min	Typ	Max	Unit	Note
MTBF					
MIL-HDBK-217F		3.6		Mhrs	25°C, GB
Telcordia TR-NT-000332		4.2		Mhrs	
Telcordia SR-332		TBD		hrs	
Demonstrated		TBD		hrs	
Isolation specifications					
Voltage	1,500			Vdc	Input to Output
Capacitance		5,100	6,000	pF	Input to Output
Resistance	10			MΩ	Input to Output
Agency approvals (pending)		cTÜVus			UL/CSA 60950, EN 60950
		CE Mark			Low voltage directive
Mechanical parameters					See mechanical drawing, Figs.16 and 18
Weight		0.43 / 12.25		oz / g	
Dimensions					
Length		1.26 / 32		in / mm	
Width		0.85 / 21.5		in / mm	
Height		0.24 / 6		in / mm	

Auxiliary Pins (Conditions are at nominal line, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Primary Control (PC)					
DC voltage	4.8	5.0	5.2	V	
Module disable voltage	2.4	2.5		V	
Module enable voltage		2.5	2.6	V	
Current limit	2.4	2.5	2.9	mA	Source only
Enable delay time		300	450	µs	See Fig.2
Disable delay time		4	10	µs	
Temperature Monitor (TM)					
27°C setting	2.95	3.00	3.05	V	Operating junction temperature
Temperature coefficient		10		mV/°C	
Full range accuracy	-5		5	°C	Operating junction temperature
Current limit	100			µA	Source only

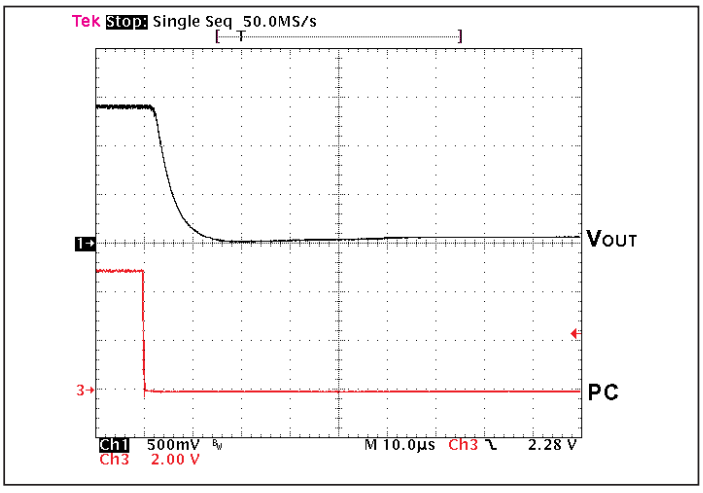


Figure 13— *VOUT at full load vs. PC disable*

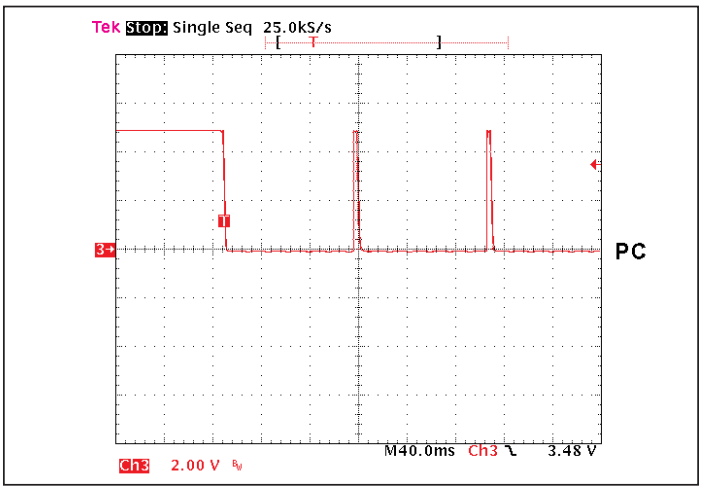


Figure 14— *PC signal during fault*

THERMAL

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Over temperature shutdown	125	130	135	°C	Junction temperature
	Thermal capacity		0.61		Ws/°C	
$R_{\theta JC}$	Junction-to-case thermal impedance		1.1		°C/W	
$R_{\theta JB}$	Junction-to-BGA thermal impedance		2.1		°C/W	
$R_{\theta JA}$	Junction-to-ambient [1]		6.5		°C/W	
$R_{\theta JA}$	Junction-to-ambient [2]		5.0		°C/W	

Notes

1. V048K015T80 surface mounted in-board to a 2" x 2" FR4 board, 4 layers 2 oz Cu, 300 LFM.
2. V048L015T80 (0.25"H integral Pin Fins) surface mounted on FR4 board, 300 LFM.

V•I CHIP STRESS DRIVEN PRODUCT QUALIFICATION PROCESS

Test	Standard	Environment
High Temperature Operational Life (HTOL)	JESD22-A-108-B	125°C, Vmax, 1,008 hrs
Temperature cycling	JESD22-A-104B	-55°C to 125°C, 1,000 cycles
High temperature storage	JESD22-A-103A	150°C, 1,000 hrs
Moisture resistance	JESD22-A113-B	Moisture sensitivity Level 4
Temperature Humidity Bias Testing (THB)	EIA/JESD22-A-101-B	85°C, 85% RH, Vmax, 1,008 hrs
Pressure cooker testing (Autoclave)	JESD22-A-102-C	121°C, 100% RH, 15 PSIG, 96 hrs
Highly Accelerated Stress Testing (HAST)	JESD22-A-110B	130°C, 85% RH, Vmax, 96 hrs
Solvent resistance/marking permanency	JESD22-B-107-A	Solvents A, B & C as defined
Mechanical vibration	JESD22-B-103-A	20g peak, 20-2,000 Hz, test in X, Y & Z directions
Mechanical shock	JESD22-B-104-A	1,500g peak 0.5 ms pulse duration, 5 pulses in 6 directions
Electro static discharge testing – human body model	EIA/JESD22-A114-A	Meets or exceeds 2,000 Volts
Electro static discharge testing – machine model	EIA/JESD22-A115-A	Meets or exceeds 200 Volts
Highly Accelerated Life Testing (HALT)	Per Vicor Internal Test Specification	Operation limits verified, destruct margin determined
Dynamic cycling	Per Vicor internal test specification	Constant line, 0-100% load, -20°C to 125°C

V•I CHIP BALL GRID ARRAY INTERCONNECT QUALIFICATION

Test	Standard	Environment
BGA Daisy-Chain thermal cycling	IPC-SM-785 IPC-9701	TC3, -40 to 125°C at <10 °C/min, 10 min dwell time
Ball shear	IPC-9701 IPC J-STD-029	No failure through intermetallic
Bend test	IPC J-STD-029	Deflection through 4 mm

+IN/-IN DC VOLTAGE PORTS

The VTM input should not exceed the high end of the range specified. Be aware of this limit in applications where the VTM is being driven above its nominal output voltage. An internal over/under voltage lock-out function prevents operation outside of the specified input range. The VTM will turn on when the input voltage rises above the under voltage lock-out specified. If the input voltage exceeds the over voltage lock-out, the VTM will shutdown until the over voltage fault clears. The VTM does not have internal input reverse polarity protection. Adding a properly sized diode in series with the positive input or a fused reverse-shunt diode will provide reverse polarity protection.

A minimum 8 µF Aluminum Electrolytic capacitor should be applied at the input of the VTM. Additional capacitance, e.g. 100 µF, may be added to enhance dynamic performance or to compensate for high source impedance.

SG – Signal Ground

The Signal Ground (SG) pin provides a Kelvin return for the Primary Control (PC) and Temperature Monitor (TM) ports. Even though the SG pin is referenced to the –IN of the VTM, it should not be used as an additional –IN connection.

PC – Primary Control

The Primary Control (PC) pin is a multifunction pin for controlling the VTM as follows:

Enable/Disable – If the PC is left floating or is pulled to logic HI, the VTM output is enabled. To disable the output, the PC pin must be pulled lower than 2.4 V, referenced to SG. Optocouplers, open collector transistors or relays can be used to control the PC pin. The PC port should not be toggled at a rate higher than 1 Hz.

Primary Auxiliary Supply – The PC port can source up to 2.4 mA at 5 Vdc.

Alarm – The VTM contains watchdog circuitry that monitors output overload, input over voltage, input under voltage, or excessive internal temperature. In response to any of these abnormal conditions the PC port will toggle as shown in Figure 14.

TM – Temperature Monitor

The Temperature Monitor (TM) provides a linear output proportional to the internal temperature of the VTM. At 300ºK (+27ºC) the TM output is 3.0 V and varies 10 mV/ºC. TM accuracy is +/-5ºC if the SG pin is used as the ground return of the TM signal. This feature is useful for validating the thermal design of the system as well as monitoring the VTM temperature in the final application.

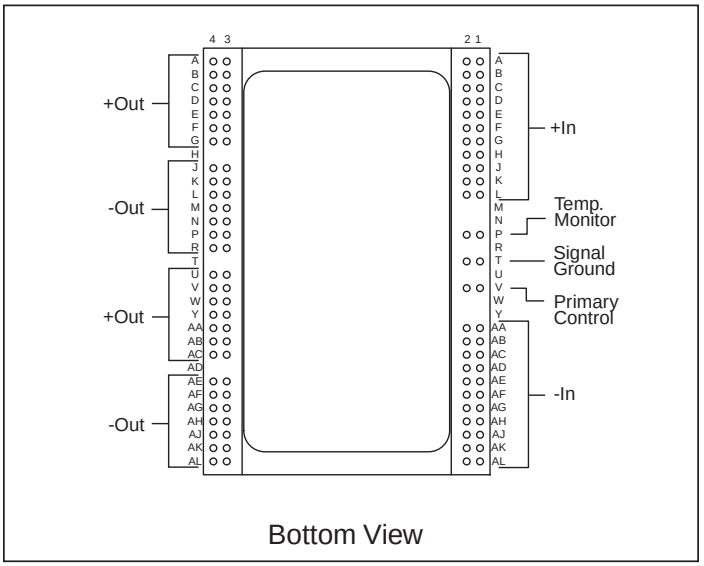


Figure 15*—VTM BGA configuration*

Signal Name	BGA Designation
+In	A1-L1, A2-L2
–In	AA1-AL1, AA2-AL2
TM	P1, P2
SG	T1, T2
PC	V1, V2
+Out	A3-G3, A4-G4, U3-AC3, U4-AC4
–Out	J3-R3, J4-R4, AE3-AL3, AE4-AL4

+OUT/-OUT DC Voltage Output Ports

The output (+OUT) and output return (-OUT) are through two sets of contact locations. The respective +OUT and –OUT groups must be connected in parallel with as low an interconnect resistance as possible. Within the specified input voltage range, the Level 1 DC behavioral model shown in Figure 27 defines the output voltage of the VTM. The current source capability of the VTM is shown in the specification table.

To take full advantage of the VTM, the user should note the low output impedance of the device as shown in Figure 9. The low output impedance provides fast transient response without the need for bulk POL capacitance. Limited-life electrolytic capacitors required with conventional converters can be reduced or even eliminated, saving cost and valuable board real estate.

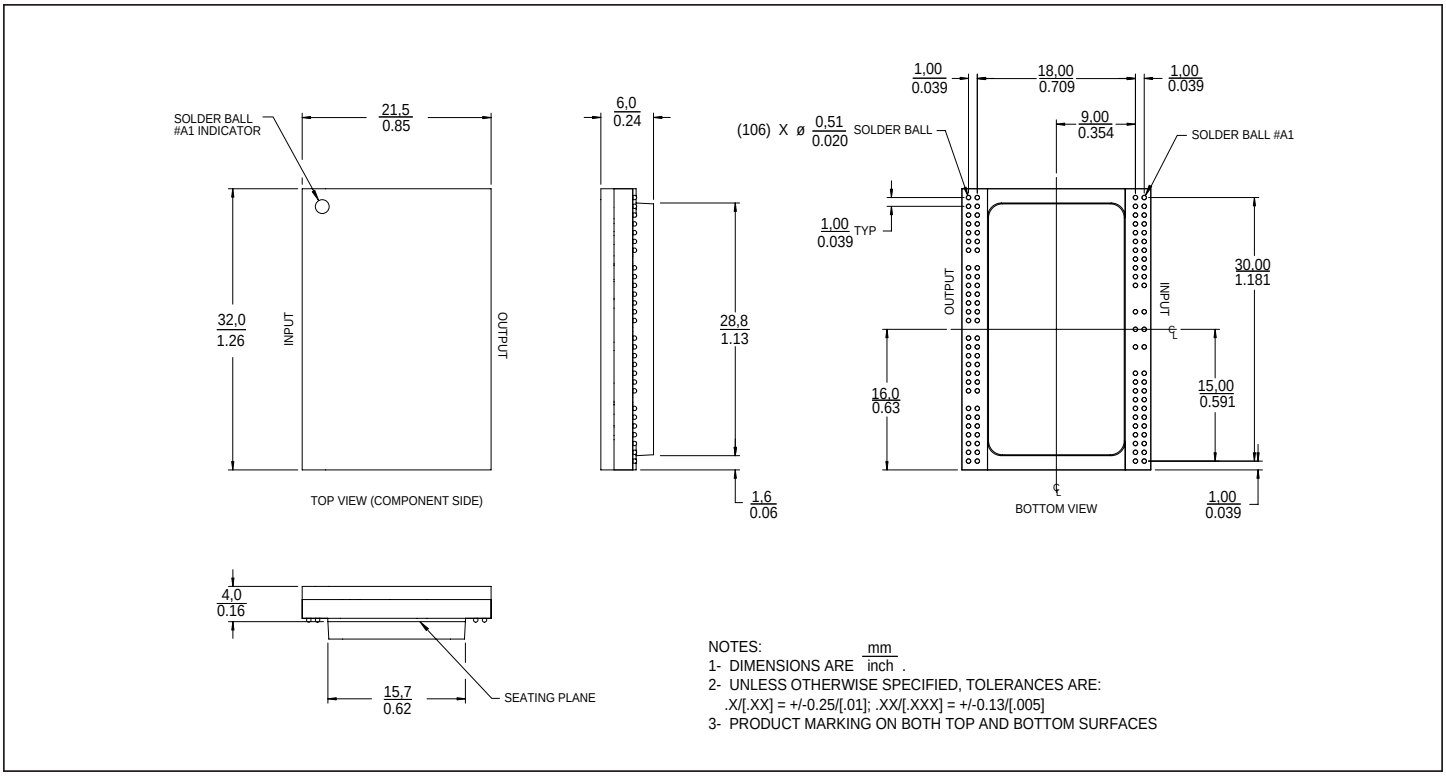


Figure 16*—VTM BGA mechanical outline; In-board mounting*

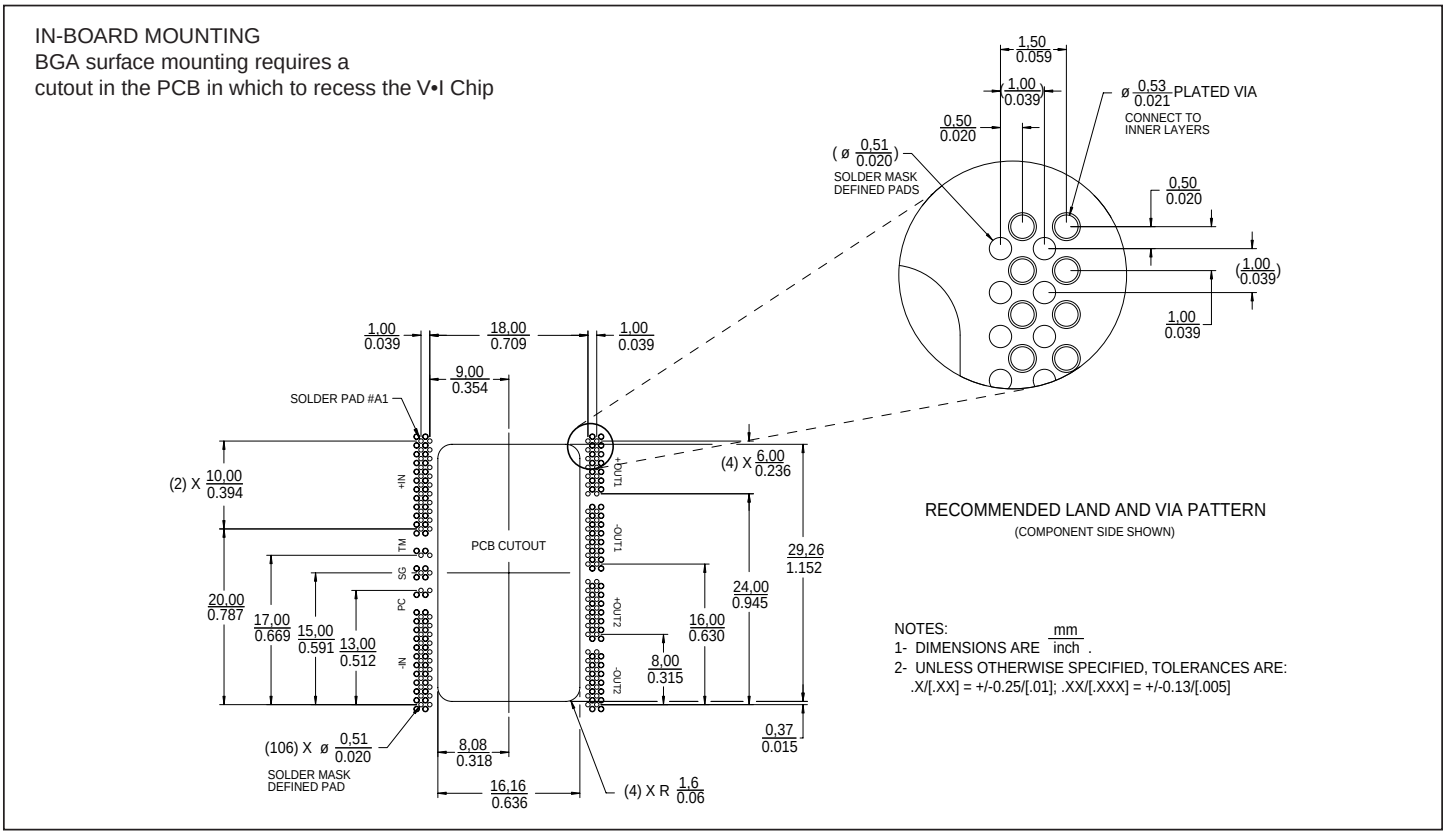


Figure 17*— VTM BGA PCB land/VIA layout information; In-board mounting*

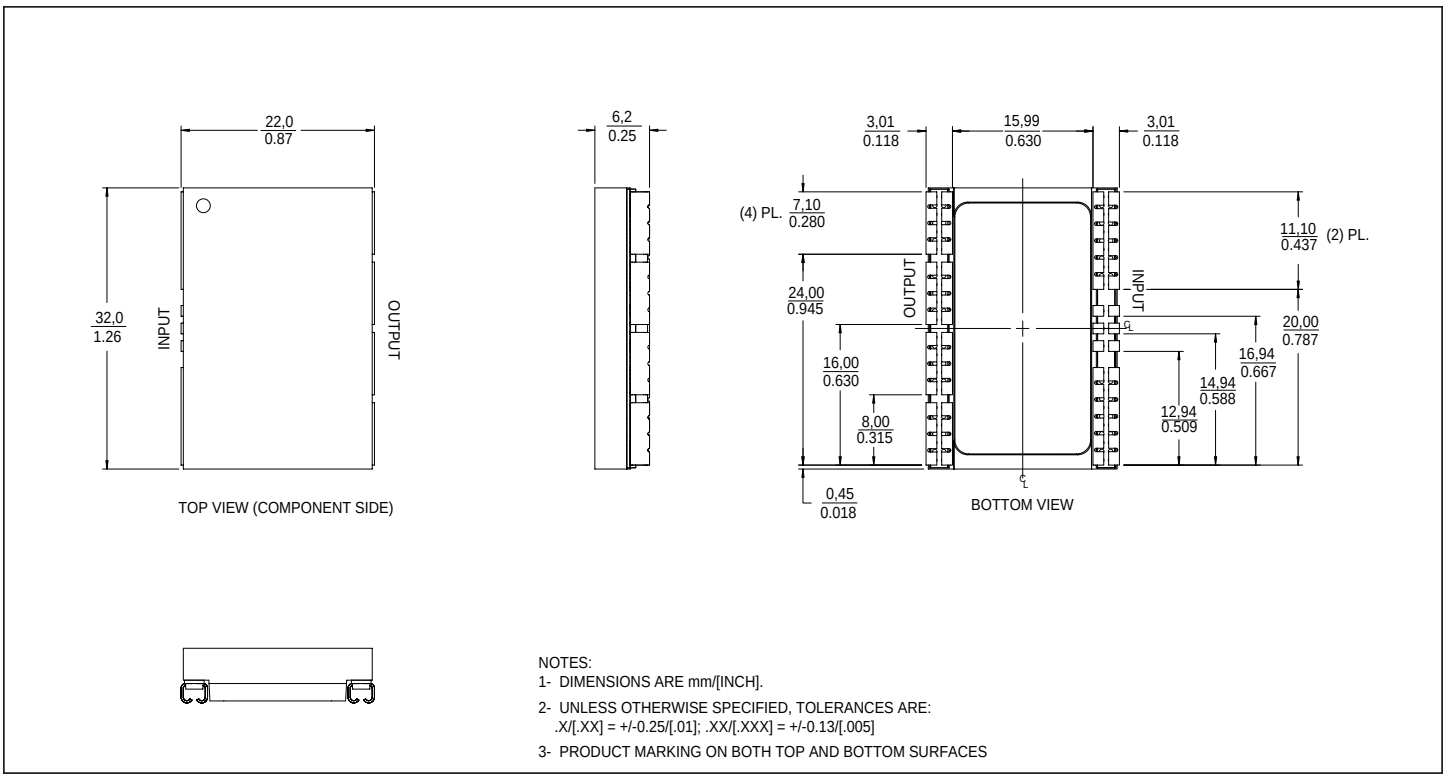


Figure 18*—VTM J-lead mechanical outline; On-board mounting*

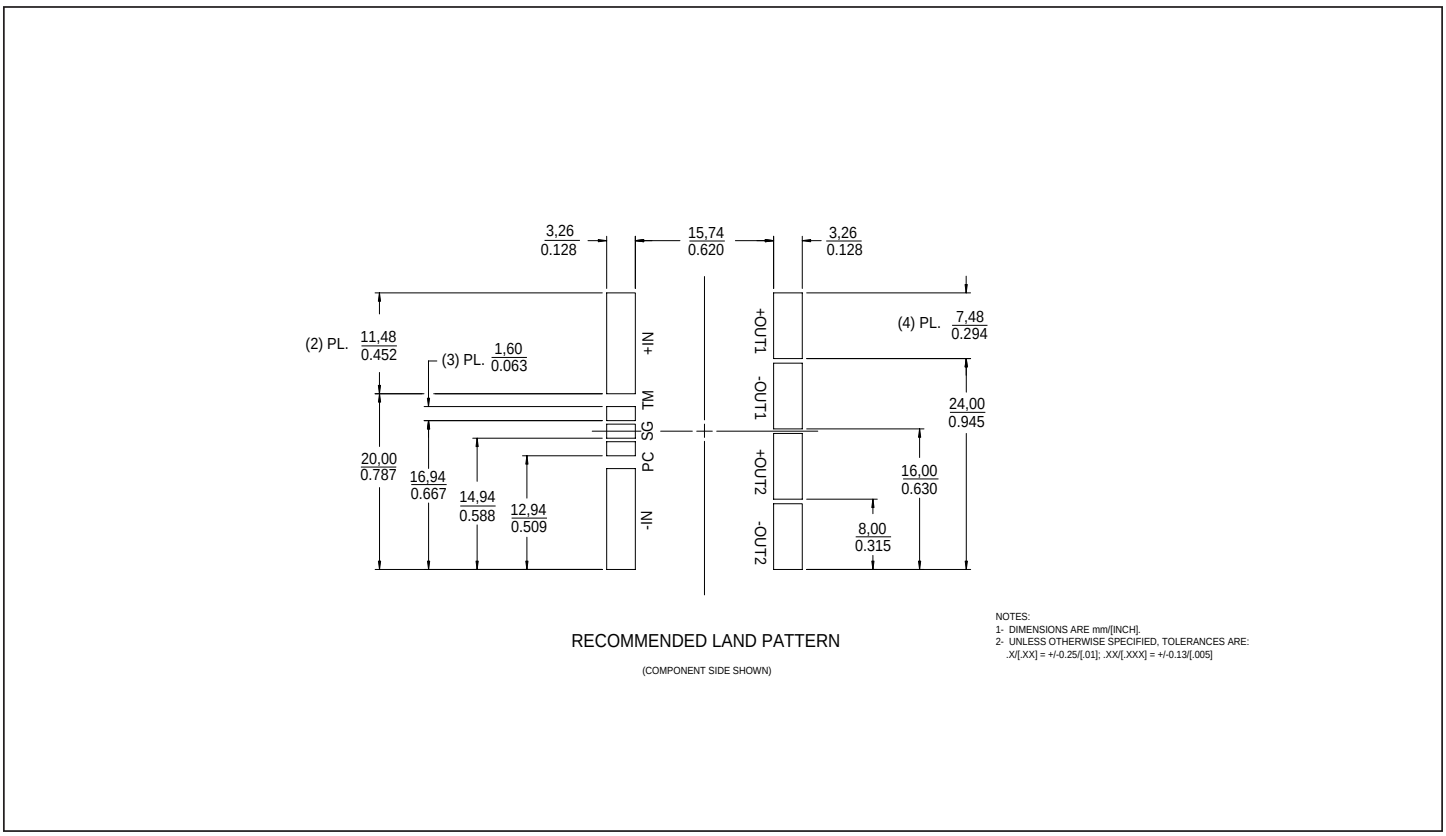


Figure 19*— VTM J-lead PCB land layout information; On-board mounting*

■ V•I Chip VOLTAGE TRANSFORMATION MODULE PART NUMBERING

V — *Voltage Transformation Module*

048 — *Input Voltage Designator*

K — *Configuration Options*
- *F = On-board (Fig.21)*
- *G = On-board with 0.25" Integral Pin Fins (Fig.23)*
- *K = In-board (Fig.20)*
- *L = In-board with 0.25" Integral Pin Fins (Fig.22)*

015 — *Output Voltage Designator (=V_{OUT} x10)*

T — *Product Grade Temperatures (°C)*

Grade	Storage	Operating
T	-40 to150	-40 to125

80 — *Output Current Designator (=I_{OUT})*

■ CONFIGURATION OPTIONS

CONFIGURATION	IN-BOARD*	ON-BOARD*	IN-BOARD WITH 0.25" PIN FINS**	ON-BOARD WITH 0.25" PIN FINS**
Effective Current Density	480 A/in^3	320 A/in^3	178 A/in^3	144 A/in^3
Junction-Board Thermal Resistance	2.1 °C/W	2.4 °C/W	2.1 °C/W	2.4 °C/W
Junction-Case Thermal Resistance	1.1 °C/W	1.1 °C/W	N/A	N/A
Junction-Ambient Thermal Resistance 300LFM	6.5 °C/W	6.8 °C/W	5.0 °C/W	5.0 °C/W
VTM Model No.	V048K015T80	V048F015T80	V048L015T80	V048G015T80

*Surface mounted to a 2" x 2" FR4 board, 4 layers 2 oz Cu

**Pin Fin heat sink also available as a separate item

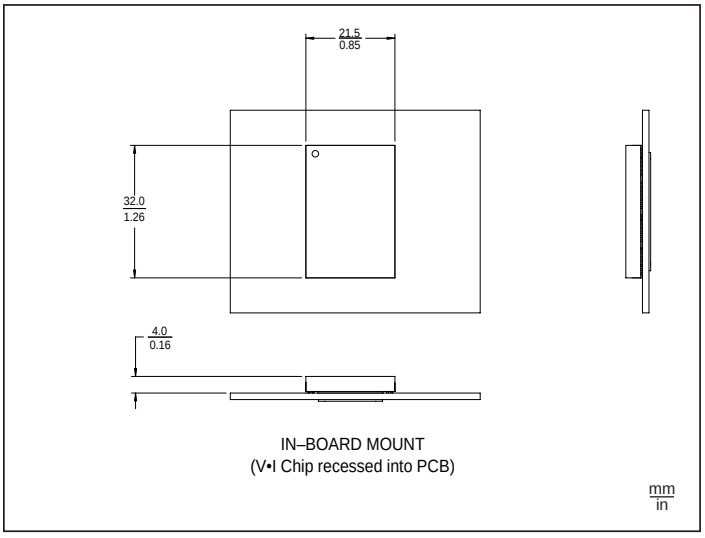


Figure 20*—In-board mounting – package K*

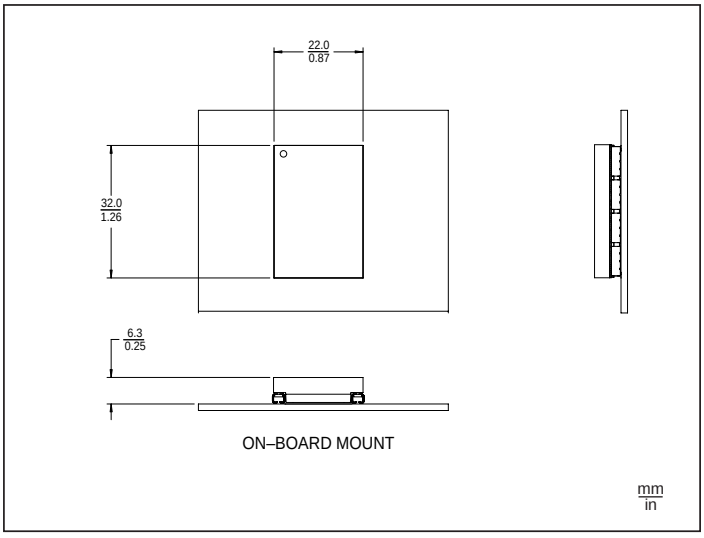


Figure 21*—On-board mounting – package F*

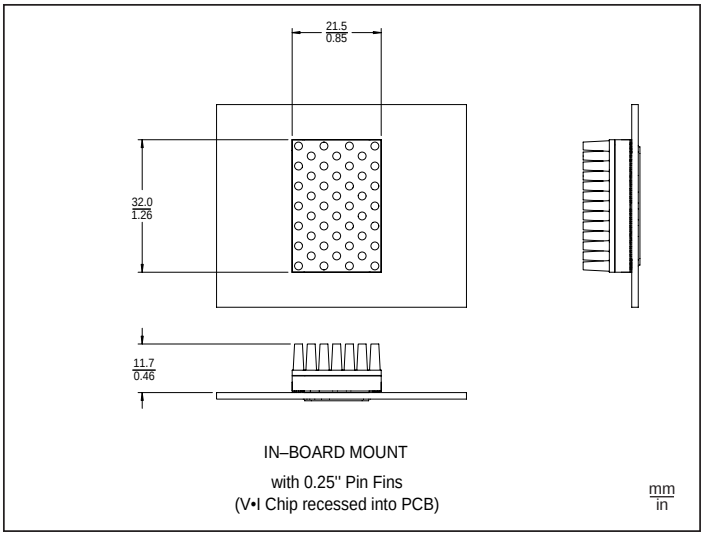


***Figure 22**— In-board with Pin Fins – package L*

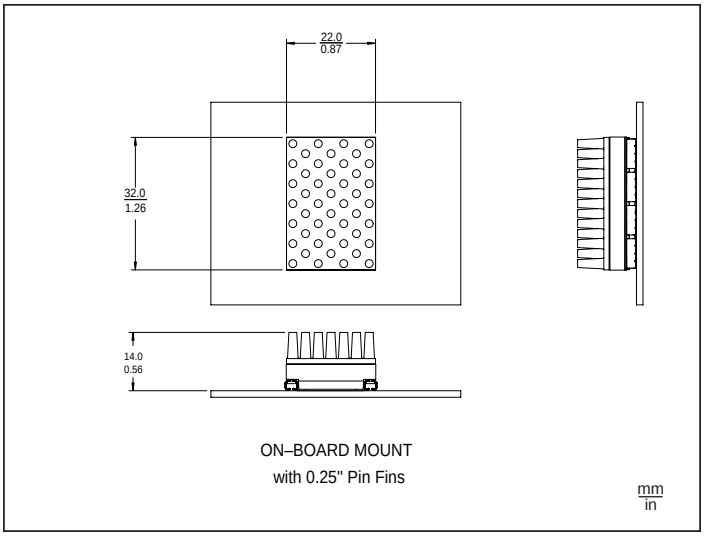
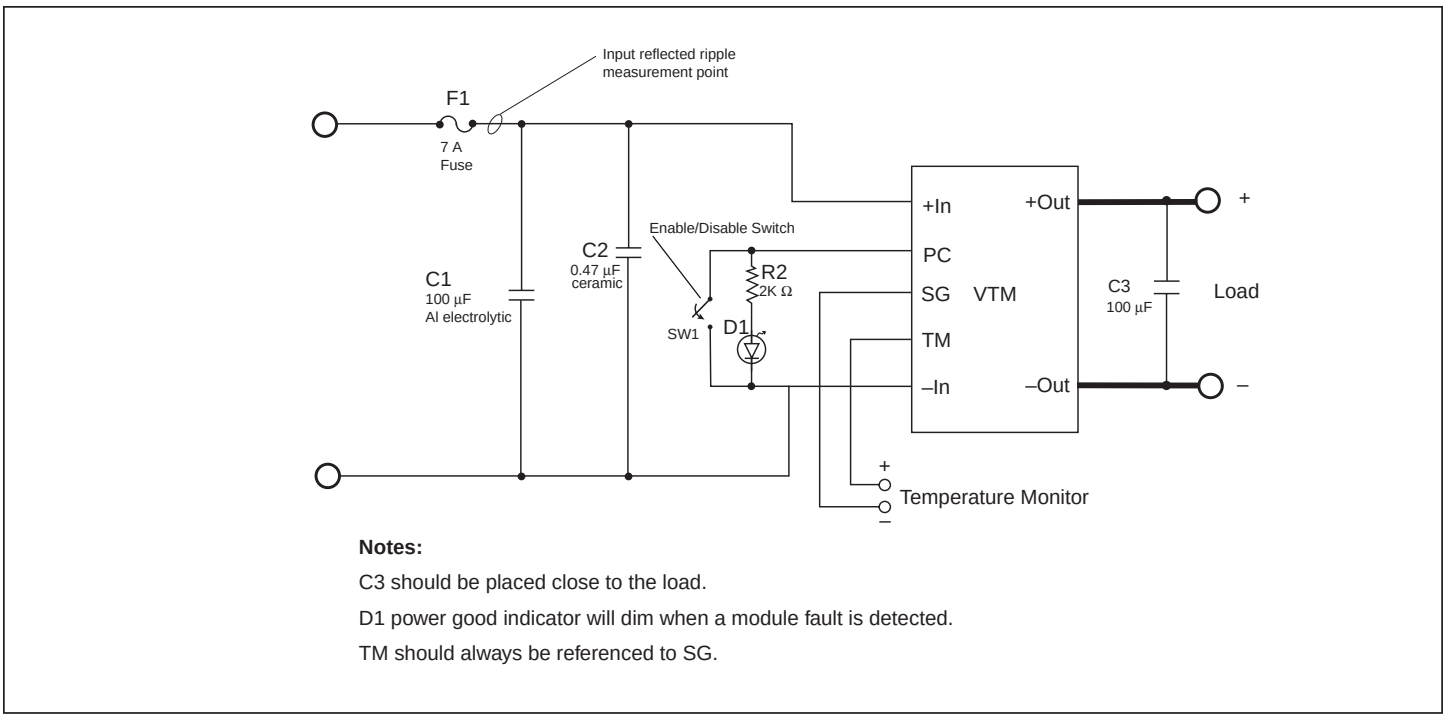


***Figure 23**— On-board with Pin Fins – package G*



Notes:

C3 should be placed close to the load.

D1 power good indicator will dim when a module fault is detected.

TM should always be referenced to SG.

***Figure 24**—VTM test circuit*

Application Note

Parallel Operation

In applications requiring higher current or redundancy, VTMs can be operated in parallel without adding control circuitry or signal lines. To maximize current sharing accuracy, it is imperative that the source and load impedance on each VTM in a parallel array be equal.

To achieve matched impedances, dedicated power planes within the PC board should be used for the output and output return paths to the array of paralleled VTMs. This technique is preferable to using traces of varying size and length.

The VTM power train and control architecture allow bi-directional power transfer when the VTM is operating within its specified ranges. Bi-directional power processing improves transient response in the event of an output load dump. The VTM may operate in reverse, returning output power back to the input source. It does so efficiently.

Thermal Management

The high efficiency of the VTM results in low power dissipation minimizing temperature rise, even at full output current. The heat generated within the internal semiconductor junctions is coupled through very low thermal resistances, $R\theta_{JC}$ and $R\theta_{JB}$ (see Figure 25), to the PC board allowing flexible thermal management.

CASE 1 Convection via optional Pin Fins to air (Pin Fins available mounted to the V•I Chip or as a separate item.)

In an environment with forced convection over the surface of a PCB with 0.4" of headroom, a VTM with Pin Fins offers a simple thermal management option. The total Junction to Ambient thermal resistance of a surface mounted V048L015T80 is 5 ºC/W in 300 LFM airflow, (see Figure 26). At full rated current (80A) the VTM dissipates approximately 11 W. Power dissipation curves in Figure 6 show typical dissipation at different output currents.

CASE 2 Conduction to the PC board

The low thermal resistance, Junction to BGA, allows the use of the PC board as a means of removing heat from the VTM. Convection from the PC board to ambient, or conduction to a cold plate, enable flexible thermal management options. In this case, the VTM can be used without the Pin Fin option, allowing a system designer to take full advantage of the VTM's low profile.

With a VTM mounted on a 2.0 in^2 area of a multi-layer PC board with appropriate power planes resulting in 8 oz of effective copper weight, the Junction-to-ambient thermal resistance, $R\theta_{JA}$, is 6.5 ºC/W in 300 LFM of air. With a maximum junction temperature of 125ºC and 11 W of dissipation at full current of 80 A, the resulting temperature rise of 72ºC allows the VTM to operate at full rated current up to a 53ºC ambient temperature. See thermal resistance table on page 1 for additional details on this thermal management option.

Adding low-profile heat sinks to the PC board can lower the thermal resistance of the PC board surrounding the VTM. This option is useful in environments that cannot accommodate the height of the Pin Fin option.

Additional cooling may be added by coupling a cold plate to the PC board with low thermal resistance stand offs.

CASE 3 Combined direct convection to the air and conduction to the PC board.

A combination of cooling techniques that utilize the power planes and dissipation to the air will also reduce the total thermal impedance. This is the most effective cooling method.To estimate the total effect of the combination, treat each cooling branch as one leg of a parallel resistor network.

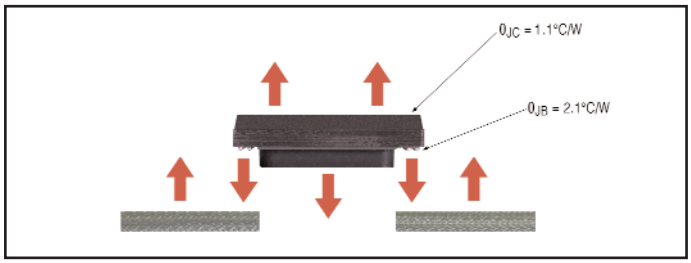


Figure 25*—Thermal resistance*

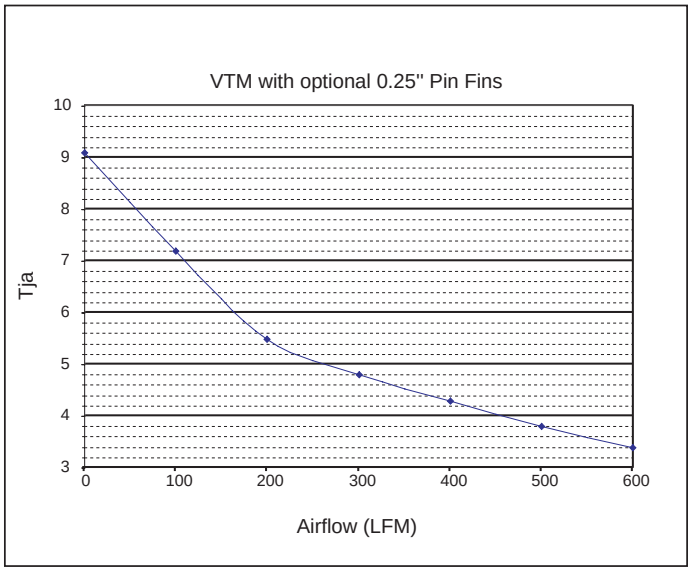


Figure 26*—Junction-to-ambient thermal resistance of VTM with 0.25" Pin Fins. (Pin Fins are available as an option for the V•I Chip package.)*

■ V•I Chip VTM LEVEL 1 DC BEHAVIORAL MODEL for 48V to 1.5V, 80A

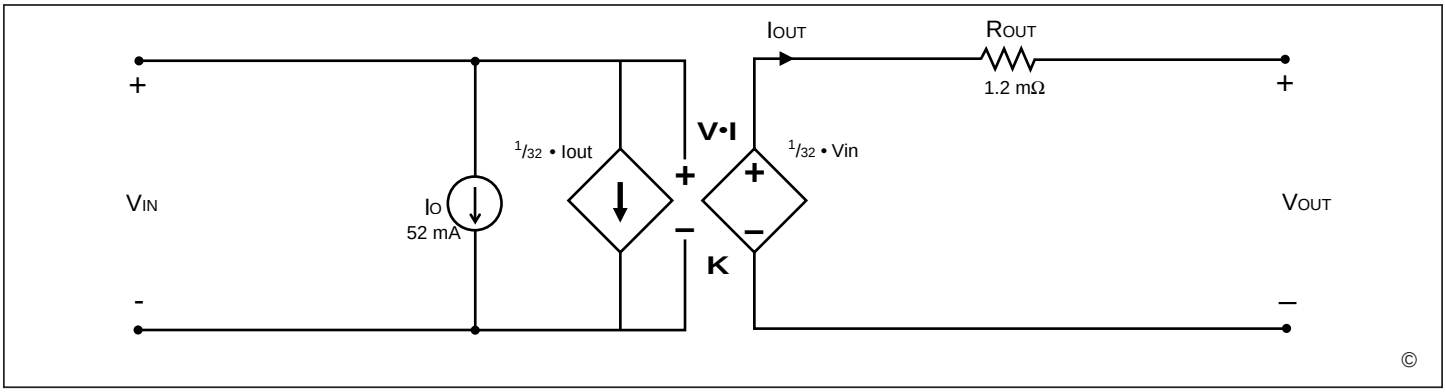


Figure 27*—This model characterizes the DC operation of the V•I Chip VTM, including the converter transfer function and its losses. The model enables estimates or simulations of output voltage as a function of input voltage and output load, as well as total converter power dissipation or heat generation.*

■ V•I Chip VTM LEVEL 2 TRANSIENT BEHAVIORAL MODEL for 48V to 1.5V, 80A

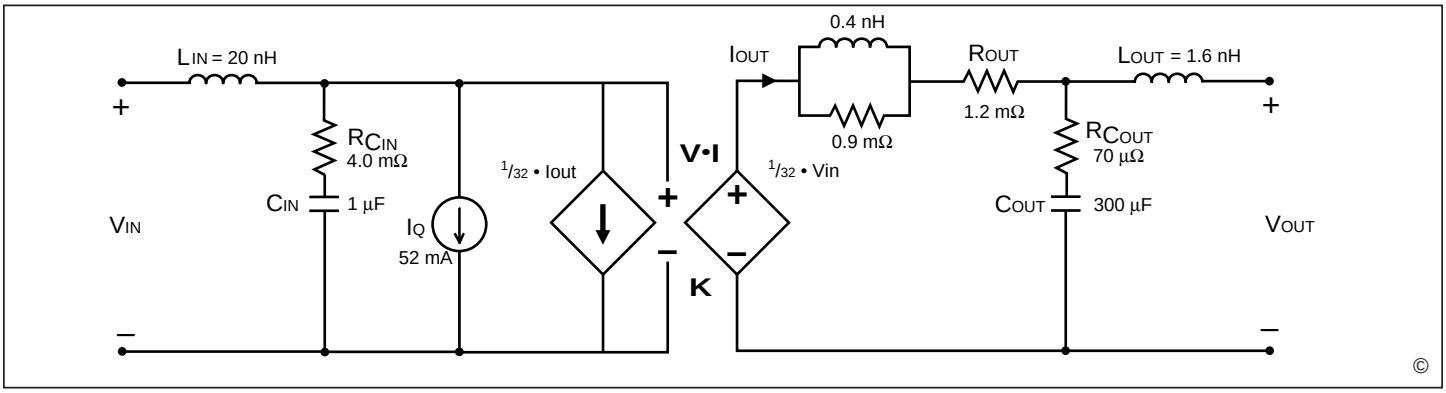


Figure 28*—This model characterizes the AC operation of the V•I Chip VTM including response to output load or input voltage transients or steady state modulations. The model enables estimates or simulations of input and output voltages under transient conditions, including response to a stepped load with or without external filtering elements.*

Using the VTM with a controlled DC source

The VTM may be applied to provide a low output voltage at high current from a controlled 48V source. The overall efficiency of a power system based on Factorized Power Architecture, using VTMs, exceeds the efficiency of power systems based on Distributed Power Architecture, using DC-DC converters, or the Intermediate Bus Architecture, using non-isolated POL converters.

The fast VTM transient response eliminates the need for large amounts of capacitance at the point of load (POL). Energy storage capacitors may be added at the input of the VTM, where they are more effective. Capacitors used at the VTM input get reflected at the output multiplied by $(1/K)^2$. For example, a 1 µF capacitor placed at the input of a VTM with a $K=1/32$ has the effective energy storage of 1,000 µF at its output. Since the VTM has a 1 MHz bandwidth, only high frequency decoupling with ceramic capacitors is necessary at the POL, even with fast switching, dynamic loads.

The following describes typical applications for a VTM powered from a 48 V source, such as DC-DC converters or PRMs.

Open Loop Application

In an open loop implementation, the VTM is connected at the output of a DC-DC converter or controlled voltage source (Fig. 29). The no load output of the VTM is the voltage of the source multiplied by the K factor of the VTM. The K factor of the V048K015T80 is $1/32$; hence, at 48 Vdc from the source, the VTM's output is $1/32 \cdot 48V = 1.5$ Vdc. The output of the VTM can be set over the range of 1.0 to 1.8 Vdc, at no load, and 0.9 to 1.7 V, at full load, by controlling the V_f of the source from 32 V to 57.6 V.

The VTM has a very low output resistance, R_{OUT}. This will cause the output voltage to change slightly with load current unless R_{OUT} is compensated by a control loop.Without compensation, the output voltage of the VTM can be expressed as follows:

$$V_{OUT} = K \cdot V_f - R_{OUT} \cdot I_{LOAD}$$

where V_f is the factorized bus input voltage to the VTM.

For the V048K015T80, this equation becomes:

$$V_{OUT} = 1/32 \cdot V_f - 0.0013 \cdot I_{LOAD}$$

The voltage of the source may be set to a value that produces the desired VTM output voltage at the nominal load current:

$$V_f = (V_{OUT} + R_{OUT} \cdot I_{NOM})/K ;$$
$$= 32 \cdot (V_{OUT} + 0.0013 \cdot I_{NOM})$$

The voltage of the source may be set by using trim up (Ru) or trim down (Rd) resistors or it may be actively controlled by a suitable voltage applied at a source voltage control node (SC).

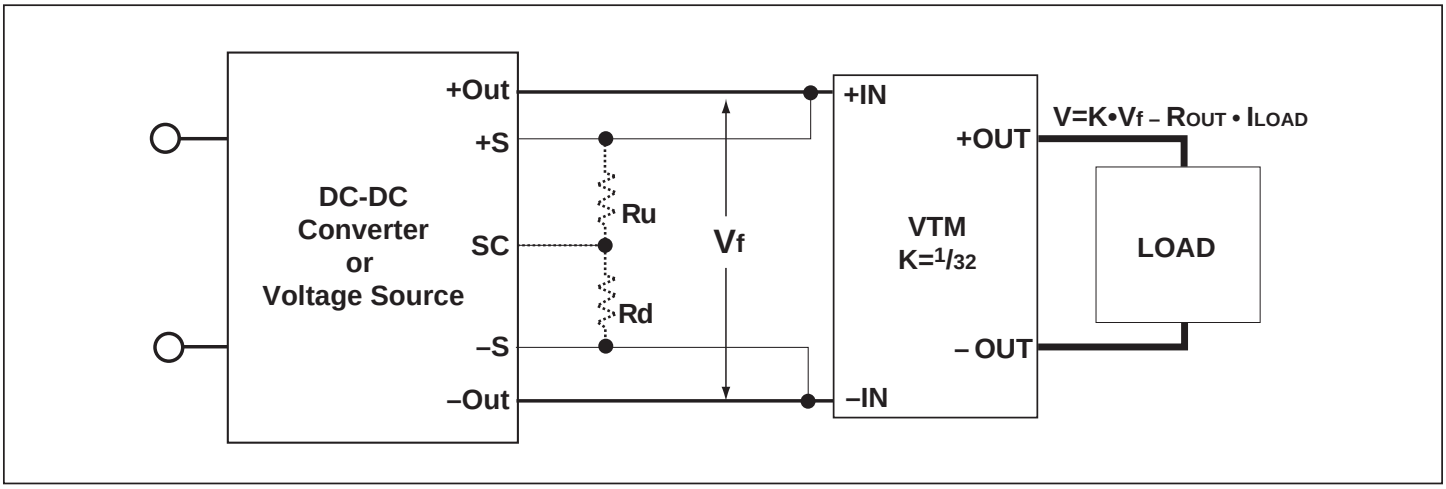


Figure 29*—Open loop operation with DC-DC converter or other controlled voltage source.*

Closed Loop Application

To compensate for the effect of the VTM's output resistance on the load voltage as a function of load current, a feedback loop can be implemented as shown in Fig.30.

VTMs can also be used in a Factorized Power Architecture system with VID control of the output voltage as a faster, more efficient alternative to multiphase VRMs as shown in Fig.31.

Off-line DC-DC converters, telecom input DC-DC converters and switching regulators may be adapted, through a suitable interface, to provide the PRM function.

High efficiency, high density PRMs in V•I Chip packages are in development.

Please consult with Vicor application engineering for specific application information.

Email:apps@vicr.com; phone: 1-800-927-9474

■ FPA Application Example

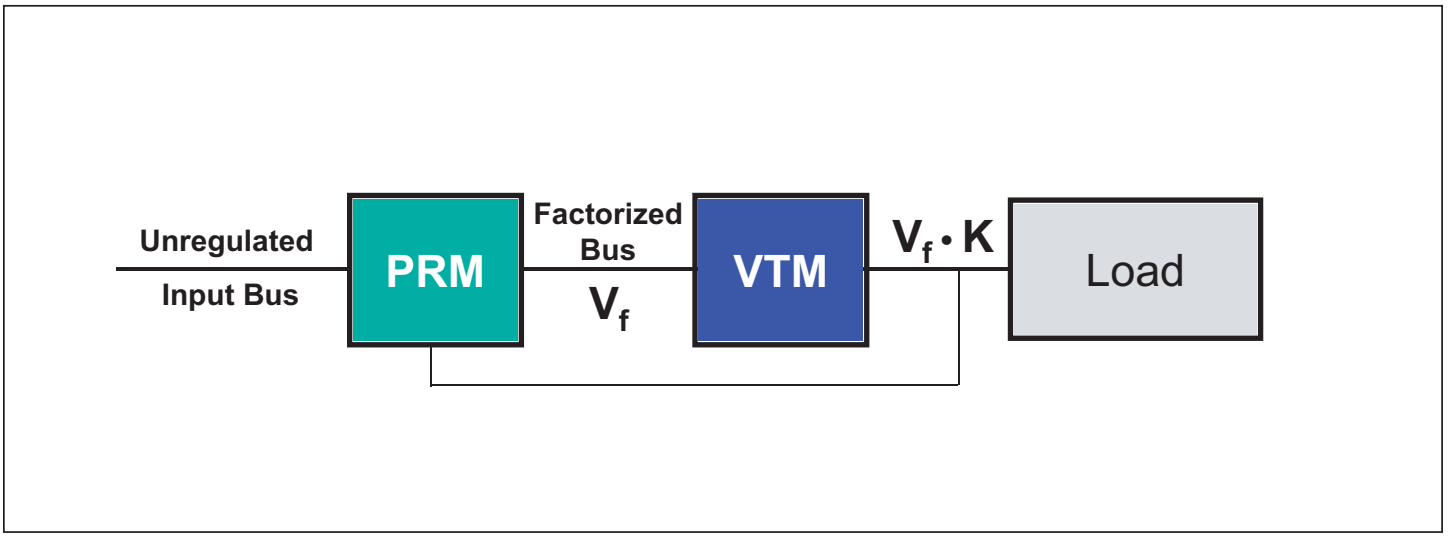


***Figure 30**—Basic Factorized Power Architecture with Pre-Regulation Module (PRM) and VTM*

■ FPA Application Example

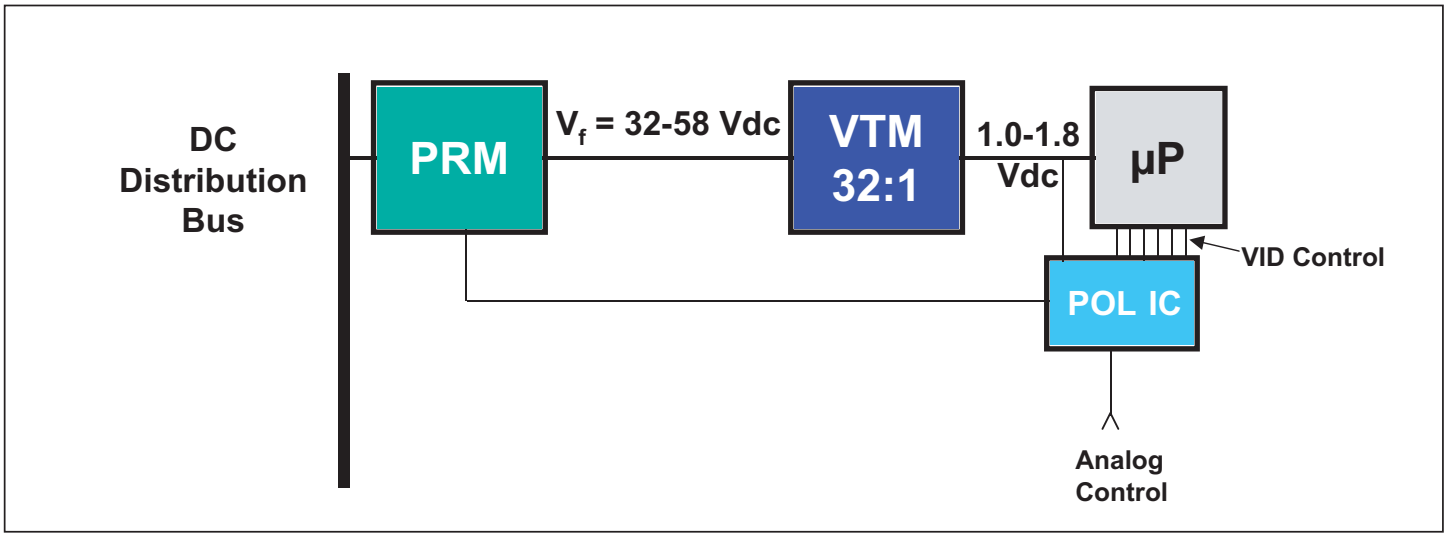


***Figure 31**—PRM and VTM, Closed loop with VID Controller*

V•I Chip Handling and Solderability

The product should remain in its package in a dry environment until ready for use.

The following table shows the soldering requirements for both the BGA in-board surface mount package and the J-lead on-board surface mount package.

The reflow process should use industry standard Surface Mount Technology (SMT) conditions. The exact conditions will depend upon the solder paste manufacturer's recommendations. Under no circumstance should the case temperature exceed 208°C. Refer to Fig.32 for a suggested thermal profile.

	BGA Package	J-Lead Package
Solder Paste	63/37 "No Clean"*	63/37 "No Clean"
Stencil Thickness	4-6 mil	4-6 mil
Stencil Aperture	20 mil; 1:1 ratio	0.8-0.9:1 ratio
Placement	Within 50% of pad center	± 5 mil
Acceleration Rate	<500 in/sec^2	<500 in/sec^2

*Halide free water washable 63/37 Flux paste can be used for the BGA version package only. Please consult our Application Engineers for further information.

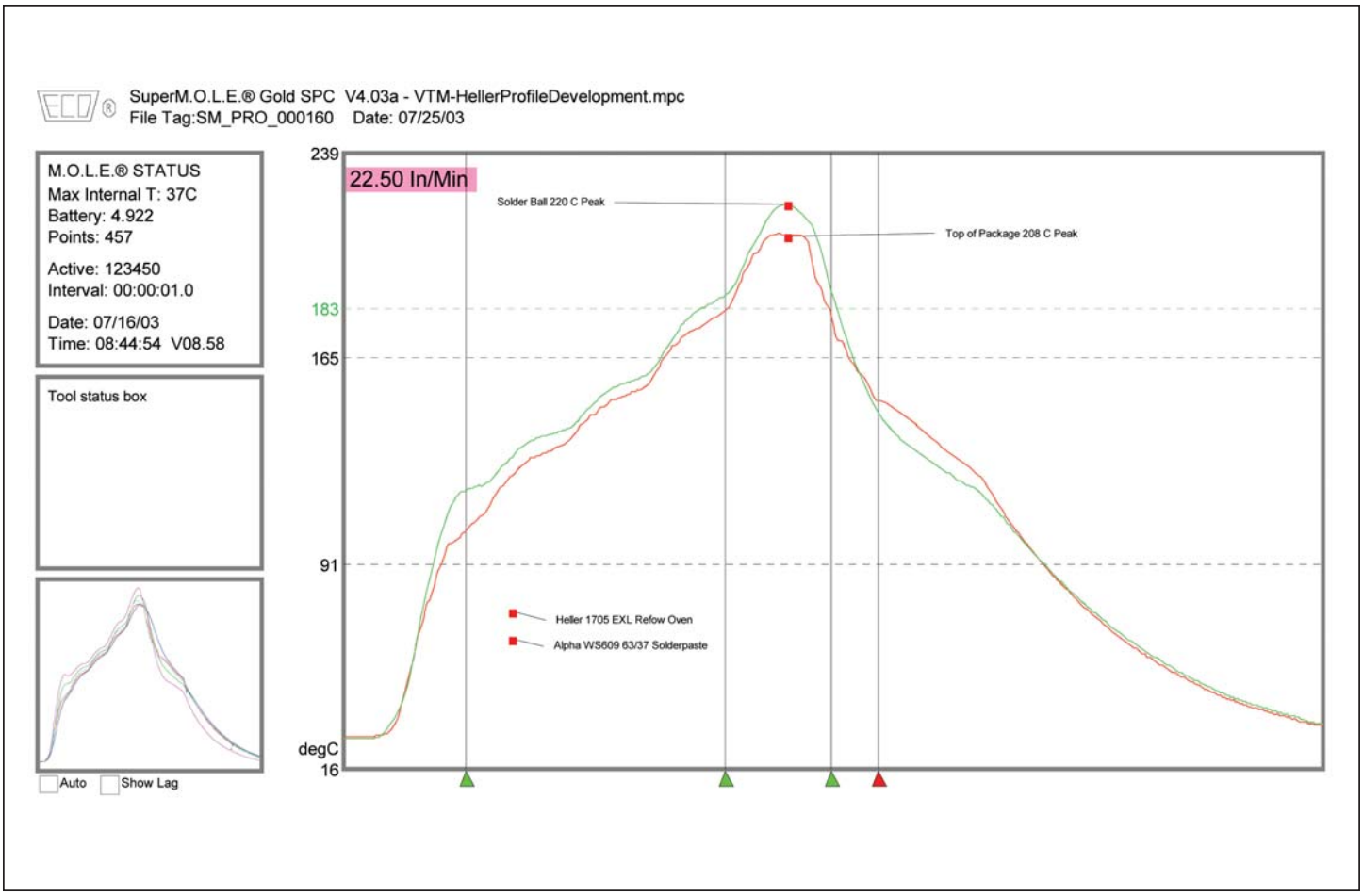


Figure 32*—Thermal profile diagram*

Application Note (continued)

Input Impedance Recommendations

To take full advantage of the VTM's capabilities, the impedance of the source (input source plus the PC board impedance) must be low over a range from DC to 5 MHz. The input of the VTM should be locally bypassed with a 8 µF low Q aluminum electrolytic capacitor. Additional input capacitance may be added to improve transient performance or compensate for high source impedance. The VTM has extremely wide bandwidth so the source response to transients is usually the limiting factor in overall output response of the VTM.

Anomalies in the response of the source will appear at the output of the VTM, multiplied by its K factor of $^{1}/_{32}$. The DC resistance of the source should be kept as low as possible to minimize voltage deviations on the input to the VTM. If the VTM is going to be operating close to the high or low limit of its input range, make sure input voltage deviations will not trigger the under or over voltage shutdown.

Input Fuse Recommendations

V•I Chips are not internally fused in order to provide flexibility in power system configuration. However, input line fusing of V•I Chips must always be incorporated within the power system. A fast acting fuse, such as NANO2 FUSE 451 Series 7 A 125 V, is required to meet safety agency Conditions of Acceptability. The input line fuse should be placed in series with the +IN port.

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NOTES

NOTES

Vicor's comprehensive line of power solutions includes high density AC-DC and DC-DC modules and accessory components, fully configurable AC-DC and DC-DC power supplies, and complete custom power systems.

Specifications are subject to change without notice.

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- The electrical and thermal utility of the V•I Chip package
- The design of the V•I Chip package
- The Power Conversion Topology utilized in the V•I Chip package
- The Control Architecture utilized in the V•I Chip package
- The Factorized Power Architecture.

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