



Rev. 1.6

UTRON

UT611024

128K X 8 BIT HIGH SPEED CMOS SRAM

REVISION HISTORY

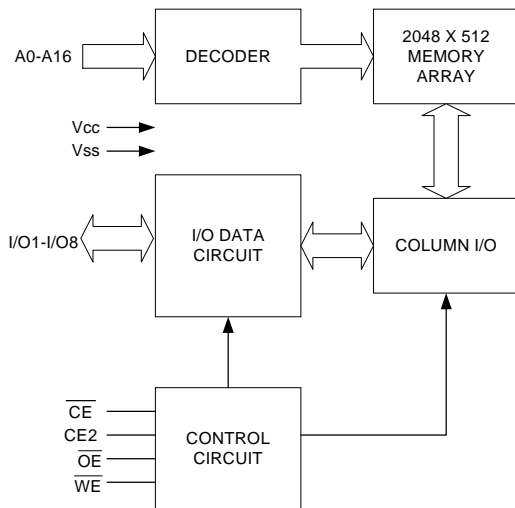
REVISION	DESCRIPTION	DATE
REV. 1.0	Original.	
REV. 1.1	Add Data Retention Section	Jan. 14,2000
REV. 1.2	NA	Nov. 01,2000
REV 1.4	1. The symbols CE1#,OE# and WE# are revised as $\overline{CE1}$, \overline{OE} and \overline{WE} 2. Delete data retention section.	Jun. 18,2001
REV 1.5	Add note in DC ELECTRICAL CHARACTERISTICS setion: $V_{IL}=-3.0V$ for pulse width less than 10ns.	Oct. 30,2001
REV 1.6	1.Add order information for lead free product 2.Revised timing read/write waveform	May. 22,2003



FEATURES

- Fast access time : 10/12/15ns (max.)
- Low operating power consumption:
100 mA (typical.)
- Single 5V power supply
- All inputs and outputs are TTL compatible
- Fully static operation
- Three state outputs
- Package : 32-pin 300 mil skinny PDIP
32-pin 300 mil SOJ
32-pin 8mmx20mm TSOP-1
32-pin 8mmx13.4mm STSOP

FUNCTIONAL BLOCK DIAGRAM



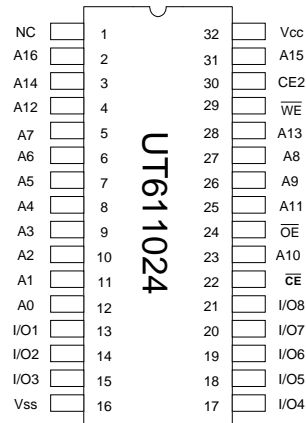
GENERAL DESCRIPTION

The UT611024 is a 1,048,576-bit high speed CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

The UT611024 is designed for high-speed system application. It is particularly suited for use in high speed and high density system applications.

The UT611024 operates from a signal 5V power supply and all inputs and outputs are fully TTL compatible

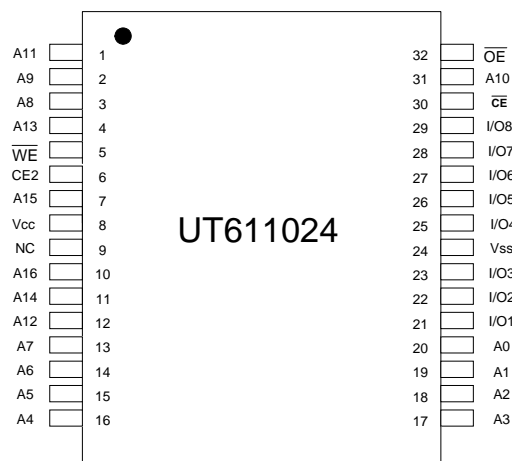
PIN CONFIGURATION



PDIP / SOJ

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
CE, CE2	Chip Enable Inputs
WE	Write Enable Input
OE	Output Enable Input
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection



STSOP / TSOP-1

**ABSOLUTE MAXIMUM RATINGS***

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}	V_{TERM}	-0.5 to +7.0	V
Operating Temperature	T_A	0 to +70	
Storage Temperature	T_{STG}	-65 to +150	
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 sec)	T_{solder}	260	

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE	CE2	OE	WE	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	I_{SB} , I_{SB1}
Standby	X	L	X	X	High - Z	I_{SB} , I_{SB1}
Output Disable	L	H	H	H	High - Z	I_{CC}
Read	L	H	L	H	D_{OUT}	I_{CC}
Write	L	H	X	L	D_{IN}	I_{CC}

Note: H = V_{IH} , L = V_{IL} , X = Don't care.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_A = 0$ to 70)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	
Input High Voltage	V_{IH}		2.2	$V_{CC} + 0.5$	V	
Input Low Voltage	V_{IL}		-0.5	0.8	V	
Input Leakage Current	I_{LI}	V_{SS} V_{IN} V_{CC}	-1	1	μA	
Output Leakage Current	I_{LO}	V_{SS} $V_{I/O}$ V_{CC} , $\overline{CE} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $WE = V_{IL}$	-1	1	μA	
Output High Voltage	V_{OH}	$I_{OH} = -4mA$	2.4	-	V	
Output Low Voltage	V_{OL}	$I_{OL} = 8mA$	-	0.4	V	
Operating Power Supply Current	I_{CC}	Cycle time = Min., $I_{I/O} = 0mA$, $\overline{CE} = V_{IL}$, $CE2 = V_{IH}$	-10	-	180	mA
			-12	-	160	mA
			-15	-	140	mA
Standby Power Supply Current	I_{SB}	$\overline{CE} = V_{IH}$ or $CE2 = V_{IL}$ V_{IN} V_{IH} or V_{IN} V_{IL}	-	30	mA	
	I_{SB1}	$\overline{CE} = V_{CC} - 0.2V$ or $CE2 = V_{CC} - 0.2V$ V_{IN} $V_{CC} - 0.2V$ or V_{IN} $0.2V$	-	5	mA	

Notes:

1. Overshoot : $V_{CC} + 2.0V$ for pulse width less than 8ns.
2. Undershoot : $V_{SS} - 2.0V$ for pulse width less than 8ns.
3. Overshoot and Undershoot are sampled, not 100% tested.

**CAPACITANCE** (TA=25 , f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	8	pF
Input/Output Capacitance	C _{I/O}	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF, I _{OH} /I _{OL} = -1mA/4mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, TA = 0 to 70)**(1) READ CYCLE**

PARAMETER	SYMBOL	UT611024-10		UT611024-12		UT611024-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	10	-	12	-	15	-	ns
Address Access Time	t _{AA}	-	10	-	12	-	15	ns
Chip Enable Access Time	t _{ACE1} , t _{ACE2}	-	10	-	12	-	15	ns
Output Enable Access Time	t _{OE}	-	5	-	6	-	7	ns
Chip Enable to Output in Low Z	t _{CLZ1*} , t _{CLZ2*}	2	-	3	-	4	-	ns
Output Enable to Output in Low Z	t _{OLZ*}	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	t _{CHZ*1} , t _{CHZ*2}	-	5	-	6	-	7	ns
Output Disable to Output in High Z	t _{OHZ*}	-	5	-	6	-	7	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	3	-	ns

(2) WRITE CYCLE

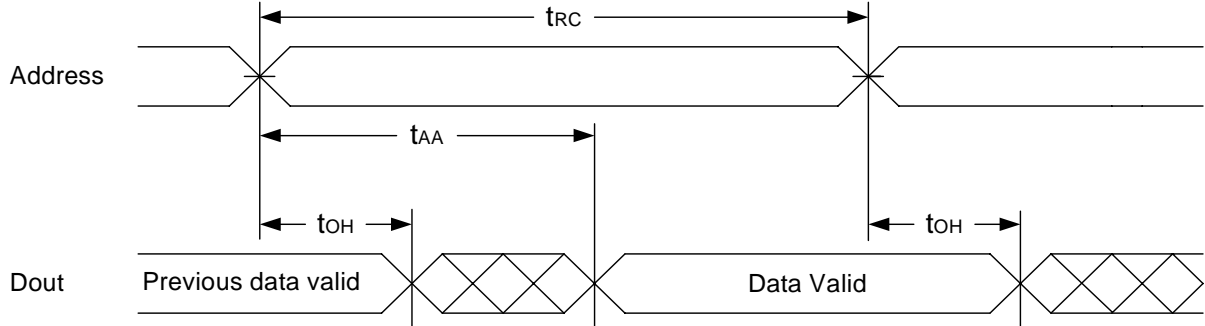
PARAMETER	SYMBOL	UT611024-10		UT611024-12		UT611024-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	10	-	12	-	15	-	ns
Address Valid to End of Write	t _{AW}	8	-	10	-	12	-	ns
Chip Enable to End of Write	t _{CW1} , t _{CW2}	8	-	10	-	12	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	8	-	9	-	10	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW*}	2	-	3	-	4	-	ns
Write to Output in High Z	t _{WHZ*}	-	6	-	7	-	8	ns

*These parameters are guaranteed by device characterization, but not production tested.

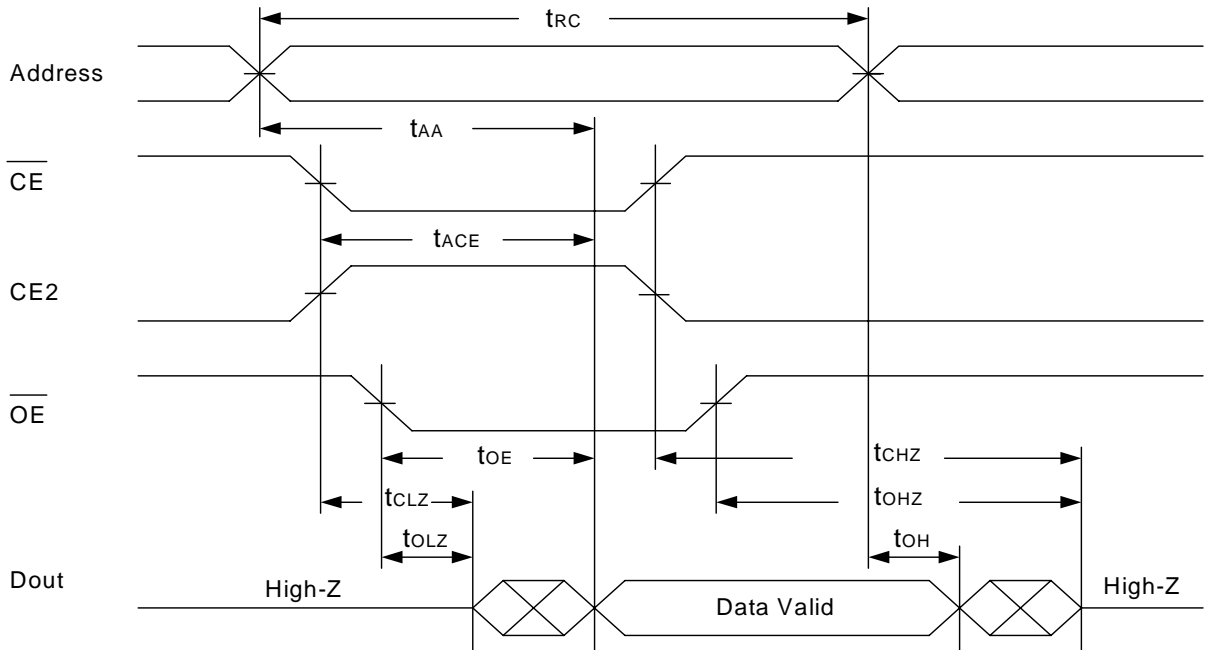


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (\overline{CE} and CE2 and \overline{OE} Controlled) (1,3,4,5)

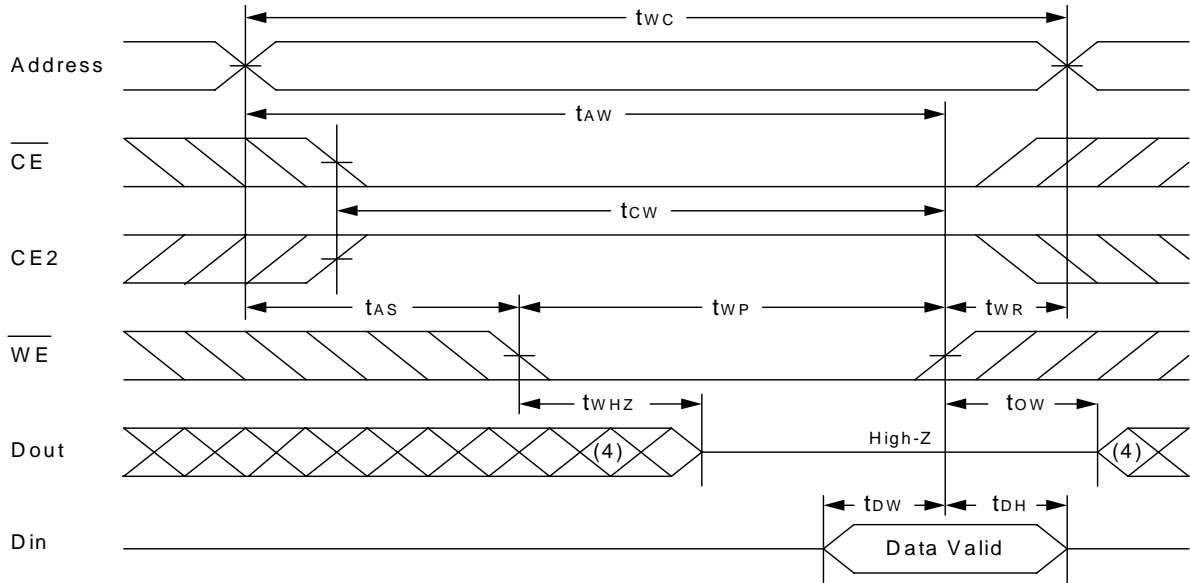


Notes :

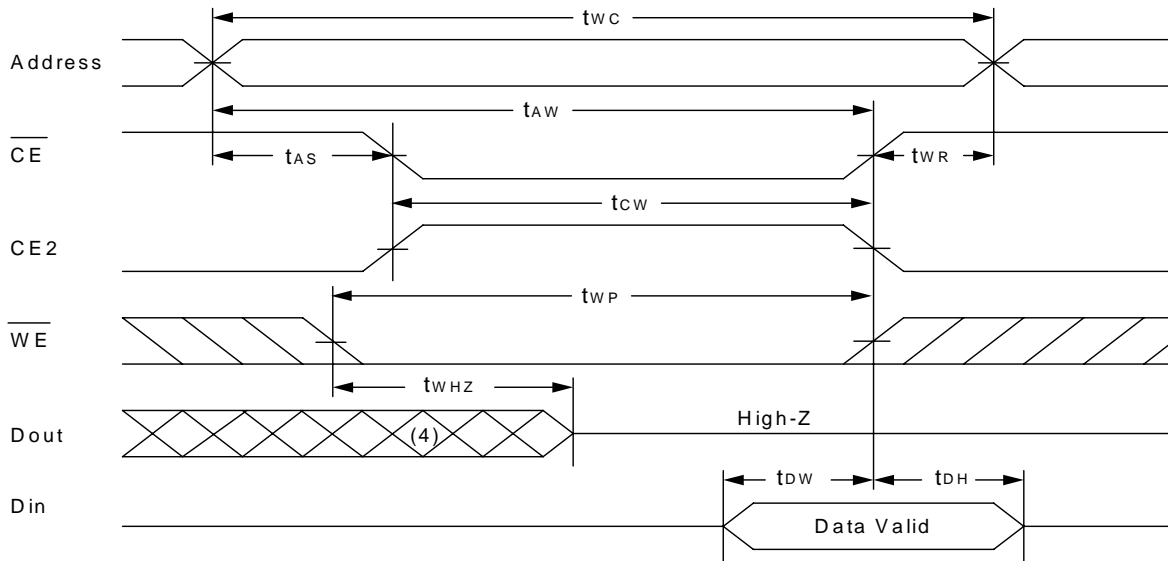
1. \overline{WE} is high for read cycle.
2. Device is continuously selected $\overline{OE} = \text{low}$, $\overline{CE} = \text{low}$, CE2=high.
3. Address must be valid prior to or coincident with $\overline{CE} = \text{low}$, CE2=high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (\overline{WE} Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (\overline{CE} and $\overline{CE2}$ Controlled) (1,2,5,6)



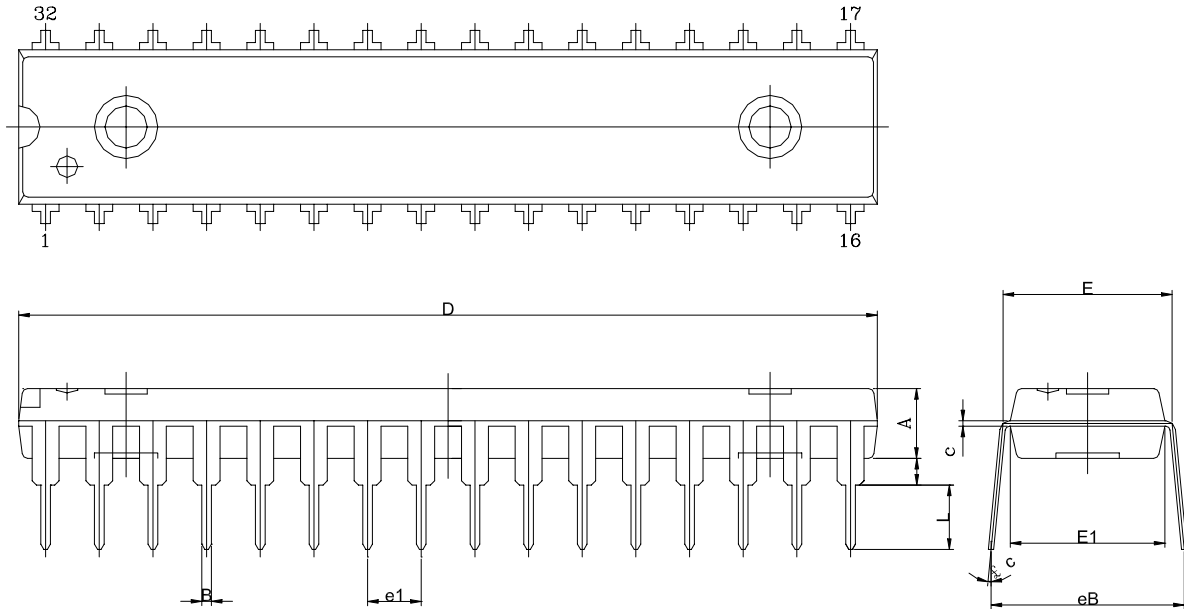
Notes :

1. \overline{WE} , \overline{CE} must be high or $\overline{CE2}$ must be low during all address transitions.
2. A write occurs during the overlap of a low \overline{CE} , high $\overline{CE2}$, low \overline{WE} .
3. During a \overline{WE} controlled write cycle with \overline{OE} low, t_{wp} must be greater than $t_{whz}+t_{dw}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the \overline{CE} low transition and $\overline{CE2}$ high transition occurs simultaneously with or after \overline{WE} low transition, the outputs remain in a high impedance state.
6. t_{ow} and t_{whz} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.



PACKAGE OUTLINE DIMENSION

32 pin PDIP 300mil Package Outline Dimension



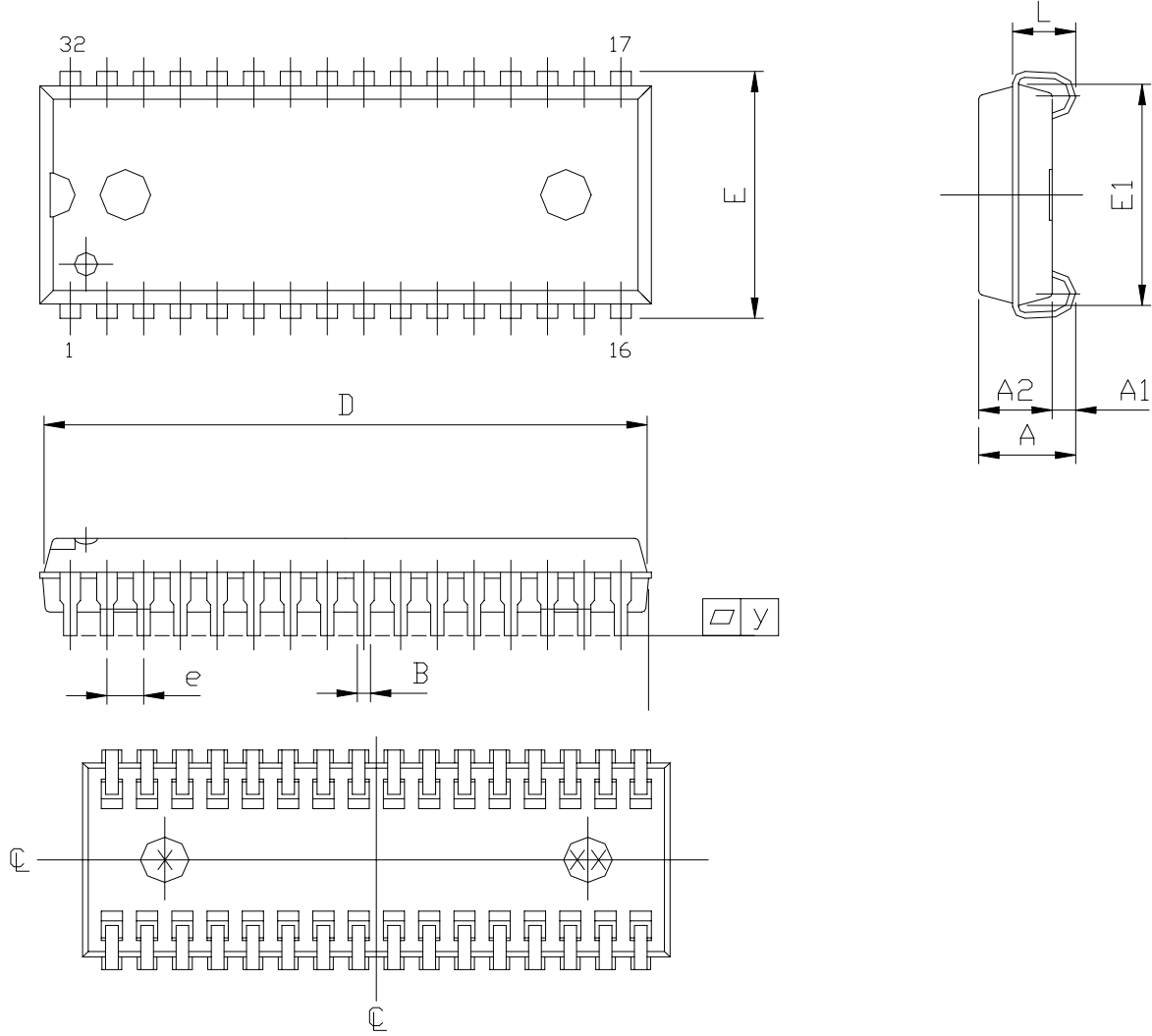
UNIT SYMBOL	INCH(BASE)	MM(REF)
A	0.130 ±0.005	3.302 ±0.127
A1	0.015(MIN)	0.381 (MIN)
B	0.018 ±0.004	0.457 ±0.102
B1	0.050 ±0.008	1.270 ±0.203
c	0.010 ±0.004	0.254 ±0.102
D	1.600 ±0.005	40.640 ±0.127
E	0.315 ±0.010	8.001 ±0.254
E1	0.288 ±0.004	7.315 ±0.102
e1	0.100 TYP	2.540 TYP
Eb	0.350 ±0.020	8.890 ±0.508
L	0.125 (MIN)	3.175 (MIN)
Q1	0.060 ±0.005	1.524 ±0.127
1c	0° 10°	0° 10°

Note :

1. All EDGE WITH MATTE FINISH.
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION.



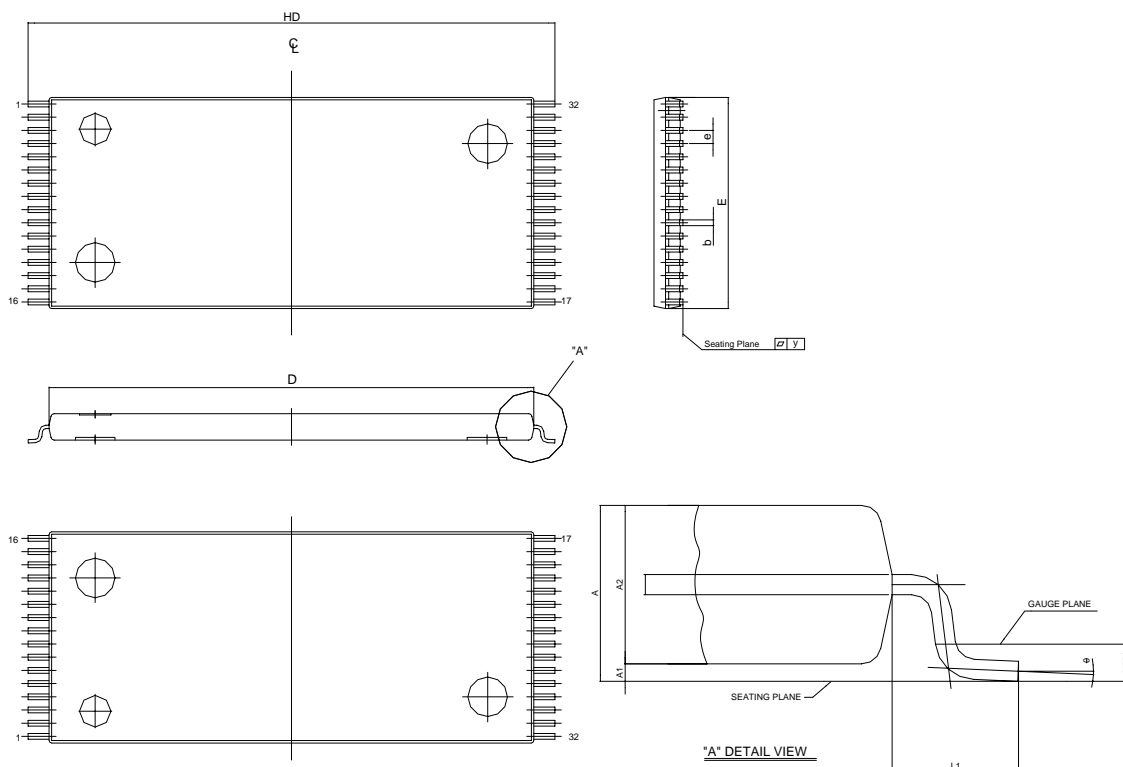
32 pin SOJ Package Outline Dimension



SYMBOL	UNIT	INCH(REF)	MM(BASE)
A		0.148 (MAX)	3.759 (MAX)
A1		0.026 (MIN)	0.660 (MIN)
A2		0.100 ±0.005	2.540 ±0.127
B		0.018 ±0.003	0.457 ±0.076
B1		0.028 ±0.003	0.711 ±0.076
C		0.010 ±0.003	0.254 ±0.076
D		0.830 (MAX)	21.082 (MAX)
E		0.335 ±0.010	8.509 ±0.254
E1		0.300 ±0.005	7.620 ±0.127
e		0.050 ±0.003	1.270 ±0.076
L		0.086 ±0.010	2.184 ±0.254
y		0.003 (MAX)	0.076 (MAX)



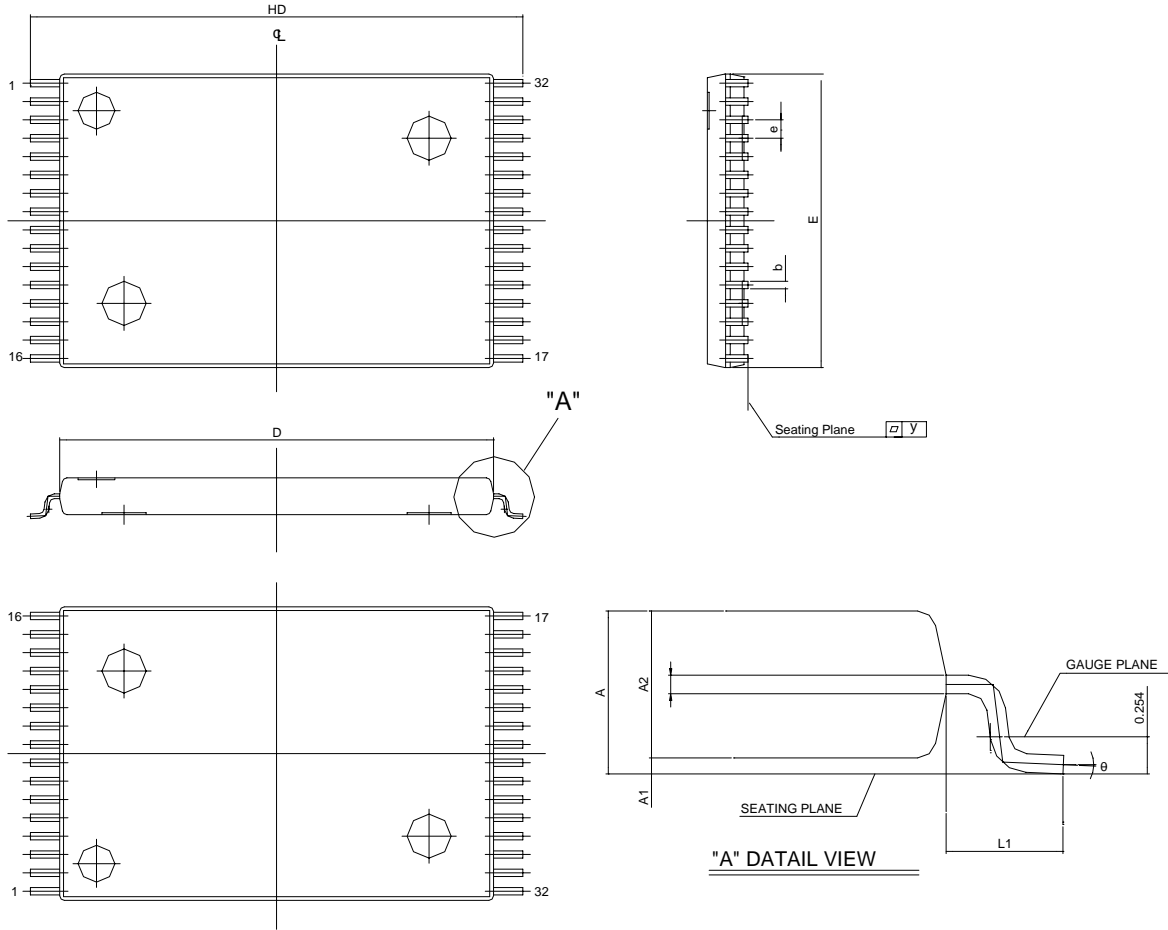
32pin TSOP-I Package Outline Dimension



SYMBOL	UNIT	INCH(BASE)	MM(REF)
A		0.047 (MAX)	1.20 (MAX)
A1		0.004 ±0.002	0.10 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.008 + 0.002 - 0.001	0.20 + 0.05 - 0.03
c		0.005 (TYP)	0.127 (TYP)
D		0.724 ±0.004	18.40 ±0.10
E		0.315 ±0.004	8.00 ±0.10
e		0.020 (TYP)	0.50 (TYP)
HD		0.787 ±0.008	20.00 ±0.20
L		0.0197 ±0.004	0.50 ±0.10
L1		0.0315 ±0.004	0.08 ±0.10
y		0.003 (MAX)	0.076 (MAX)
		0° 5°	0° 5°



32pin 8mm x 13.4mm STSOP Package Outline Dimension



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.008 ±0.001	0.200 ±0.025
D	0.465 ±0.004	11.800 ±0.100
E	0.315 ±0.004	8.000 ±0.100
e	0.020 (TYP)	0.50 (TYP)
HD	0.528 ±0.008	13.40 ±0.20.
L1	0.0315 ±0.004	0.80 ±0.10
y	0.003 (MAX)	0.076 (MAX)
	0° 5°	0° 5°



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128K X 8 BIT HIGH SPEED CMOS SRAM

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	PACKAGE
UT611024KC-12	12	32 PIN SKINNY PDIP
UT611024KC-15	15	32 PIN SKINNY PDIP
UT611024JC-10	10	32 PIN SOJ
UT611024JC-12	12	32 PIN SOJ
UT611024JC-15	15	32 PIN SOJ
UT611024LC-10	10	32 PIN TSOP-1
UT611024LC-12	12	32 PIN TSOP-1
UT611024LC-15	15	32 PIN TSOP-1
UT611024LS-10	10	32 PIN STSOP
UT611024LS-12	12	32 PIN STSOP
UT611024LS-15	15	32 PIN STSOP

ORDERING INFORMATION (for lead free product)

PART NO.	ACCESS TIME (ns)	PACKAGE
UT611024KCL-12	12	32 PIN SKINNY PDIP
UT611024KCL-15	15	32 PIN SKINNY PDIP
UT611024JCL-10	10	32 PIN SOJ
UT611024JCL-12	12	32 PIN SOJ
UT611024JCL-15	15	32 PIN SOJ
UT611024LCL-10	10	32 PIN TSOP-1
UT611024LCL-12	12	32 PIN TSOP-1
UT611024LCL-15	15	32 PIN TSOP-1
UT611024LSL-10	10	32 PIN STSOP
UT611024LSL-12	12	32 PIN STSOP
UT611024LSL-15	15	32 PIN STSOP



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