1/4 inch　330k pixel　Black and white

CMOS Image Sensor with A/D converter

TCM5040T

Technical data sheet

(Tentative Ver. 3.0)

April 17th, 2001

TOSHIBA Corporation

Semiconductor Company, System LSI Division
Marketing & Engineering Group
Digital Consumer System LSI & Image Sensor

Feature

Item	Contents
Optical format	1/4 inch
Total pixel numbers	698(H) x 502(V) (350k pixels)
Signal pixel numbers	660(H) x 492(V) (330k pixels)
Pixel pitch	5.4um(H) x 5.4um(V)
Image size	3.564mm(H) x 2.657mm(V)
Aspect ratio	4(H) : 3(V)
Power current consumption	21mA(typ) @30fps
Master clock frequency	24.54545MHz
Signal output	Progressive scanning
Color filter array	Black and white with microlens
Output format	10bit digital and proportional output in parallel
Frame rate	30fps @12.27272MHz data rate
Package	32pin CLCC

Additional functions	- Variable electronic shutter
	  Internal synchronization mode (serial command setting):
	    From 2H to 524H by 1H
	    From 1V to 16V by 1H
	  External synchronization mode:
	    From 1H to 524H and from 1V to 16V by 1H
	    From 1H to 524H, 1V and 4V combined with camera DSP
	     TC90A70F
	- Variable gain control
	- Built-in feed back clamp: Optical black level is fixed to 64LSB
	- Synchronization generator is implemented
	- Command setting by micro wire
	- 2.3 to 3.6V digital input/output is available

Maximum Ratings (Vss=0V)

Characteristics	Symbol	Rating	Unit
Power supply voltage	Vdvddio	-0.5 to 4.4	V
	Vavdd, Vdvdd	-0.5 to 3.7	
Input voltage	Vin	-0.3 to Vdd +0.3	
Input current of protection diode	Iin	+/- 20	mA
Storage temperature	Tstg	-30 to 85	Centigrade

Recommended operating conditions (Vss=0V)

Characteristics	Symbol	Rating			Unit
		Min	Typ	Max	
Power supply voltage	Vdvddio	2.3	2.8	3.6	V
	Vavdd,Vdvdd	2.7	2.8	2.9	
Input voltage	Vin	0 to Vdvddio			
Operating temperature	Topr	-20 to 60			Centigrade

Block Diagram

Input of SGMODE controls synchronization mode between external synchronization mode and internal. In the case of ext. sync. mode, HPA, VRR and ESR pulse should be supplied to sensor.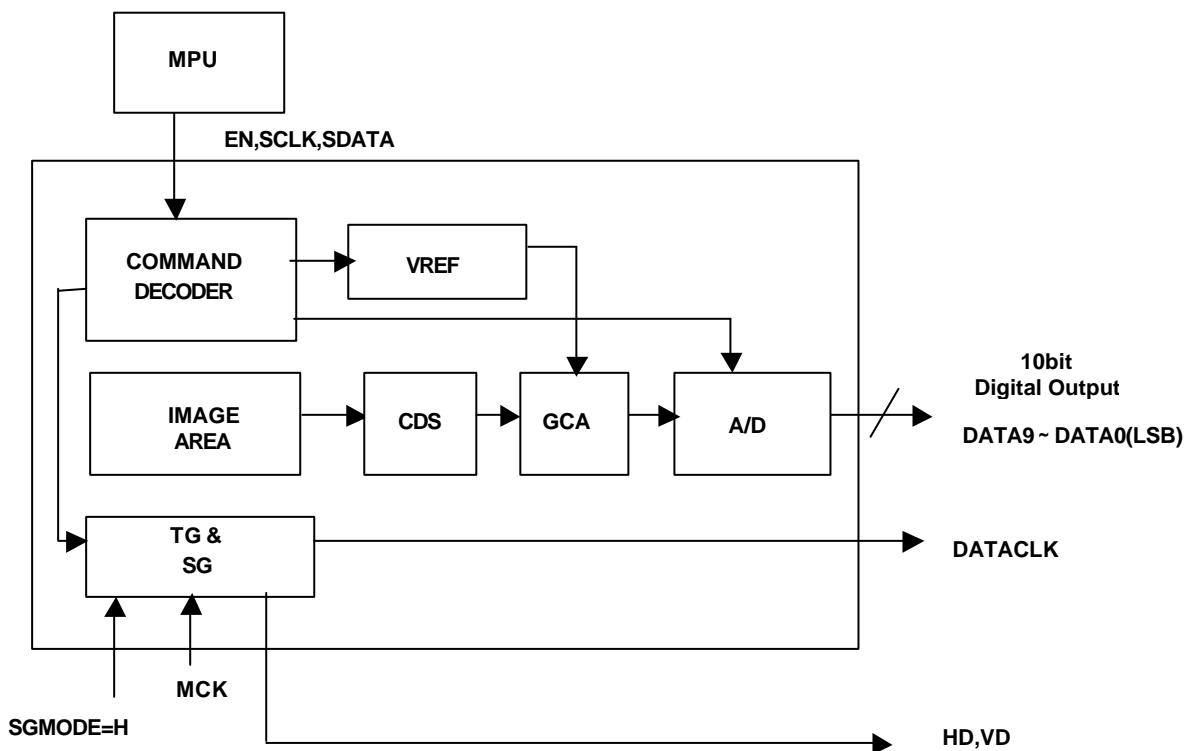 On the other hand, HD, VD and data clock is generated from sensor on int. sync. In that case electronic shutter speed is controlled by command setting.
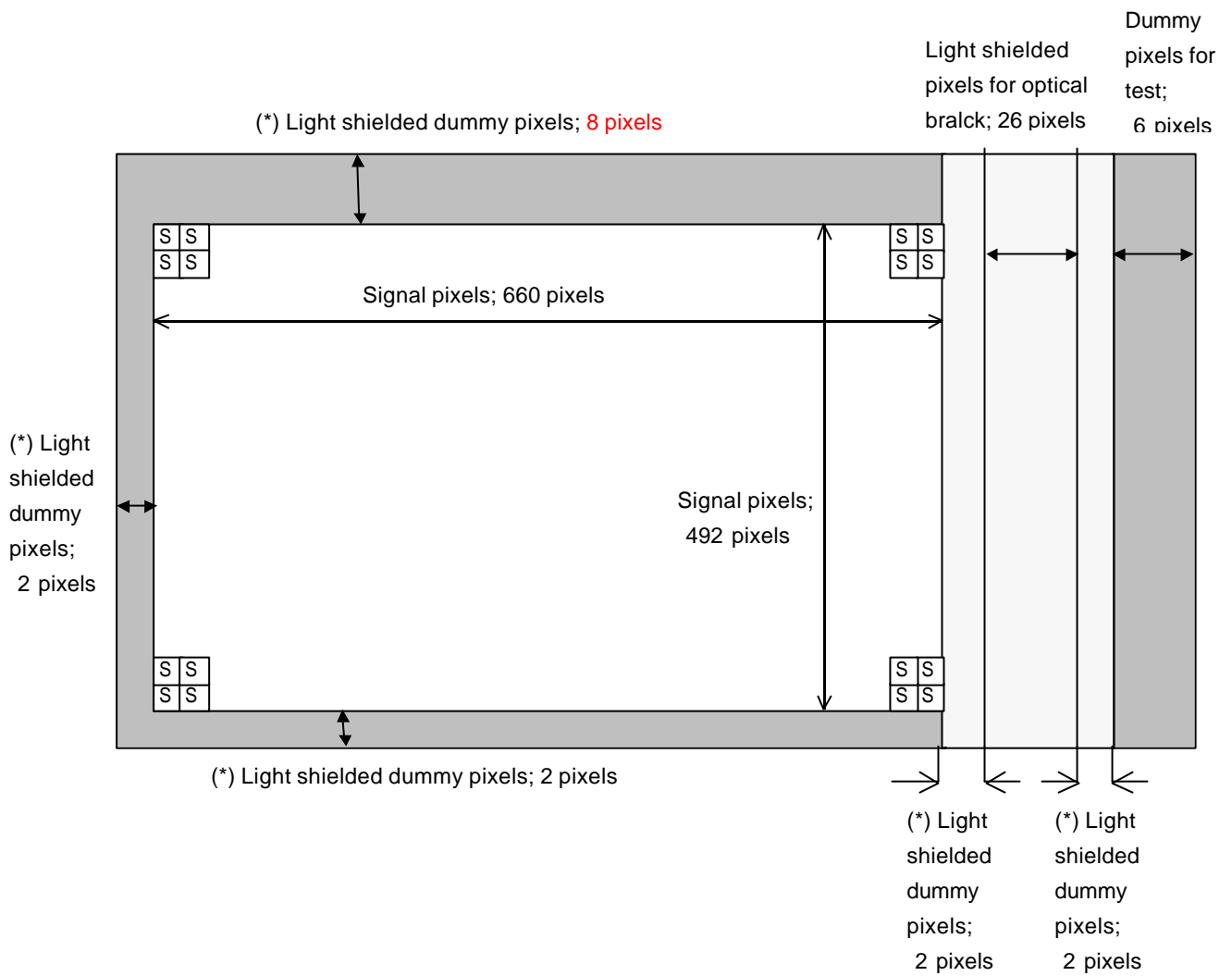
External synchronization mode

```
                    ┌──────────┐
                    │   MPU    │
                    └────┬─────┘
                         │ EN,SCLK,SDATA
        ┌────────────────┼──────────────────────────────────────┐
        │                ▼                                        │
        │         ┌──────────────┐      ┌──────────┐              │
        │    ┌───▶│   COMMAND    │─────▶│   VREF   │──┐           │
        │    │    │   DECODER    │      └──────────┘  │           │
        │    │    └──────────────┘                    │           │
        │    │                                        │           │
        │    │  ┌────────────┐  ┌──────┐  ┌──────┐  ┌──────┐      │
        │    │  │   IMAGE    │─▶│ CDS  │─▶│ GCA  │─▶│ A/D  │──────┼──▶ 10bit Digital Output
        │    │  │   AREA     │  └──────┘  └──────┘  └──────┘      │     DATA9  DATA0(LSB)
        │    │  └────────────┘                                    │
        │    │  ┌────────────┐                                    │
        │    └─▶│   TG &      │                                    │
        │       │   SG        │                                    │
        │       └────┬──┬──┬──┘                                    │
        └────────────┼──┼──┼───────────────────────────────────────┘
                     ▲  ▲  ▲
                     │  │  │ HPA,VRR,ESR
        SGMODE=L or OPEN   MCK
```

Internal synchronization mode

```
                    ┌──────────┐
                    │   MPU    │
                    └────┬─────┘
                         │ EN,SCLK,SDATA
        ┌────────────────┼──────────────────────────────────────┐
        │                ▼                                        │
        │         ┌──────────────┐      ┌──────────┐              │
        │    ┌───▶│   COMMAND    │─────▶│   VREF   │──┐           │
        │    │    │   DECODER    │      └──────────┘  │           │
        │    │    └──────────────┘                    │           │
        │    │                                        │           │
        │    │  ┌────────────┐  ┌──────┐  ┌──────┐  ┌──────┐      │
        │    │  │   IMAGE    │─▶│ CDS  │─▶│ GCA  │─▶│ A/D  │──────┼──▶ 10bit Digital Output
        │    │  │   AREA     │  └──────┘  └──────┘  └──────┘      │     DATA9  DATA0(LSB)
        │    │  └────────────┘                                    │
        │    │  ┌────────────┐                                    │
        │    └─▶│   TG &      │───────────────────────────────────┼──▶ DATACLK
        │       │   SG        │                                    │
        │       └────┬──┬─────┘                                    │
        └────────────┼──┼──────────────────────────────────────────┼──▶ HD,VD
                     ▲  ▲
                     │  │
              SGMODE=H   MCK
```

Pixel Arrangement

Light shielded pixels for optical bralck; 26 pixels

Dummy pixels for test; 6 pixels

(*) Light shielded dummy pixels; 8 pixels

Signal pixels; 660 pixels

S S
S S

S S
S S

(*) Light shielded dummy pixels; 2 pixels

Signal pixels; 492 pixels

S S
S S

S S
S S

(*) Light shielded dummy pixels; 2 pixels

(*) Light shielded dummy pixels; 2 pixels

(*) Light shielded dummy pixels; 2 pixels

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Pin Configuration

Pin No.	Symbol	Function	Pin management
1	SCLK	Serial clock input	
2	SDATA	Serial data input	
3	EN	Data enable input	
4	TEST1	Test terminal	Connected to GND(AVSS) via a capacitor of 2.2uF
5	TEST2	Test terminal	Connected to GND(AVSS) via a capacitor of 0.1uF
6	AVSS	Analog GND (VSS)	0V
7	TEST3	Test terminal	No connection
8	AVDD	Analog power supply (VDD)	2.8V +/- 0.1V. Bi-passed condenser(2.2uF and 0.1uF) is preferable.
9	DVSS	Digital GND (VSS)	0V
10	MCK	Master clock input	24.54545 MHz
11	DVDD	Digital power supply (VDD)	2.8V +/- 0.1V. Bi-passed condenser(4.7uF and 0.1uF) is preferable. Output impedance of power supply is recommended to be under 0.5 ohm @10kHz.
12	DATA0	AD output(LSB)	
13	DATA1	AD output	
14	DATA2	AD output	
15	DATA3	AD output	
16	DATA4	AD output	
17	DATA5	AD output	
18	DATA6	AD output	
19	DATA7	AD output	
20	DATA8	AD output	
21	DATA9	AD output(MSB)	
22	DVSSIO	Digital I/O GND (VSS)	0V
23	DATACLK	Data clock output (a half of MCK)	
24	DVDDIO	Digital I/O power supply (VDD)	2.3 to 3.6V. Bi-passed condenser(2.2uF and 0.1uF) is preferable.
25	TEST4	Test terminal	No connection
26	DSTOP	Read stop control input (pull-up)	1: Active / 0: Halt
27	VRR(VD)	Vertical timing pulse start pulse input / VD pulse output	
28	ESR STR	Electrical shutter start pulse input	
29	HPA(HD)	Horizontal timing start pulse input / HD pulse output	
30	SGMODE	Internal / external synchronization mode (pull-down)	0: External sync (HPA,VRR and ESR input) 1: Internal sync (HD,VD output)
31	TEST5	Test terminal	Connected to AVSS
32	RESET	Reset for parameter setting	Connected to DVDDIO via 100k to 1M ohm. Connected to GND via 0.1uF

*Aluminum electrolytic capacitor or Tantalum capacitor are desirable for power line.

Application circuit

C1: 4.7uF
C2: 2.2uF
C3: 0.1uF
R1: 100k to 1M

2.8+/-0.1V
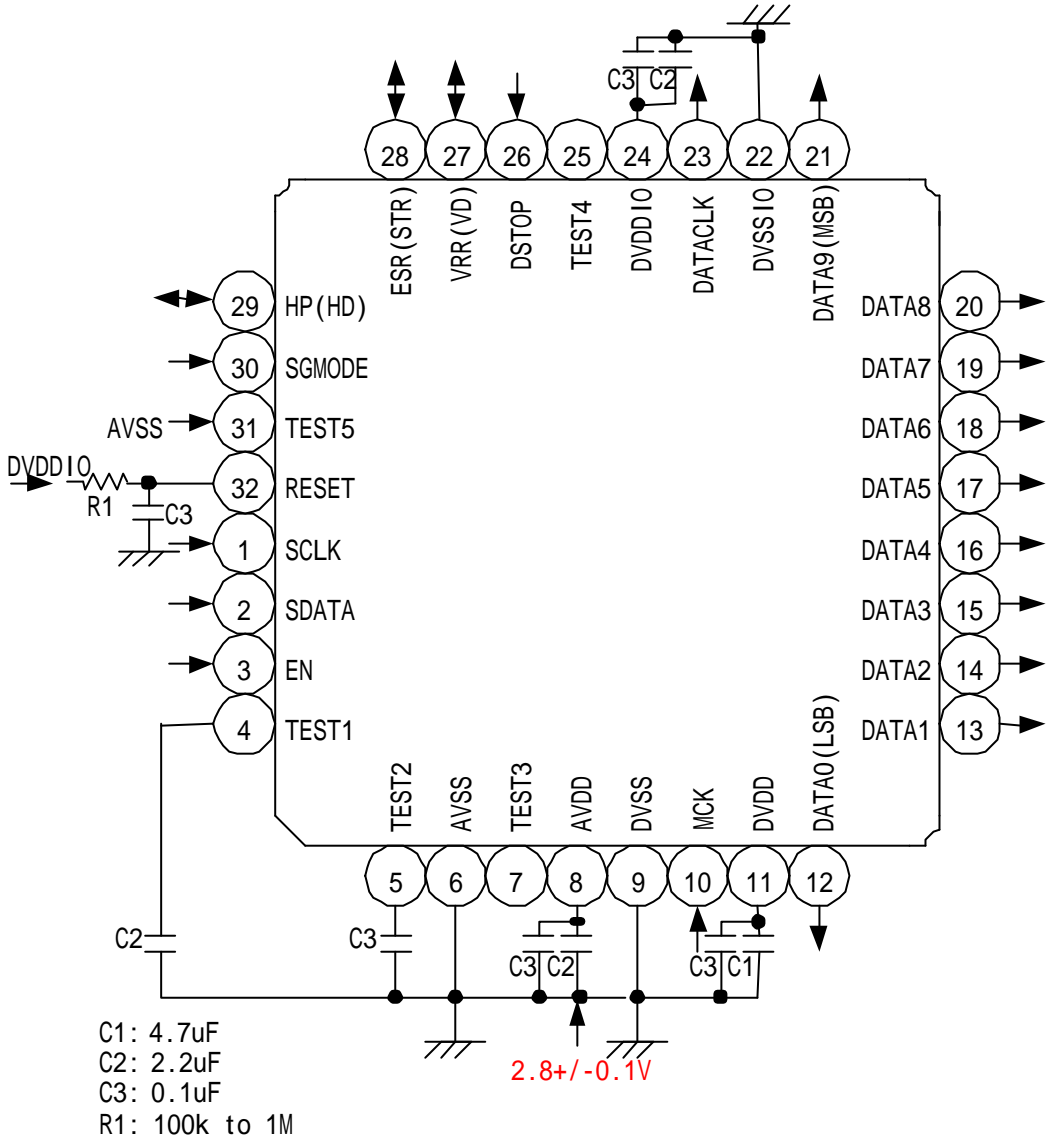
Optical and electrical characteristics

Item	Symbol	Conditions	Min	Typ	Max	Unit
Sensitivity	R	Condition *1	512	682	-	LSB
Blooming margin	BLM	500 times as standard condition	No blooming			
S/N (dark)	S/N	Standard condition	-	57	-	dB
Decay lag	LAG	Output; over 20mV	-	3 (6 LSB)	7 (14 LSB)	mV
Power current	IDD	Frame rate; 30fps	-	21	-	mA

- Setting value of internal gain amplifier; x1 (0dB)
- (***LSB) means 10 bit digital output not include 64LSB for black level.
- Signal output includes 64 LSB for black level.

Standard conditions (Tc=60 degrees Centigrade)
 - Driving conditions:
   Frame rate; 30fps, Electronics shutter; Off (1/30s), VDD=2.8+/-0.1V
   Parameter setting value; Default
 - Light source: Color temperature; 3200K, Tangusten light
 - Optical lens; Fujinon CF25L (F0.85, f=25mm), F2.8
 - Standard signal level: Output (average) 250mV

Condition *1
 - Luminance of object; 100nt
 - Driving and optical conditions are same as standard conditions.

Relation between analog and digital output
 - Setting value of internal gain amplifier; x1 (0dB)
 - Linear gain
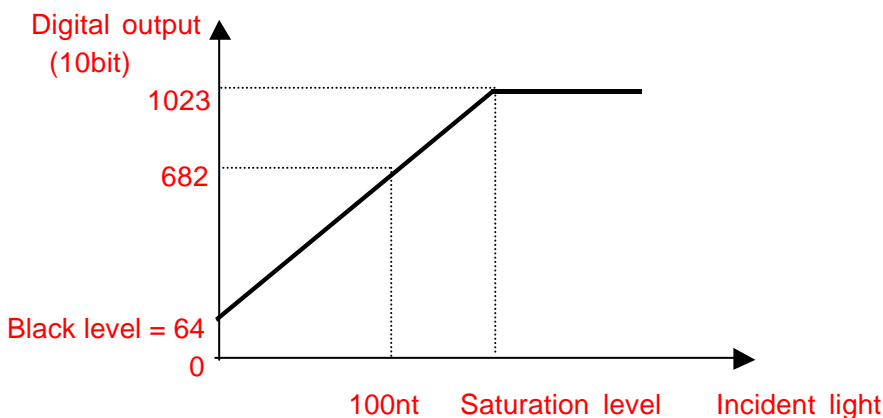
DC/AC characteristics

DC characteristics (Vdd=2.8+/-0.2V, Tc=-20 to 60 degrees Centigrade)

Symbol	Item	Conditions	Min	Typ	Max	Unit	Note
VIH	High level input voltage		2	-	-	V	Note1
VIL	Low level input voltage		-	-	0.8	V	Note1
IIH	High level input current	VIN=VDD	-1	-	1	uA	Note1
IIL	Low level input current	VIN=VSS	-1	-	1	uA	Note1
VOH	High level output voltage	IOH=-4mA	2.2	-	-	V	Note2
VOL	Low level output voltage	IOL= 4mA	-	-	0.4	V	Note2
IDD	Current consumption	VDD=2.8V	-	21	-	mA	

Note1   DSTOP, VRR, ESR, HPA, SGMODE, RESET, SCLK, SDATA, EN and MCK
Note2   VD, STR, HD, DATACLK, DATA0 to DATA9

AC characteristics (Vdd=2.8+/-0.2V, Tc=-20 to 60 degrees Centigrade)

Item	Symbol	Conditions	Min	Typ	Max	Unit	Note
Set-up time for input	ts	Based on MCK			10	ns	Note1
Hold time for input	th	Based on MCK			10	ns	Note1
Output delay time	tpd	Based on MCK (C=15pF)			10	ns	Note2
Command clock frequency	fsclk				6		Note3

Note1   DSTOP, VRR, ESR and HPA,
Note2   DATACLK, DATA0 to DATA9
Note3   SCLK
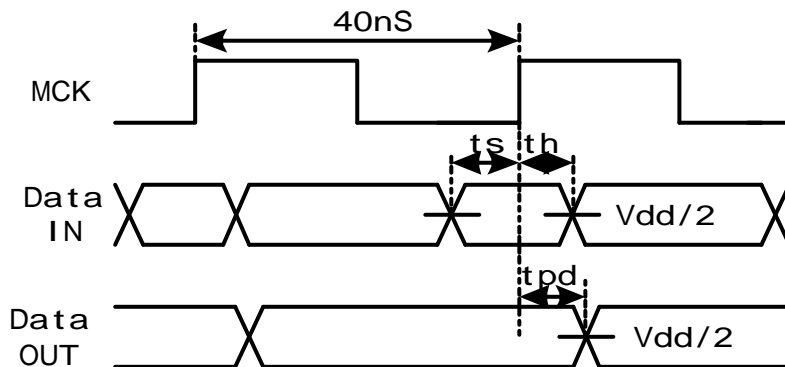
Command setting table

(1) Timing chart
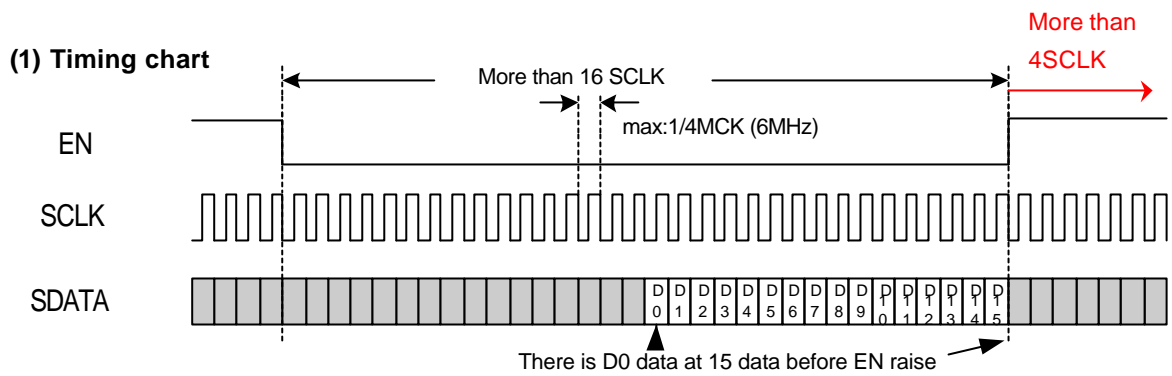
(2) Command setting

Setting item	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Note
Gain setting	0	0	0	0	MSB		Setting	data(10bit)				LSB					
Electronic shutter	1	0	1	0	MSB		Setting	data(10bit)				LSB					2H to 16V
Monitoring mode	1	1	1	1		*											0: 30fps(default) 1: 60fps

* Default value setting is available w/o sending command. Gain value should be set after power on reset.

* In the case of internal synchronization mode, command setting of electronic shutter speed is available. ESR pulse need to be input on external synchronization mode.

* Command is set at the rising edge of VRR or VD, and it will be effective on next frame.

(3) Typical setting value

1) Gain setting table (typical value)

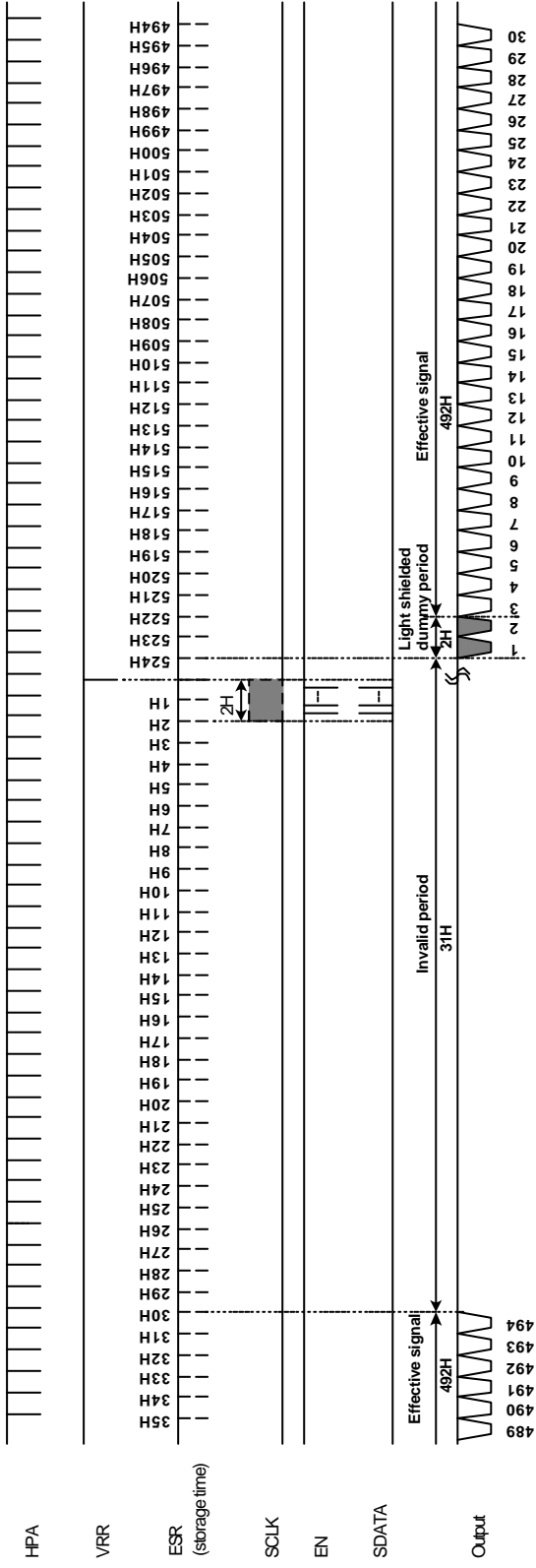| Gain level (dB)	Setting value									
	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2
-2.4 (Min)	1	0	0	1	0	1	1	1	1	0
0 (Standard)	0	1	1	1	0	0	1	1	0	0
3	0	1	0	1	0	0	0	1	1	0
6	0	0	1	1	1	0	0	1	1	0
9	0	0	1	0	1	0	0	0	1	1
12	0	0	0	1	1	1	0	1	0	0
18	0	0	0	0	1	1	1	0	1	0
20 (Recommended max)	0	0	0	0	1	0	1	1	1	0

2) Electronic shutter setting (internal synchronization mode)

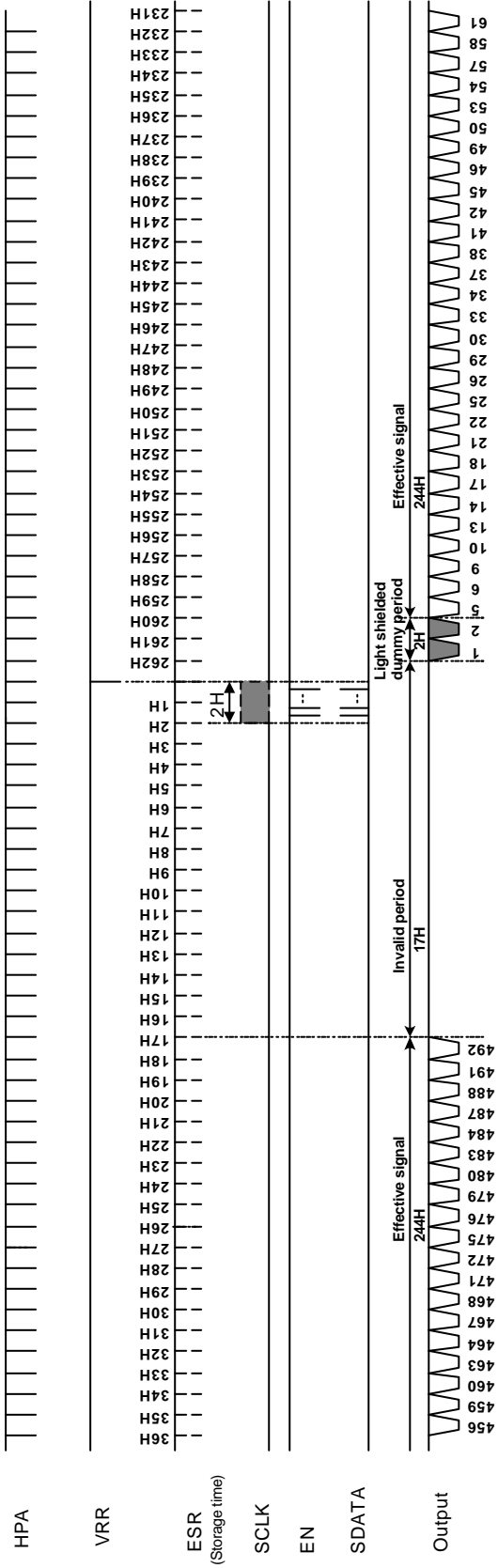| Electronic shutter speed (Storage time)	Setting value									
	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2
Shutter Off (525H)	0	0	0	0	0	0	0	0	0	0
2 (H)	0	0	0	0	0	0	0	0	0	1
3 (H)	0	0	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:	:	:
523 (H)	1	0	0	0	0	0	1	0	1	0
524 (H)	1	0	0	0	0	0	1	0	1	1

Signal output format (external sync in normal mode) 1V=525H
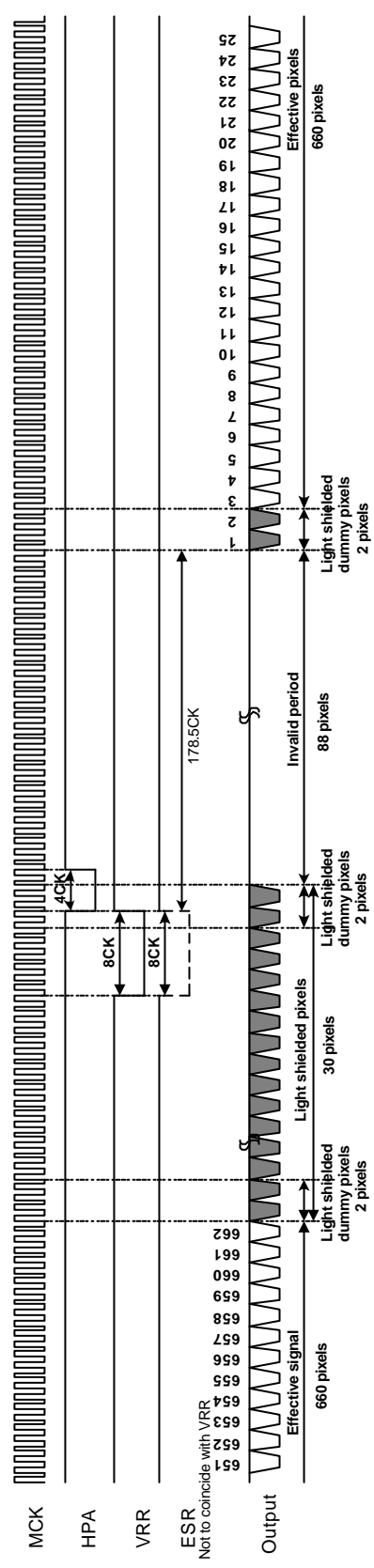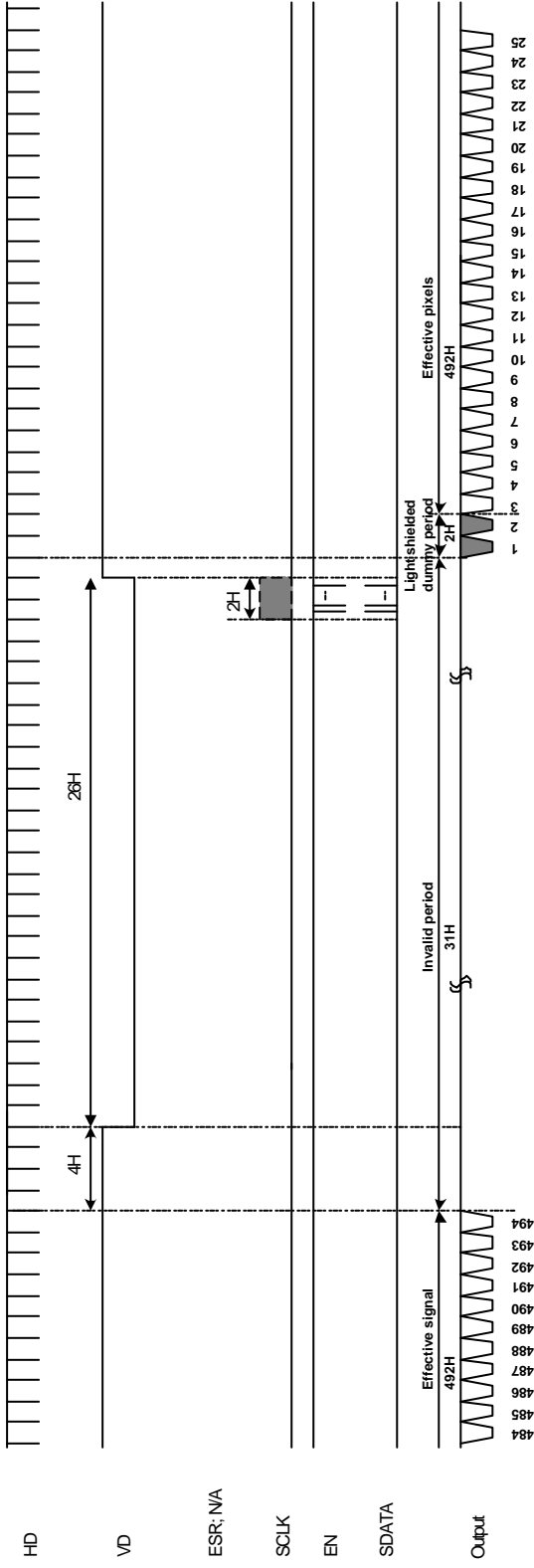
Vertical period

Horizontal period

HPA
VRR
ESR (storage time)
SCLK
EN
SDATA
Output

MCK
HPA
VRR
ESR (Not to coincide with VRR)
Output

494H 495H 496H 497H 498H 499H 500H 501H 502H 503H 504H 505H 506H 507H 508H 509H 510H 511H 512H 513H 514H 515H 516H 517H 518H 519H 520H 521H 522H 523H 524H

1H 2H 3H 4H 5H 6H 7H 8H 9H 10H 11H 12H 13H 14H 15H 16H 17H 18H 19H 20H 21H 22H 23H 24H 25H 26H 27H 28H 29H 30H 31H 32H 33H 34H 35H

2H

Effective signal 492H

Invalid period 31H

Light shielded dummy period 2H

Effective signal 492H

30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

494 493 492 491 490 489

Effective signal 660 pixels
651 652 653 654 655 656 657 658 659 660 661 662

Light shielded dummy pixels 2 pixels

Light shielded pixels 30 pixels

8CK
8CK
4CK

178.5CK

Invalid period 88 pixels

Light shielded dummy pixels 2 pixels

Light shielded dummy pixels 2 pixels

Effective pixels 660 pixels

25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

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Signal output format (external sync in monitoring mode) 1V=263H

Vertical pieoid

HPA

VRR

ESR
(Storage time)

SCLK

EN

SDATA

Output

Effective signal
244H

Invalid period
17H

Effective signal
244H

2H

Light shielded
dummy period

Effective signal
244H

Light shielded
dummy period
2H

Horizontal period

MCK

HPA

VRR

ESR
Not to coincide with VRR

Output

Effective signal
660 pixels

Light shielded
dummy pixels
2 pixels

Light shielded pixels
30 pixels

8CK

8CK

4CK

178.5CK

Invalid period
88 pixels

Light shielded
dummy pixels
2 pixels

Light shielded
dummy pixels
2 pixels

Effective pixels
660 pixels

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Signal output format (Internal sync in normal mode) 1V=525H

Vertical period

Labels: HD, VD, ESR; N/A, SCLK, EN, SDATA, Output

26H, 4H, 2H, 2H

Invalid period 31H

Light shielded dummy period

Effective signal 492H

Effective pixels 492H

484 485 486 487 488 489 490 491 492 493 494

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25

Horizontal period

Labels: MCK, HD, VD, Output

174CK, 141CK, 39CK

Invalid period 88 pixels

Light shielded pixels 30 pixels

Light shielded dummy pixels 2 pixels

Effective pixels 660 pixels

651 652 653 654 655 656 657 658 659 660 661 662

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25

11

Signal output format (internal sync in monitoring mode) 1V=263H

Vertical period

Horizontal period

Long storage time mode

1) Setting mode

  (1) External sync mode

    Intermittent mode by skipping VRR input

    Electronic shutter can be set by 1H from 1V to 16V

  (2) Internal sync mode

Electronic shutter speed (storage time)	Setting value									
	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2
Long storage　2V	1	1	0	0	0	0	0	0	0	1
3V	1	1	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:	:	:
15V	1	1	0	0	0	0	1	1	1	0
16V	1	1	0	0	0	0	1	1	1	1

Timing diagram for long storage mode

Long storage mode on external sync mode

Normal storage operation

VRR

ESR

Storage time=262H

Signal output
(assumed as analog output)

16V 1V 2V 3V 4V 5V 6V 10V 11V 12V 13V 14V 15V 16V 1V
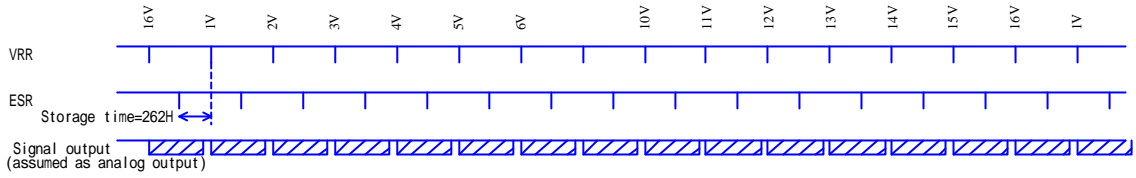
Long storage mode from 1V to 16V by 1H

Example 1

VRR

ESR

Storage time=1V+262H

Signal output
(assumed as analog output)

Example 2

VRR

ESR

Storage time=15V+262H

Signal output
(assumed as analog output)
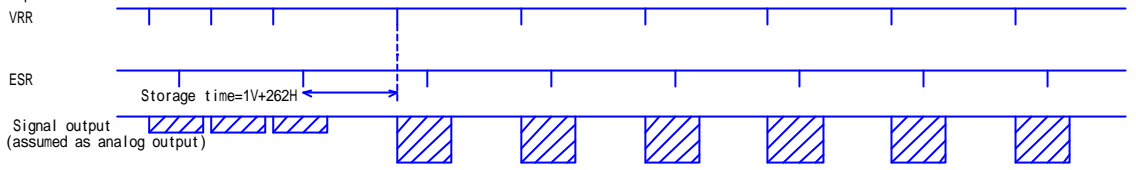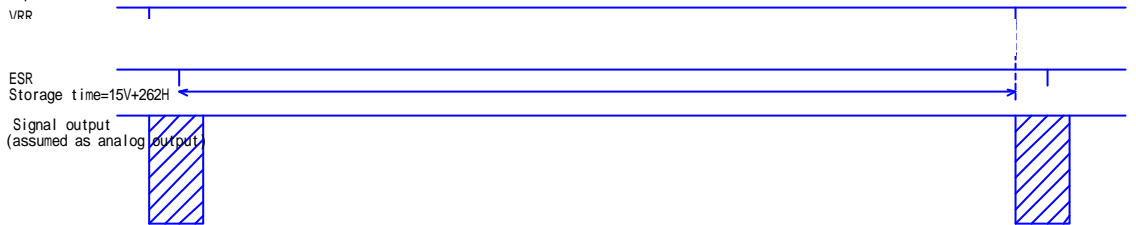
Note: ESR can be set from 1H to 524H, or set to OFF(H)

Long strorage mode on internal sync mode

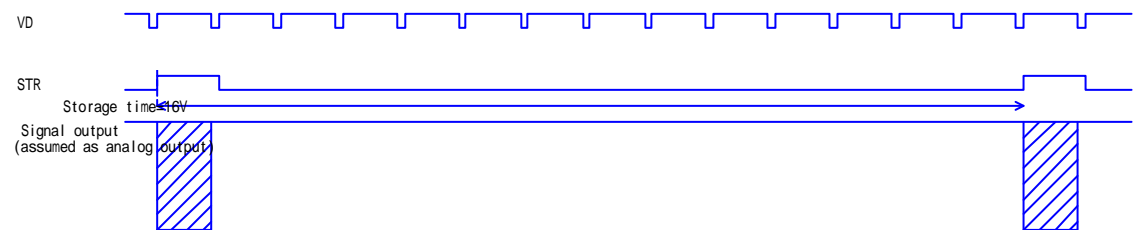Normal storage operation

When Electrical shutter speed is set to 262H

VD

STR

Signal output
(assumed as analog output)

16V 1V 2V 3V 4V 5V 6V 10V 11V 12V 13V 14V 15V 16V 1V
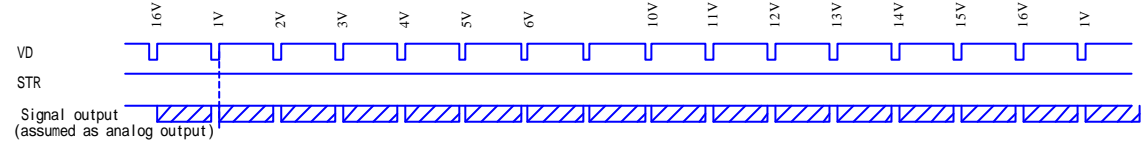
Long storage mode from 2V to 16V by 1V

Example 1

VD

STR

Storage time=2V

Signal output
(assumed as analog output)

Example 2

VD

STR

Storage time=16V

Signal output
(assumed as analog output)
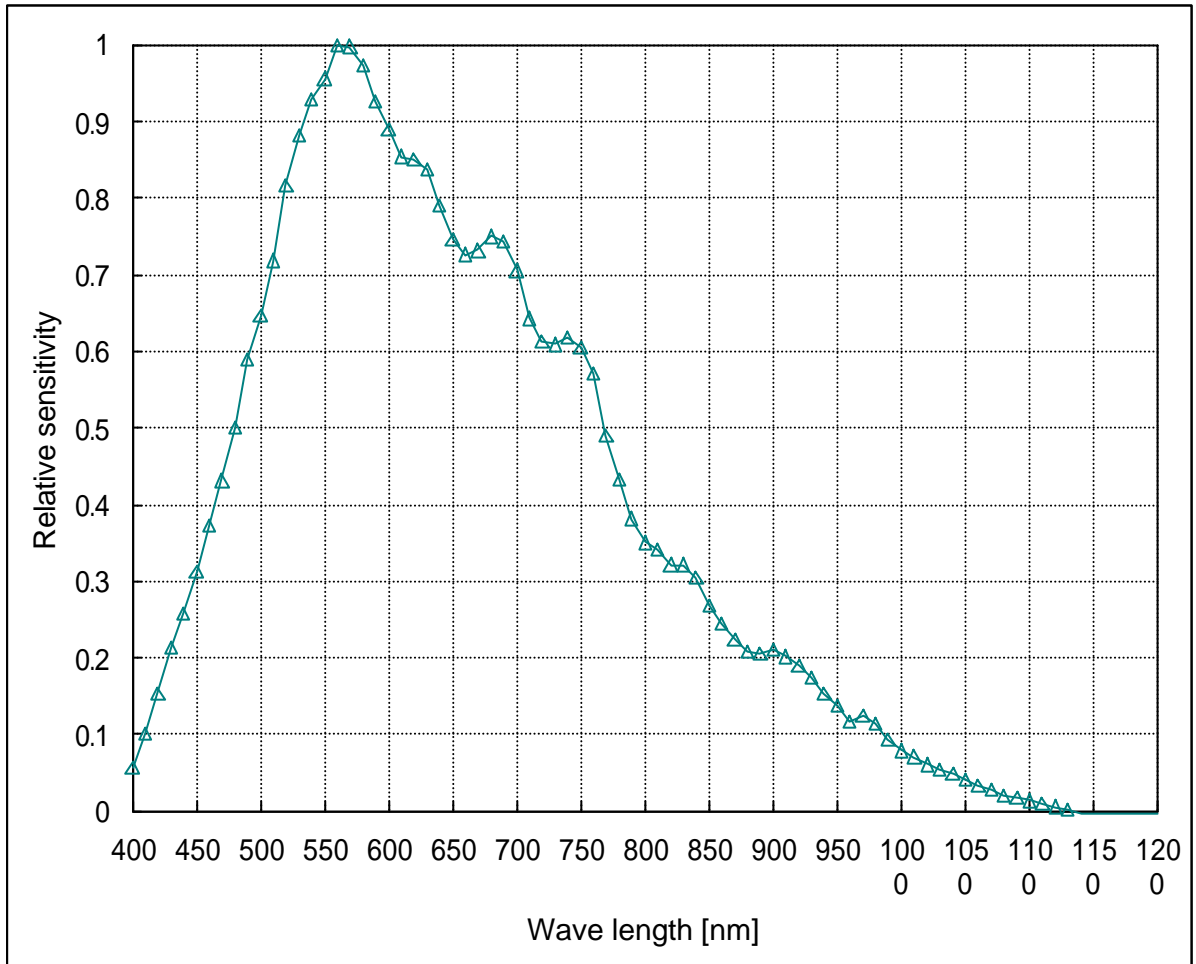
14
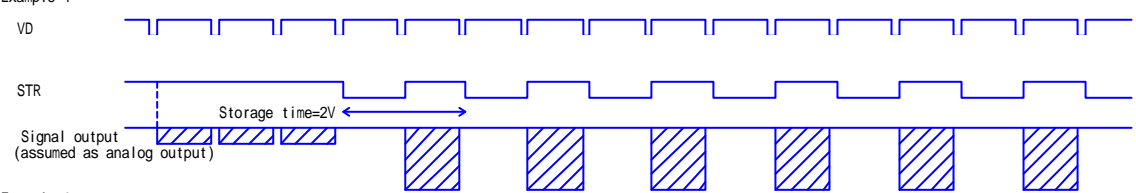
Typical spectral response

Package outline
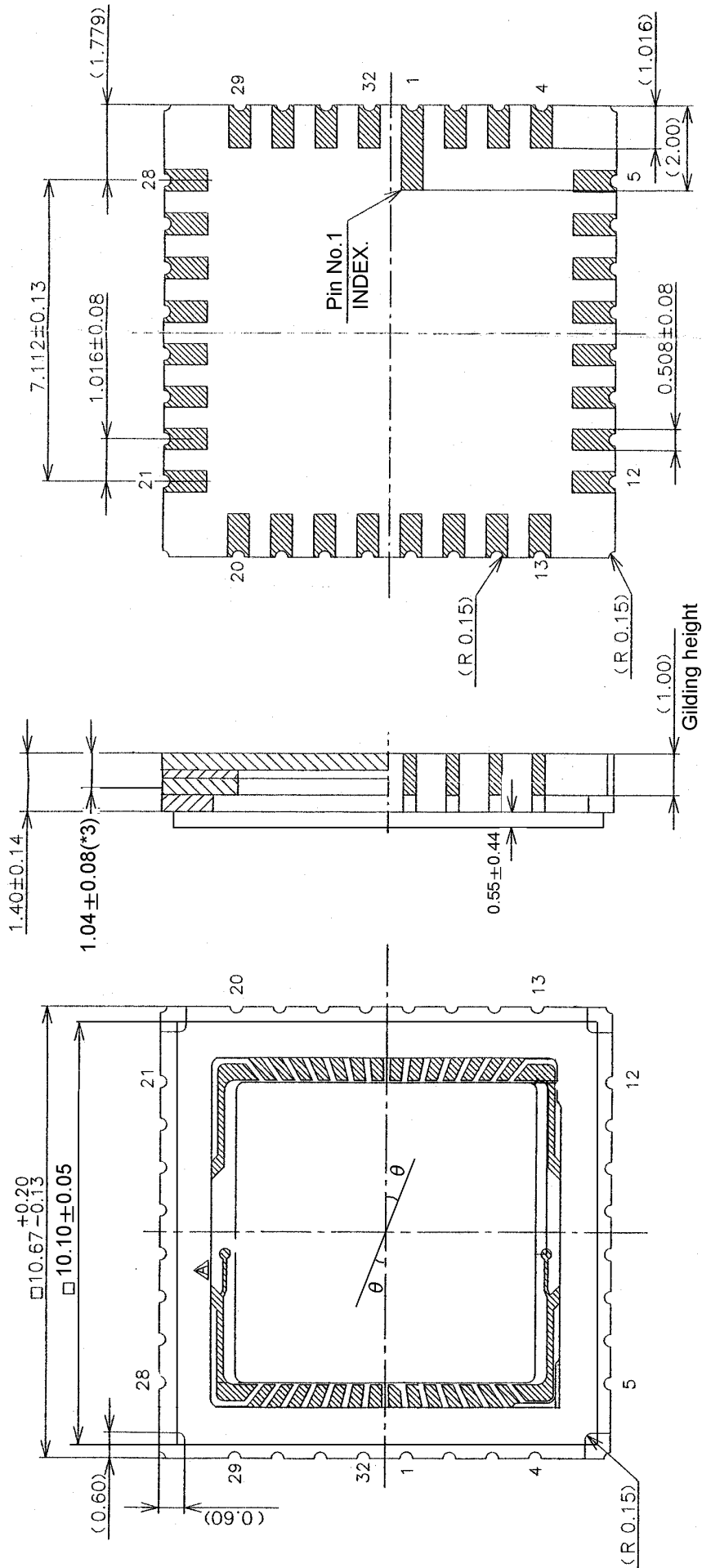

Image center coincide with package center; tolerance is +/- 0.15mm

Refractive index of Glass : nd = 1.52

Rotation of die : θ =1.0deg MAX

(*3)Chip surface to Package Bottom

16