TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7MA245FK

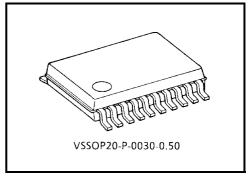
Low-Voltage Octal Bus Transceiver with 3.6 V Tolerant Inputs and Outputs

The TC7MA245FK is a high performance CMOS octal bus transceiver. Designed for use in 1.8 , 2.5 or 3.3 V systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

It is also designed with over voltage tolerant inputs and outputs up to $3.6\ V\!.$

The direction of data transmission is determined by the level of the DIR inputs. The \overline{OE} inputs can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.



Weight: 0.03 g (typ.)

Features

- Low voltage operation: VCC = 1.8~3.6 V
- High speed operation:

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t_{pd} = 3.5 \text{ ns (max) (V}_{CC} = 3.0 \text{~-} 3.6 \text{ V)} \\ t_{pd} = 4.2 \text{ ns (max) (V}_{CC} = 2.3 \text{~-} 2.7 \text{ V)} \\ t_{pd} = 8.4 \text{ ns (max) (V}_{CC} = 1.8 \text{ V)} \\
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- 3.6 V tolerant inputs and outputs.
- Package: VSSOP (US20)
- Output current:

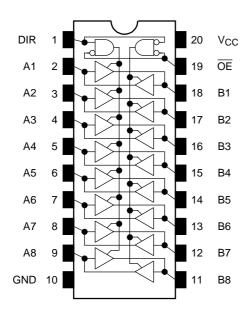
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\begin{split} & I_{OH}/I_{OL} = \pm 24 \text{ mA (min) (V}_{CC} = 3.0 \text{ V)} \\ & I_{OH}/I_{OL} = \pm 18 \text{ mA (min) (V}_{CC} = 2.3 \text{ V)} \\ & I_{OH}/I_{OL} = \pm 6 \text{ mA (min) (V}_{CC} = 1.8 \text{ V)} \end{split}
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- Latch-up performance: ±300 mA
- ESD performance:

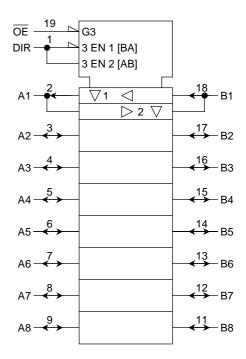
Machine model $> \pm 200 \text{ V}$

- Human body model > ±2000 V
- Bidirectional interface between 2.5 V and 3.3 V signals. (*1)
- Power down protection is provided on all inputs and outputs. (*2)
- Supports live insertion/withdrawal (*3)
 - *1: Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
 - *2: All floating (high impedance) bus terminal must have their input level fixed by means of pull up or pull down resistors.
 - *3: To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

Inp	uts	Outputs	Fund	ction
ŌĒ	DIR	Odipuis	A-Bus	B-Bus
L	L	A = B	Output	Input
L	Н	B = A	Input	Output
Н	Х	Z	2	7

X: Don't care

Z: High impedance

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Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	-0.5~4.6	V
DC input voltage (DIR, $\overline{\text{OE}}$)	V _{IN}	-0.5~4.6	V
DC bus I/O voltage	Vivo	-0.5~4.6 (Note1)	V
Do bus 1/O voltage	V _{I/O} -0.5~V _{CC} + 0.5 (Note2		V
Input diode current	I _{IK}	-50	mA
Output diode current	I _{OK}	±50 (Note3)	mA
DC output current	lout	±50	mA
Power dissipation	P _D	180	mW
DC V _{CC} /ground current	I _{CC} /I _{GND}	±100	mA
Storage temperature	T _{stg}	-65~150	°C

Note1: Off-state

Note2: High or low state. $I_{\mbox{\scriptsize OUT}}$ absolute maximum rating must be observed.

Note3: $V_{OUT} < GND, V_{OUT} > V_{CC}$

Recommended Operating Range

Characteristics	Symbol	Rating	Unit	
Supply voltage	V	1.8~3.6	V	
Supply voltage	V _{CC}	1.2~3.6 (Note4)	V	
Input voltage (DIR, OE)	V _{IN}	-0.3~3.6	V	
Bus I/O voltage	Vera	0~3.6 (Note5)	V	
Bus I/O voltage	V _{I/O}	0~V _{CC} (Note6)	V	
		±24 (Note7)		
Output current	I _{OH} /I _{OL}	±18 (Note8)	mA	
		±6 (Note9)	·	
Operating temperature	T _{opr}	-40~85	°C	
Input rise and fall time	dt/dv	0~10 (Note10)	ns/V	

Note4: Data retention only

Note5: Off-state

Note6: High or low state

Note7: $V_{CC} = 3.0 \sim 3.6 \text{ V}$

Note8: $V_{CC} = 2.3 \sim 2.7 \text{ V}$

Note9: $V_{CC} = 1.8 \text{ V}$

Note10: $V_{IN} = 0.8 \sim 2.0 \text{ V}, V_{CC} = 3.0 \text{ V}$

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Electrical Characteristics

DC Characteristics (Ta = $-40 \sim 85$ °C, 2.7 V < V_{CC} \leq 3.6 V)

Characteri	stics	Symbol	Test Condition		V _{CC} (V)	Min	Max	Unit
Input voltage	High level	V _{IH}		_	2.7~3.6	2.0	_	V
input voitage	Low level	V _{IL}		_	2.7~3.6	_	0.8	V
				I _{OH} = -100 μA	2.7~3.6	V _{CC} - 0.2	-	
	High level	V _{OH}	$V_{IN} = V_{IH}$ or V_{IL}	I _{OH} = -12 mA	2.7	2.2	_	
				$I_{OH} = -18 \text{ mA}$	3.0	2.4	_	
Output voltage				$I_{OH} = -24 \text{ mA}$	3.0	2.2		V
		evel V _{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100 \mu A$	2.7~3.6	_	0.2	
	Low level			I _{OL} = 12 mA	2.7	_	0.4	
	LOW level			$I_{OL} = 18 \text{ mA}$	3.0	_	0.4	
				$I_{OL} = 24 \text{ mA}$	3.0	_	0.55	
Input leakage curre	nt	I _{IN}	V _{IN} = 0~3.6 V		2.7~3.6	_	±5.0	μΑ
3-state output off-st	ate current	I _{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OLIT} = 0 \sim 3.6 \text{ V}$		2.7~3.6	_	±10.0	μΑ
Power off leakage of	current	l _{OFF}	V _{IN} , V _{OUT} = 0~3.6 V		0	_	10.0	μА
		,	V _{IN} = V _{CC} or GND		2.7~3.6	_	20.0	
Quiescent supply co	unent	Icc	$V_{CC} \le (V_{IN}, V_{OUT}) \le 3.6 \text{ V}$		2.7~3.6	_	±20.0	μΑ
Increase in I _{CC} per	input	Δl _{CC}	$V_{IH} = V_{CC} - 0.6 V$		2.7~3.6	_	750	

DC Characteristics (Ta = $-40\sim85^{\circ}$ C, 2.3 V \leq V_{CC} \leq 2.7 V)

Characteristics		Symbol	mbol Test Condition			Min	Max	Unit		
Character	1131103	Symbol	163	rest Condition		IVIIII	IVIAA	Offic		
Input voltage	High level	V_{IH}		_	2.3~2.7	1.6	_	V		
Input voltage	Low level	V _{IL}		_	2.3~2.7	_	0.7	V		
				I _{OH} = -100 μA	2.3~2.7	V _{CC} - 0.2	_			
	High level	Voн	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -6 mA	2.3	2.0	_			
						I _{OH} = -12 mA	2.3	1.8	_	
Output voltage				I _{OH} = -18 mA	2.3	1.7	_			
				$I_{OL} = 100 \mu A$	2.3~2.7	_	0.2			
	Low level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH} \ or \ V_{IL}$	I _{OL} = 12 mA	2.3	_	0.4		
				I _{OL} = 18 mA	2.3	_	0.6			
Input leakage curre	ent	I _{IN}	V _{IN} = 0~3.6 V		2.3~2.7	_	±5.0	μА		
3-state output off-state current		la-	V _{IN} = V _{IH} or V _{IL}		2.3~2.7		±10.0	^		
3-state output on-s	state current	loz	V _{OUT} = 0~3.6 V	V _{OUT} = 0~3.6 V		_	±10.0	μА		
Power off leakage	current	loff	V _{IN} , V _{OUT} = 0~3.6 V		0	_	10.0	μΑ		
Quiescent supply current I _C		loo	$V_{IN} = V_{CC}$ or GND		2.3~2.7		20.0			
		Icc	$V_{CC} \le (V_{IN}, V_{OUT}) \le$	3.6 V	2.3~2.7	_	±20.0	μА		

DC Characteristics (Ta = -40~85°C, 1.8 V \leq V_{CC} < 2.3 V)

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Characteri	stics	Symbol	Test Condition		V _{CC} (V)	Min	Max	Unit
Input voltage	High level	V _{IH}		_	1.8~2.3	0.7 × V _{CC}	_	V
input voitage	Low level	V _{IL}		_	1.8~2.3		0.2 × V _{CC}	V
	High level	V _{OH}	$V_{IN} = V_{IH}$ or V_{IL}	I _{OH} = -100 μA	1.8	V _{CC} - 0.2		
Output voltage				$I_{OH} = -6 \text{ mA}$	1.8	1.4	_	- V
	Low level	Voi	V_{OL} $V_{IN} = V_{IH}$ or V_{IL}	I _{OL} = 100 μA	1.8		0.2	
	LOW level	VOL		I _{OL} = 6 mA	1.8		0.3	
Input leakage curre	nt	I _{IN}	V _{IN} = 0~3.6 V		1.8		±5.0	μΑ
3-state output off-st	ate current	loz	$V_{IN} = V_{IH}$ or V_{IL}		1.8		±10.0	μА
3-state output off-state current		102	V _{OUT} = 0~3.6 V		1.0		±10.0	μΛ
Power off leakage of	current	I _{OFF}	V _{IN} , V _{OUT} = 0~3.6 V		0	_	10.0	μА
Quiescent supply c	Quiocoont cumply current		$V_{IN} = V_{CC}$ or GND		1.8	_	20.0	μА
Quioscont supply of	unont	Icc	$V_{CC} \le (V_{IN}, V_{OUT}) \le 3.6 \text{ V}$		1.8	_	±20.0	μΛ

AC Characteristics (Ta = -40~85°C, Input: $t_r = t_f = 2.0$ ns, $C_L = 30$ pF, $R_L = 500$ Ω)

Characteristics	Symbol	Test Condition	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	Min	Max	Unit
			V _{CC} (V)			
	t _{pLH}		1.8	1.5	8.4	
Propagation delay time	t _{pHL}	Figure 1, Figure 2	2.5 ± 0.2	8.0	4.2	ns
	φпс		3.3 ± 0.3	0.6	3.5	
	.		1.8	1.5	9.8	
3-state output enable time	t _{pZL} t _{pZH}	Figure 1, Figure 3	2.5 ± 0.2	8.0	5.6	ns
			3.3 ± 0.3	0.6	4.5	
			1.8	1.5	7.2	
3-state output disable time	t _{pLZ}	Figure 1, Figure 3	2.5 ± 0.2	8.0	4.0	ns
	^t pHZ		3.3 ± 0.3	0.6	3.6	
			1.8		0.5	
Output to output skew	t _{osLH}	(Note11)	2.5 ± 0.2	_	0.5	ns
	tosHL		3.3 ± 0.3	_	0.5	

For $C_L = 50\ pF$, add approximately 300 ps to the AC maximum specification.

Note11: This parameter is guaranteed by design.

 $(t_{OSLH} = |t_{PLHm} - t_{PLHn}|, \ t_{OSHL} = |t_{PHLm} - t_{PHLn}|)$

Dynamic Switching Characteristics (Ta = 25°C, Input: $t_r = t_f = 2.0$ ns, $C_L = 30$ pF)

Characteristics	Symbol	Test Condition		V _{CC} (V)	Тур.	Unit
		$V_{IH} = 1.8 \text{ V}, V_{IL} = 0 \text{ V}$ (No.	ote12)	1.8	0.25	
Quiet output maximum dynamic V _{OL}	V _{OLP}	$V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$ (No.	ote12)	2.5	0.6	V
		$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ (No.	ote12)	3.3	0.8	
		$V_{IH} = 1.8 \text{ V}, V_{IL} = 0 \text{ V}$ (No.	ote12)	1.8	-0.25	
Quiet output minimum dynamic $V_{\mbox{OL}}$	V _{OLV}	$V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$ (No.	ote12)	2.5	-0.6	V
		$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ (No.	ote12)	3.3	-0.8	
		$V_{IH} = 1.8 \text{ V}, V_{IL} = 0 \text{ V}$ (No.	ote12)	1.8	1.5	
Quiet output minimum dynamic V _{OH}	V _{OHV}	$V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$ (No.	ote12)	2.5	1.9	V
		$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ (No.	ote12)	3.3	2.2	

Note12: This parameter is guaranteed by design.

Capacitive Characteristics (Ta = 25°C)

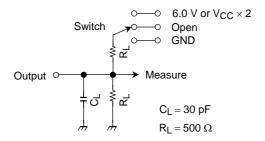
Characteristics	aracteristics Symbol Test Condition			Тур.	Unit	
Characteristics				V _{CC} (V)	τyp.	Offic
Input capacitance	C _{IN}	_		1.8, 2.5, 3.3	6	рF
Bus I/O capacitance	C _{I/O}	_		1.8, 2.5, 3.3	7	pF
Power dissipation capacitance	C _{PD}	$f_{\text{IN}} = 10 \text{ MHz}$ (No	ote13)	1.8, 2.5, 3.3	20	рF

Note13: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 (per bit)$

AC Test Circuit



Parameter	Switch		
t _{pLH} , t _{pHL}	Open		
t _{pLZ} , t _{pZL}			
t _{pHZ} , t _{pZH}	GND		

Figure 1

AC Waveform

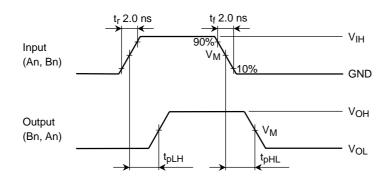


Figure 2 t_{pLH}, t_{pHL}

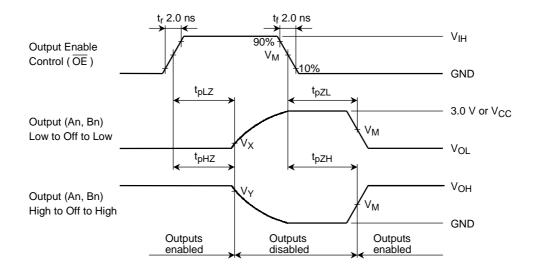
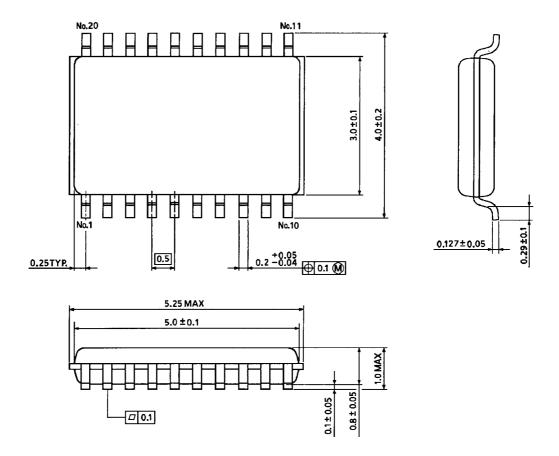


Figure 3 $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$

Cumbal		V _{CC}	
Symbol	$3.3\pm0.3~\textrm{V}$	$2.5\pm0.2\textrm{V}$	1.8 V
V _{IH}	2.7 V	V _{CC}	V _{CC}
V _M	1.5 V	V _{CC} /2	V _{CC} /2
V _X	V _{OL} + 0.3 V	V _{OL} + 0.15 V	V _{OL} + 0.15 V
VY	V _{OH} – 0.3 V	V _{OH} – 0.15 V	V _{OH} – 0.15 V

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Package Dimensions



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Weight: 0.03 g (typ.)

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