

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74LCX16244AFT

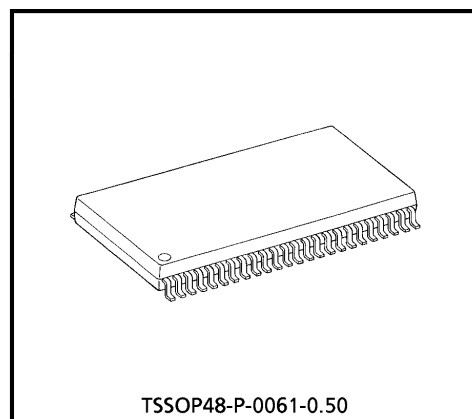
LOW-VOLTAGE 16-BIT BUS BUFFER WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX16244AFT is a high performance CMOS 16bit BUS BUFFER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

This device is non-inverting 3-state buffer having four active-low output enables. It can be used as four 4-bit buffers two 8-bit buffers or one 16-bit buffer. When the \overline{OE} input is high, the outputs are in a high impedance state. This device is designed to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge.

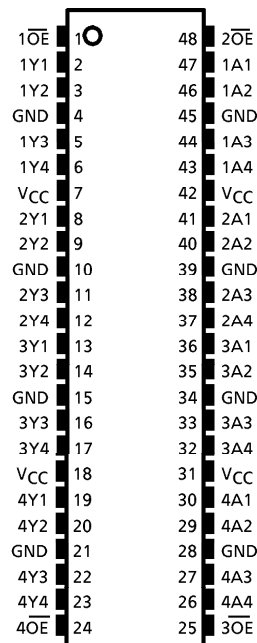


Weight : 0.25 g (Typ.)

FEATURES

- Low Voltage Operation : $V_{CC} = 2.0 \sim 3.6V$
- High Speed Operation : $t_{pd} = 5.2ns$ (max.) at $V_{CC} = 3.0 \sim 3.6V$
- Output Current : $|I_{OH}| / I_{OL} = 24mA$ (MIN) at $V_{CC} = 3.0V$
- Latch-up Performance : $\pm 500mA$
- Package : TSSOP
(Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.

PIN CONNECTION



(TOP VIEW)

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TRUTH TABLE

INPUTS		OUTPUTS
$\overline{1OE}$	1A1-1A4	1Y1-1Y4
L	L	L
L	H	H
H	X	Z

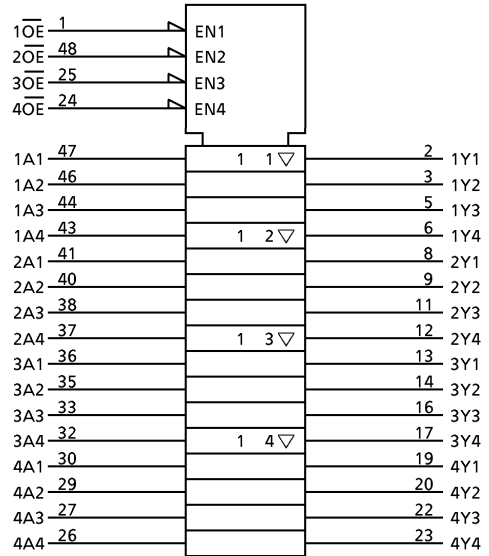
INPUTS		OUTPUTS
$\overline{2OE}$	1A1-2A4	2Y1-2Y4
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUTS
$\overline{3OE}$	3A1-3A4	3Y1-3Y4
L	L	L
L	H	H
H	X	Z

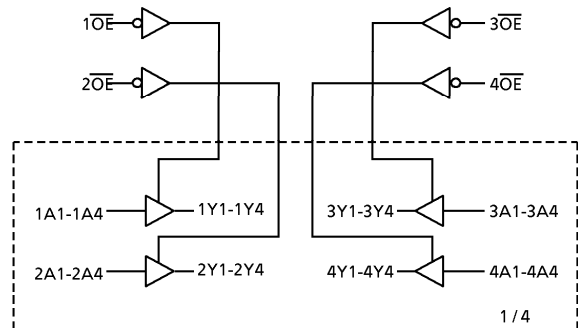
INPUTS		OUTPUTS
$\overline{4OE}$	4A1-4A4	4Y1-4Y4
L	L	L
L	H	H
H	X	Z

X : Don't Care
Z : High impedance

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



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MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	-0.5~7.0	V
Input Voltage	V_{IN}	-0.5~7.0	V
Output Voltage	V_{OUT}	-0.5~7.0 (Note 1)	V
		-0.5~ $V_{CC} + 0.5$ (Note 2)	
Input Diode Current	I_{IK}	-50	mA
Output Diode Current	I_{OK}	± 50 (Note 3)	mA
DC Output Current	I_{OUT}	± 50	mA
Power Dissipation	P_D	400	mW
DC V_{CC} / Ground Current Per Supply Pin	I_{CC} / I_{GND}	± 100	mA
Storage Temperature	T_{stg}	-65~150	$^{\circ}C$

(Note 1) Output in Off-State

(Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.

(Note 3) $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
		1.5~3.6 (Note 4)	
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~5.5 (Note 5)	V
		0~ V_{CC} (Note 6)	
Output Current	I_{OH} / I_{OL}	± 24 (Note 7)	mA
		± 12 (Note 8)	
Operating Temperature	T_{opr}	-40~85	$^{\circ}C$
Input Rise And Fall Time	dt / dv	0~10 (Note 9)	ns / V

(Note 4) Data Retention Only

(Note 5) Output in Off-State

(Note 6) High or Low State

(Note 7) $V_{CC} = 3.0 \sim 3.6V$

(Note 8) $V_{CC} = 2.7 \sim 3.0V$

(Note 9) $V_{IN} = 0.8 \sim 2.0V$, $V_{CC} = 3.0V$

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = -40~85°C)

PARAMETER		SYMBOL	TEST CONDITION		V _{CC} (V)	MIN.	MAX.	UNIT
Input Voltage	"H" Level	V _{IH}			2.7~3.6	2.0	—	V
	"L" Level	V _{IL}			2.7~3.6	—	0.8	V
Output Voltage	"H" Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100μA	2.7~3.6	V _{CC} - 0.2	—	V
				I _{OH} = -12μA	2.7	2.2	—	
				I _{OH} = -18mA	3.0	2.4	—	
				I _{OH} = -24mA	3.0	2.2	—	
	"L" Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100μA	2.7~3.6	—	0.2	V
				I _{OL} = 12mA	2.7	—	0.4	
				I _{OL} = 16mA	3.0	—	0.4	
				I _{OL} = 24mA	3.0	—	0.55	
Input Leakage Current		I _{IN}	V _{IN} = 0~5.5V		2.7~3.6	—	±5.0	μA
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~5.5V		2.7~3.6	—	±5.0	μA
Power Off Leakage Current		I _{OFF}	V _{IN} / V _{OUT} = 5.5V		0	—	10.0	μA
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND		2.7~3.6	—	20.0	μA
			V _{IN} / V _{OUT} = 3.6~5.5V		2.7~3.6	—	±20.0	
Increase In I _{CC} Per Input		ΔI _{CC}	V _{IH} = V _{CC} - 0.6V		2.7~3.6	—	500	μA

AC characteristics (Ta = -40~85°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{CC} (V)	MIN.	MAX.	UNIT
Propagation Delay Time	t _{pLH}	(Fig.1, 2)	2.7	—	6.2	ns
	t _{pHL}		3.3 ± 0.3	1.5	5.2	
3-State Output Enable Time	t _{pZL}	(Fig.1, 3)	2.7	—	7.5	ns
	t _{pZH}		3.3 ± 0.3	1.5	6.5	
3-State Output Disable Time	t _{pLZ}	(Fig.1, 3)	2.7	—	6.5	ns
	t _{pHZ}		3.3 ± 0.3	1.5	5.5	
Output To Output Skew	t _{osLH}	(Note 10)	2.7	—	—	ns
	t _{osHL}		3.3 ± 0.3	—	1.0	

(Note 10) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Dynamic switching characteristics

(Ta = 25°C, Input t_r = t_f = 2.5ns, C_L = 50pF, R_L = 500Ω)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP	UNIT
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V

Capacitive characteristics (Ta = 25°C)

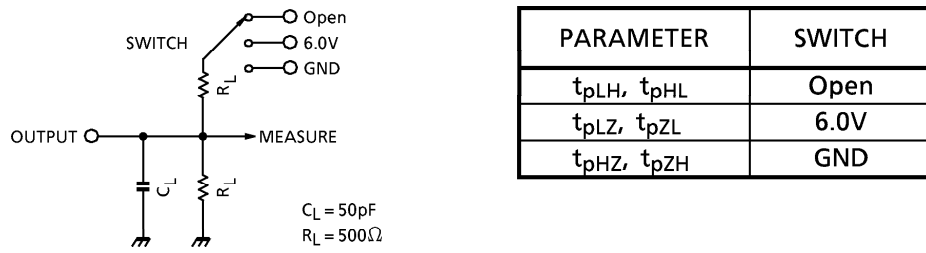
CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP	UNIT
Input Capacitance	C _{IN}	—	3.3	7	pF
Output Capacitance	C _{OUT}		3.3	8	pF
Power Dissipation Capacitance	C _{PD}	f _{IN} = 10MHz (Note 11)	3.3	25	pF

(Note 11) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC} (opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 16. \text{ (Per bit)}$$

Fig.1 Test circuit



AC WAVEFORM

Fig.2 t_{pLH}, t_{pHL}

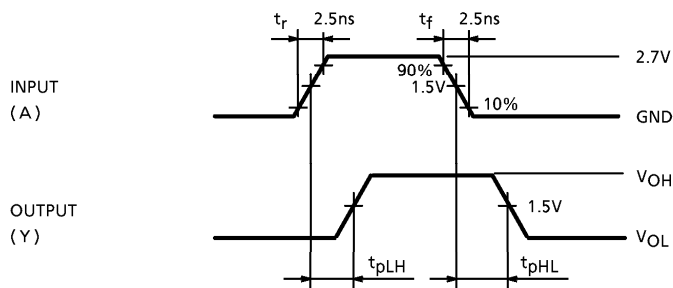
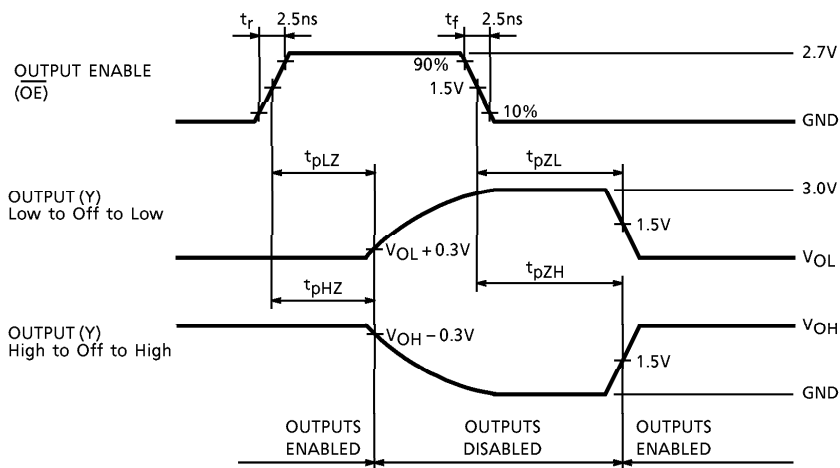


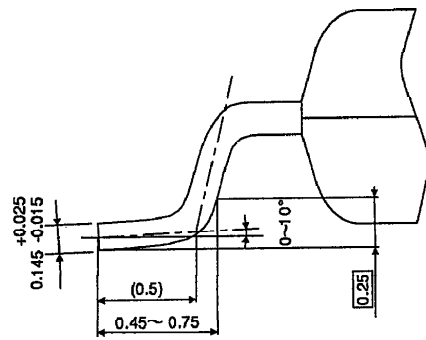
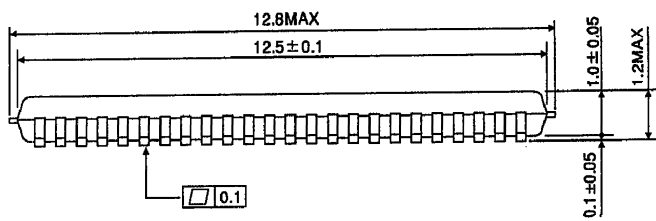
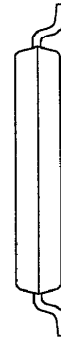
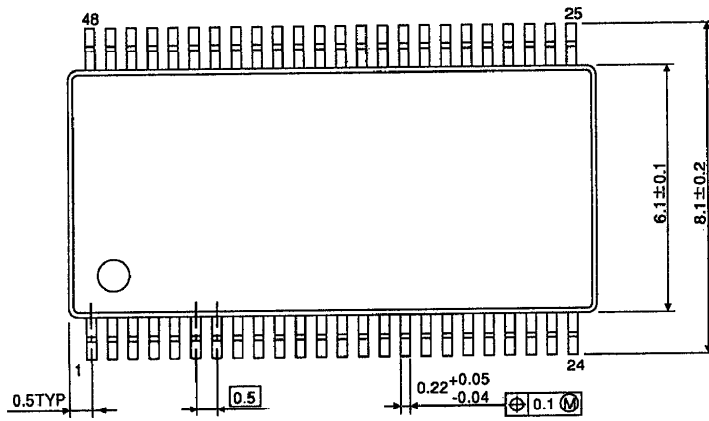
Fig.3 $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$



OUTLINE DRAWING

TSSOP48-P-0061-0.50

Unit : mm



Weight : 0.25g (Typ.)