

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC74HC670AP, TC74HC670AF

## 4 WORD × 4 BIT REGISTER FILE (3 – STATE)

The TC74HC670A is a high speed 4 – WORD<sub>S</sub> × 4 – BIT<sub>S</sub> REGISTER FILE fabricated with silicon gate C2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The register file is organized as 4 words of 4 bits each.

Separate read and write address inputs (RA, RB, and WA, WB) and enable inputs ( $\overline{RE}$ ,  $\overline{WE}$ ) are available permitting simultaneous writing into one word location and reading from another location.

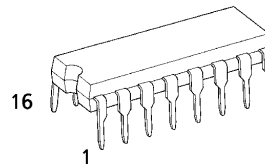
Four data inputs (D0~D3) are provided to store the 4-bit words.

The write address inputs (WA, WB) determine the location of the stored word in the register. When write Enable( $\overline{WE}$ ) is held low, the data is entered into addressed location. When  $\overline{WE}$  is held high, data and address inputs are inhibited. The data acquisition from the four registers is made possible by the read address inputs (RA, RB) when the Read Enable ( $\overline{RE}$ ) is held low. When RE is held high the data outputs are in the high impedance state.

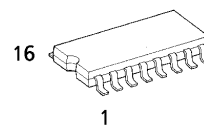
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### FEATURES :

- High Speed..... $t_{pd} = 23ns$  (Typ.)  
at  $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 4\mu A$ (Max.) at  $T_a = 25^\circ C$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 4mA$  (Min.)
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range... $V_{CC}$  (opr.) = 2V~6V
- Pin and Function Compatible with 74LS670

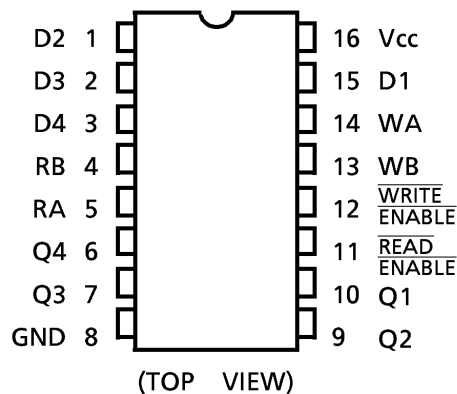


P (DIP16-P-300-2.54A)  
Weight : 1.00g (Typ.)

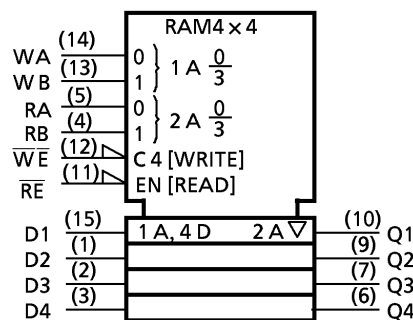


F (SOP16-P-300-1.27)  
Weight : 0.18g (Typ.)

### PIN ASSIGNMENT



### IEC LOGIC SYMBOL



980508EBA2

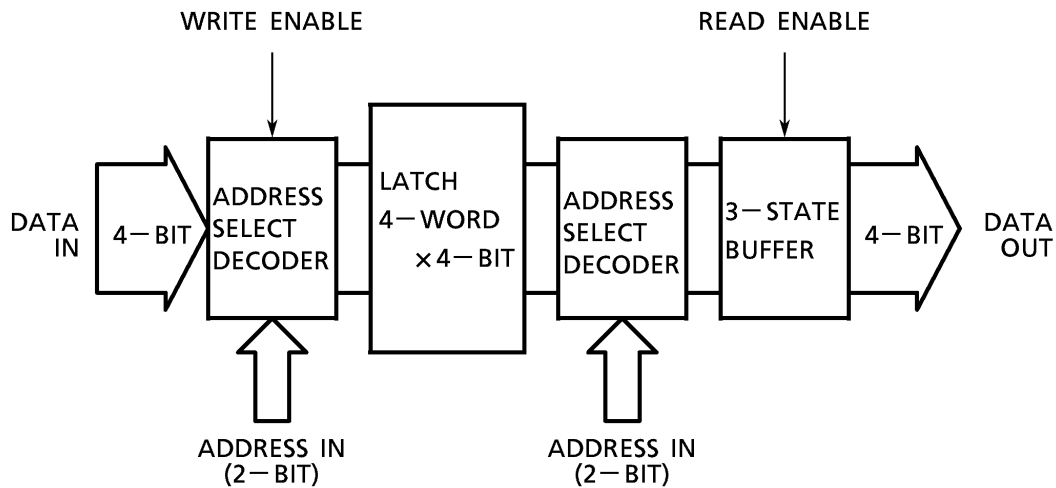
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TRUTH TABLE

WRITE FUNCTION TABLE							READ FUNCTION TABLE						
WRITE INPUTS			WORDS				READ INPUTS			OUTPUTS			
WB	WA	$\overline{WE}$	0	1	2	3	RB	RA	$\overline{RE}$	Q1	Q2	Q3	Q4
L	L	L	Q = D	Q0	Q0	Q0	L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	Q0	Q = D	Q0	Q0	L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	Q0	Q0	Q = D	Q0	H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	Q0	Q0	Q0	Q = D	H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Q0	Q0	Q0	Q0	X	X	H	Z	Z	Z	Z

- NOTES
1. X : Don't Care                      Z : High Impedance
  2. (Q = D) : The four selected internal flip-flop outputs will assume the states applied to the four external data Inputs.
  3. Q0 : The level of Q before the indicated input conditions were established.
  4. W0B1 : The first bit of word 0, etc.

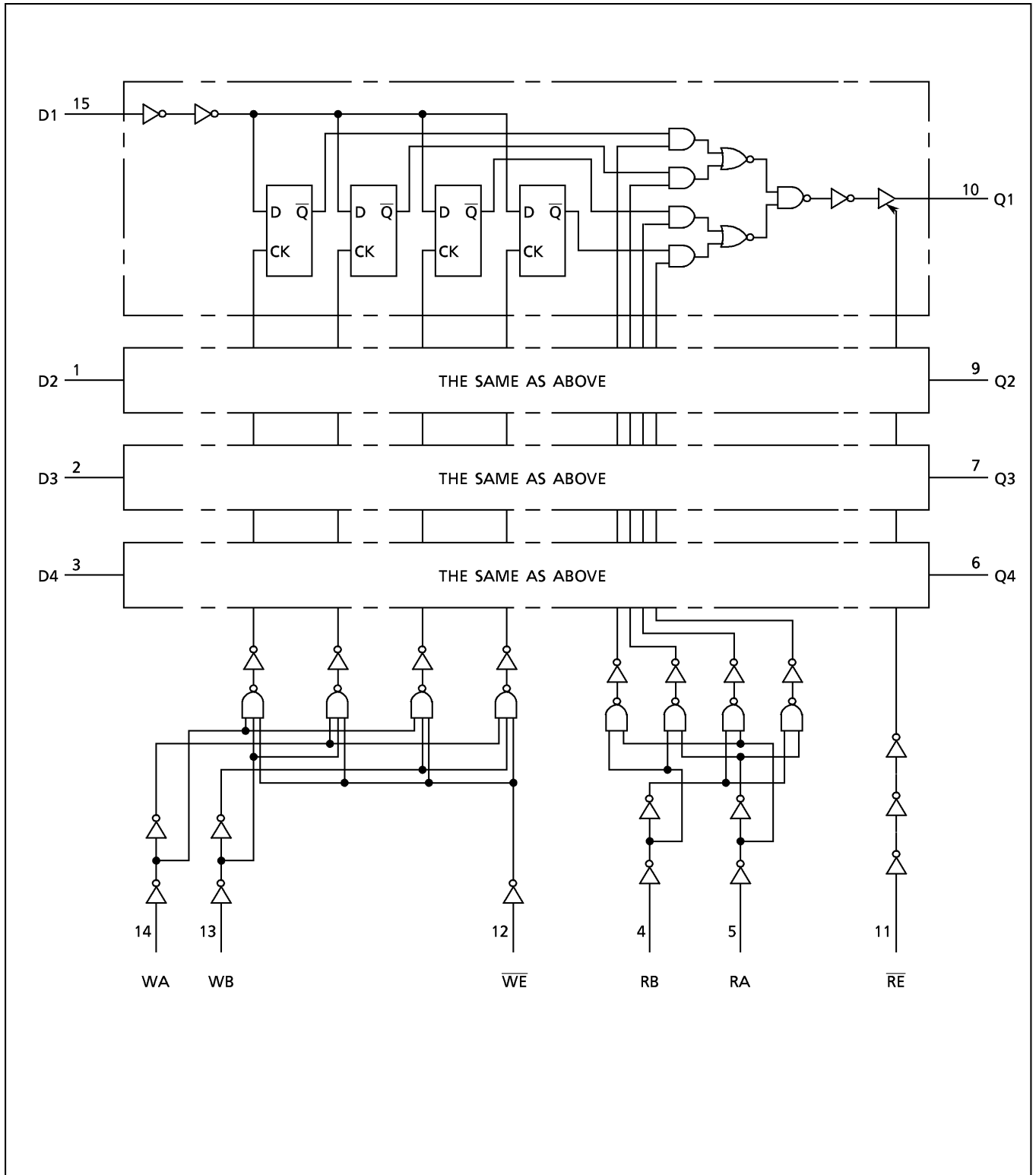
BLOCK DIAGRAM



980508EBA2'

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SYSTEM DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	± 20	mA
Output Diode Current	$I_{OK}$	± 20	mA
DC Output Current	$I_{OUT}$	± 25	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	± 50	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	-65~150	°C

\*500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ . From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  $-10\text{mW}/^{\circ}\text{C}$  should be applied until 300mW.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2~6	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$t_r, t_f$	0~1000 ( $V_{CC} = 2.0\text{V}$ ) 0~500 ( $V_{CC} = 4.5\text{V}$ ) 0~400 ( $V_{CC} = 6.0\text{V}$ )	ns

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT									
				MIN.	TYP.	MAX.	MIN.	MAX.										
High - Level Input Voltage	$V_{IH}$		2.0	1.50	—	—	1.50	—	V									
			4.5	3.15	—	—	3.15	—										
			6.0	4.20	—	—	4.20	—										
Low - Level Input Voltage	$V_{IL}$		2.0	—	—	0.50	—	0.50	V									
			4.5	—	—	1.35	—	1.35										
			6.0	—	—	1.80	—	1.80										
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V								
				4.5	4.4	4.5	—	4.4	—									
				6.0	5.9	6.0	—	5.9	—									
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V								
				4.5	—	0.0	0.1	—	0.1									
				6.0	—	0.0	0.1	—	0.1									
3 - State Output Off - State Current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	6.0	—	—	± 0.5	—	± 5.0	μA									
										Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	± 0.1	—	± 1.0

**TIMING REQUIREMENTS (Input  $t_r = t_f = 6ns$ )**

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C	UNIT
			V <sub>CC</sub> (V)	TYP.	LIMIT	LIMIT	
Minimum Pulse Width ( $\overline{WE}$ )	$t_{w(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (Dn- $\overline{WE}$ )	$t_s$		2.0	—	50	65	
			4.5	—	10	13	
			6.0	—	9	11	
Minimum Set-up Time (WA, WB- $\overline{WE}$ )	$t_s$		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Hold Time (Dn- $\overline{WE}$ )	$t_h$		2.0	—	5	5	
			4.5	—	5	5	
			6.0	—	5	5	
Minimum Hold Time (WA, WB- $\overline{WE}$ )	$t_h$		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Latch Time ( $\overline{WE}$ -RA, RB)	$t_{latch}$	Note(1)	2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	

Note(1):  $t_{latch}$  is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.

**AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 15pF, V<sub>CC</sub> = 5V, Ta = 25°C, Input  $t_r = t_f = 6ns$ )**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	$t_{TLH}$		—	4	8	ns
	$t_{THL}$					
Propagation Delay Time (RA, AB-Qn )	$t_{pLH}$		—	23	34	
	$t_{pHL}$					
Propagation Delay Time ( $\overline{WE}$ -Qn )	$t_{pLH}$		—	24	38	
	$t_{pHL}$					
Propagation Delay Time (Dn-Qn )	$t_{pLH}$		—	22	32	
	$t_{pHL}$					
3-State Output Enable Time	$t_{pZL}$	R <sub>L</sub> = 1kΩ	—	11	18	
	$t_{pZH}$					
3-State Output Disable Time	$t_{pLZ}$	R <sub>L</sub> = 1kΩ	—	11	15	
	$t_{pHZ}$					

AC ELECTRICAL CHARACTERISTICS (  $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C						Ta = -40~85°C		UNIT
			V <sub>CC</sub> (V)	MIN.	TYP.	MAX.	MIN.	MAX.			
Output Transition Time	t <sub>TLH</sub> t <sub>THL</sub>		2.0	—	30	75	—	95	ns		
			4.5	—	8	15	—	19			
			6.0	—	7	13	—	16			
Propagation Delay Time (RA, AB—Qn)	t <sub>pLH</sub> t <sub>pHL</sub>		2.0	—	90	195	—	245	ns		
			4.5	—	27	39	—	49			
			6.0	—	22	33	—	42			
Propagation Delay Time (WE—Qn)	t <sub>pLH</sub> t <sub>pHL</sub>		2.0	—	95	220	—	275	ns		
			4.5	—	28	44	—	55			
			6.0	—	22	37	—	47			
Propagation Delay Time (Dn—Qn)	t <sub>pLH</sub> t <sub>pHL</sub>		2.0	—	90	185	—	230	ns		
			4.5	—	26	37	—	46			
			6.0	—	20	31	—	39			
Output Enable time	t <sub>pZH</sub> t <sub>pZL</sub>	R <sub>L</sub> = 1kΩ	2.0	—	46	110	—	140	ns		
			4.5	—	14	22	—	28			
			6.0	—	12	19	—	24			
Output Disable time	t <sub>pLZ</sub> t <sub>pHZ</sub>	R <sub>L</sub> = 1kΩ	2.0	—	25	95	—	120	ns		
			4.5	—	14	19	—	24			
			6.0	—	12	16	—	20			
Input Capacitance	C <sub>IN</sub>		—	5	10	—	10	pF			
Output Capacitance	C <sub>OUT</sub>		—	10	—	—	—				
Power Dissipation Capacitance	C <sub>PD</sub> (1)		—	101	—	—	—				

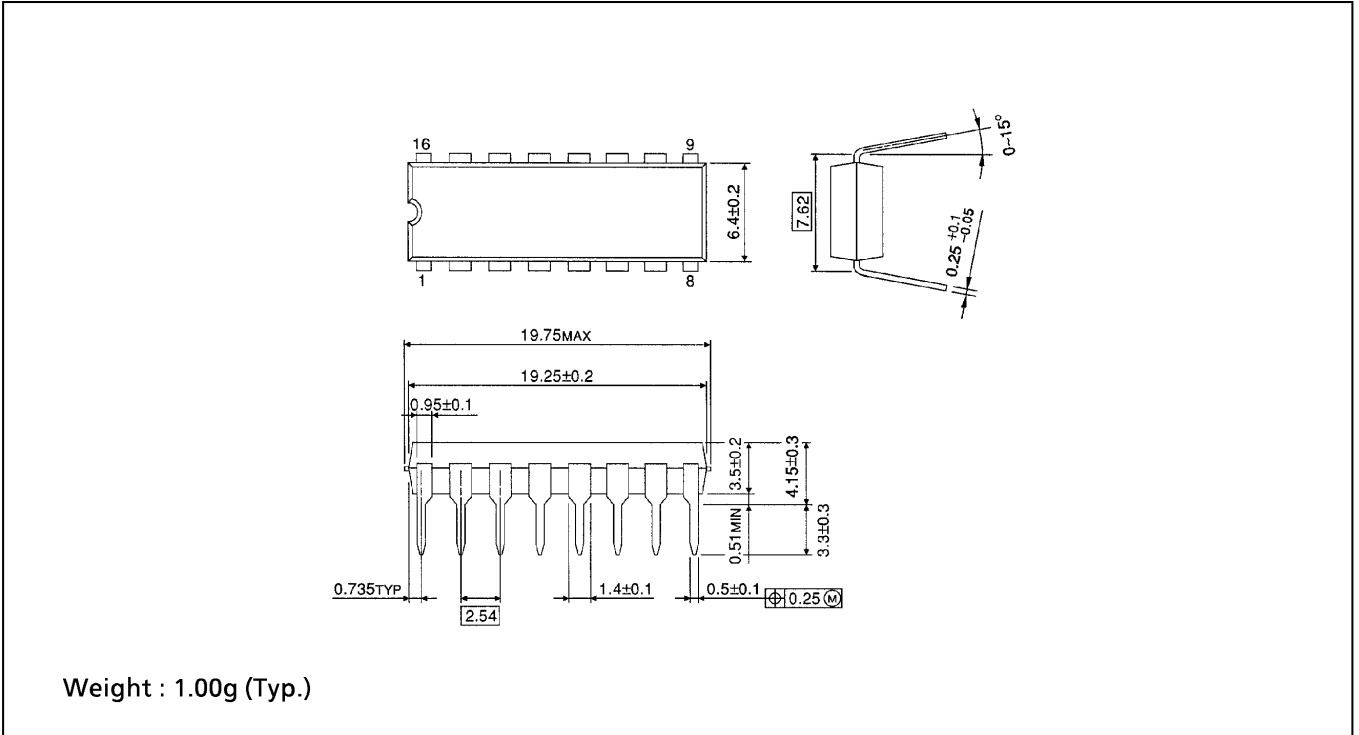
Note(1) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

Unit in mm



SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm

