

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

65,536-WORD BY 16-BIT CMOS STATIC RAM

**DESCRIPTION**

The TC55V1664BJ/BFT is a 1,048,576 bits high speed static random access memory organized as 65,536 words by 16 bits using CMOS technology, and operated from a single 3.3V supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature.

The TC55V1664BJ/BFT has low power feature with device control using chip enable ( $\overline{CE}$ ), and has output enable ( $\overline{OE}$ ) for fast memory access. Also it allows lower and upper byte access by data byte control ( $\overline{LB}$ ,  $\overline{UB}$ ). The TC55V1664BJ/BFT is suitable for use in cache memory where high speed is required, and high speed strage. All inputs and outputs are directly LVTTTL compatible.

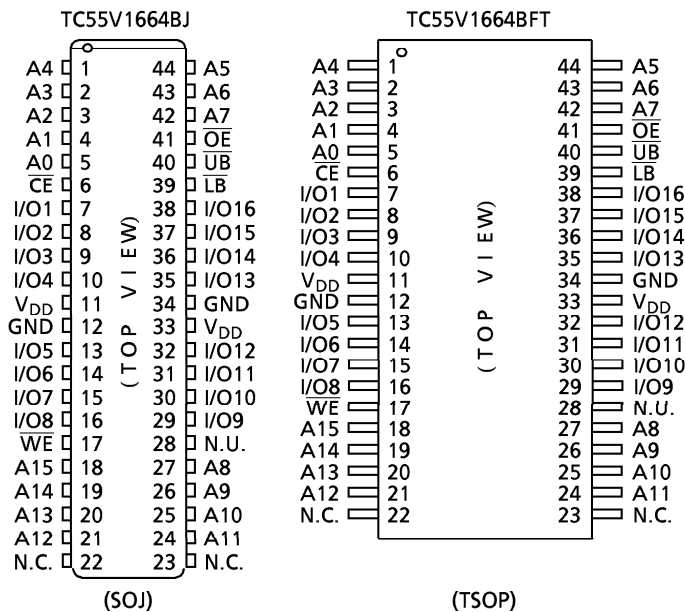
The TC55V1664BJ/BFT is packaged in 44-pin plastic SOJ and TSOP with 400 mil width for high density surface assembly.

**FEATURES**

- Fast access time : TC55V1664BJ/BFT – 8 8ns (MAX)
- Low power dissipation
- 3.3V single power supply : 3.3V ± 5%
- Fully static operation
- All Inputs and Outputs : LVTTTL compatible
- Output buffer control :  $\overline{OE}$
- Data byte control  $\overline{LB}$  (I/O1 to I/O8),  $\overline{UB}$  (I/O9 to I/O16)
- Package: SOJ44-P-400-1.27 (BJ) (Weight : 1.64gm Typ)  
TSOP II 44-P-400-0.80 (BFT) (Weight : 0.45gm Typ)

Cycle Time	8	10	12	15	20	ns
Operation (MAX)	260	230	190	170	150	mA
Standby :						2mA (MAX)

**PIN CONNECTION**



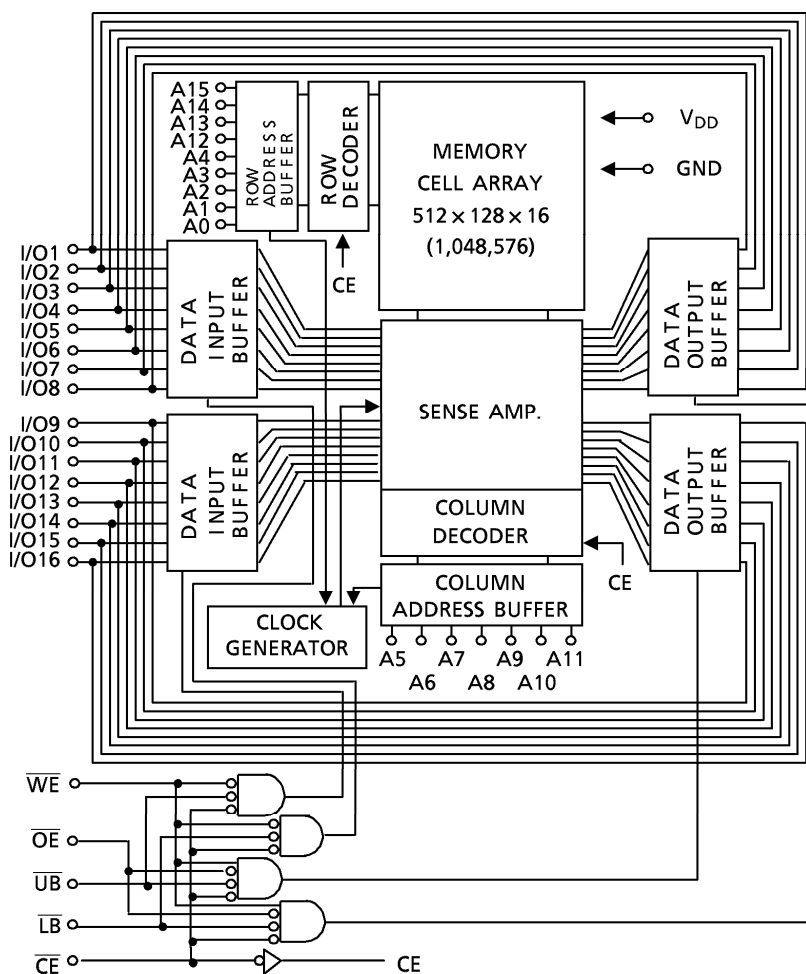
**PIN NAMES**

A0 to A15	Address Inputs
I/O1 to I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$ , $\overline{UB}$	Data Byte Control Inputs
V <sub>DD</sub>	Power (+ 3.3V)
GND	Ground
N.C.	No Connection
N.U.	Not Usable (Input)

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BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.5 to 4.6	V
V <sub>IN</sub>	Input Terminal Voltage	-0.5* to 4.6	V
V <sub>I/O</sub>	Input/Output Terminal Voltage	-0.5* to V <sub>DD</sub> + 0.5**	V
P <sub>D</sub>	Power Dissipation	0.95	W
T <sub>solder</sub>	Soldering Temperature (10s)	260	°C
T <sub>strg</sub>	Storage Temperature	-65 to 150	°C
T <sub>opr</sub>	Operating Temperature	-10 to 85	°C

\* : -1.5V with a pulse width of 20% · t<sub>RC</sub> min (4ns max)  
 \*\* : V<sub>DD</sub> + 1.5V with a pulse width of 20% · t<sub>RC</sub> min (4ns max)

**DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>DD</sub>	Power Supply Voltage	3.0	3.3	3.6	V
V <sub>IH</sub>	Input High Voltage	2.0	-	V <sub>DD</sub> + 0.3**	V
V <sub>IL</sub>	Input Low Voltage	-0.3*	-	0.8	V

\* : -1.0V with a pulse width of 20% · t<sub>RC</sub> min (4ns max)  
 \*\* : V<sub>DD</sub> + 1.0V with a pulse width of 20% · t<sub>RC</sub> min (4ns max)

**DC and OPERATING CHARACTERISTICS (Ta = 0° to 70°C, V<sub>DD</sub> = 3.3V ± 5%)**

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
I <sub>IL</sub>	Input Leakage Current (Except NU pin)	V <sub>IN</sub> = 0 to V <sub>DD</sub>	-1	-	1	μA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ V <sub>OUT</sub> = 0 to V <sub>DD</sub>	-1	-	1	μA	
I <sub>I(NU)</sub>	Input Current (NU pin)	V <sub>IN</sub> = 0 to 0.8V	-1	-	20	μA	
		V <sub>IN</sub> = 0 to 0.2V	-1	-	1		
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -2mA	2.4	-	-	V	
		I <sub>OH</sub> = -100μA	V <sub>DD</sub> - 0.2	-	-		
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2mA	-	-	0.4		
		I <sub>OL</sub> = 100μA	-	-	0.2		
I <sub>DDO</sub>	Operating Current	$\overline{CE} = V_{IL}$ , I <sub>out</sub> = 0mA Other Inputs = V <sub>IH</sub> / V <sub>IL</sub>	t <sub>cycle</sub> = 8ns	-	-	260	mA
			t <sub>cycle</sub> = 10ns	-	-	230	
			t <sub>cycle</sub> = 12ns	-	-	190	
			t <sub>cycle</sub> = 15ns	-	-	170	
			t <sub>cycle</sub> = 20ns	-	-	150	
I <sub>DDS1</sub>	Standby Current	$\overline{CE} = V_{IH}$ , Other Inputs = V <sub>IH</sub> / V <sub>IL</sub>	-	-	50	mA	
I <sub>DDS2</sub>		$\overline{CE} = V_{DD} - 0.2V$ Other Inputs = V <sub>DD</sub> - 0.2V or 0.2V	-	-	2		

**CAPACITANCE (Ta = 25°C, f = 1.0MHz)**

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	6	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>I/O</sub> = GND	8	pF

NOTE : This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	POWER
Read	L	L	H	L	L	Output	Output	I <sub>DDO</sub>
				H	L	High Impedance	Output	I <sub>DDO</sub>
				L	H	Output	High Impedance	I <sub>DDO</sub>
Write	L	X	L	L	L	Input	Input	I <sub>DDO</sub>
				H	L	High Impedance	Input	I <sub>DDO</sub>
				L	H	Input	High Impedance	I <sub>DDO</sub>
Outputs Disable	L	H	H	X	X	High Impedance	High Impedance	I <sub>DDO</sub>
	L	X	X	H	H			
Standby	H	X	X	X	X	High Impedance	High Impedance	I <sub>DDs</sub>

X : H or L

NOTE : N.U. pin must be kept open electrically or pulled down to GND level or less than 0.8V.  
Applying a voltage more than 0.8V to N.U. pin is prohibited.

**AC CHARACTERISTICS** ( $T_a = 0^\circ$  to  $70^\circ\text{C}$  <sup>(1)</sup>,  $V_{DD} = 3.3\text{V} \pm 5\%$ )

**READ CYCLE**

SYMBOL	PARAMETER	TC55V1664BJ/BFT-8		UNIT
		MIN	MAX	
$t_{RC}$	Read Cycle Time	8	–	ns
$t_{ACC}$	Address Access Time	–	8	
$t_{CO}$	$\overline{CE}$ Access Time	–	8	
$t_{OE}$	$\overline{OE}$ Access Time	–	4	
$t_{BA}$	$\overline{UB}, \overline{LB}$ Access Time	–	4	
$t_{OH}$	Output Data Hold Time from Address Change	3	–	
$t_{COE}$	Output Enable Time from $\overline{CE}$	3	–	
$t_{OEE}$	Output Enable Time from $\overline{OE}$	1	–	
$t_{BE}$	Output Enable Time from $\overline{UB}, \overline{LB}$	1	–	
$t_{COD}$	Output Disable Time from $\overline{CE}$	–	5	
$t_{ODO}$	Output Disable Time from $\overline{OE}$	–	5	
$t_{BD}$	Output Disable Time from $\overline{UB}, \overline{LB}$	–	5	

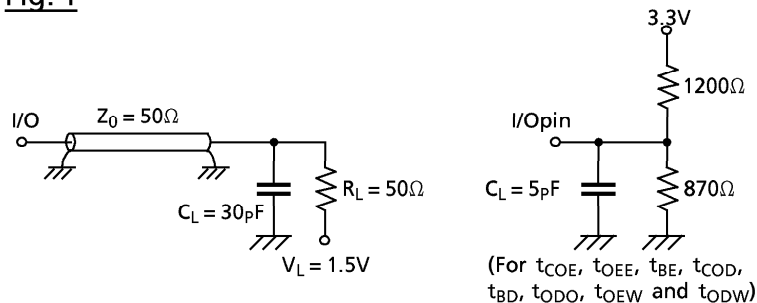
**WRITE CYCLE**

SYMBOL	PARAMETER	TC55V1664BJ/BFT-8		UNIT
		MIN	MAX	
$t_{WC}$	Write Cycle Time	8	–	ns
$t_{WP}$	Write Pulse Width	6	–	
$t_{CW}$	Chip Enable to End of Write	7	–	
$t_{BW}$	$\overline{UB}, \overline{LB}$ Enable to End of Write	7	–	
$t_{AW}$	Address Valid to End of Write	7	–	
$t_{AS}$	Address Set Up Time	0	–	
$t_{WR}$	Write Recovery Time	0	–	
$t_{DS}$	Data Set Up Time	5	–	
$t_{DH}$	Data Hold Time	0	–	
$t_{OEW}$	Output Enable Time from $\overline{WE}$	1	–	
$t_{ODW}$	Output Disable Time from $\overline{WE}$	–	5	

**AC TEST CONDITIONS**

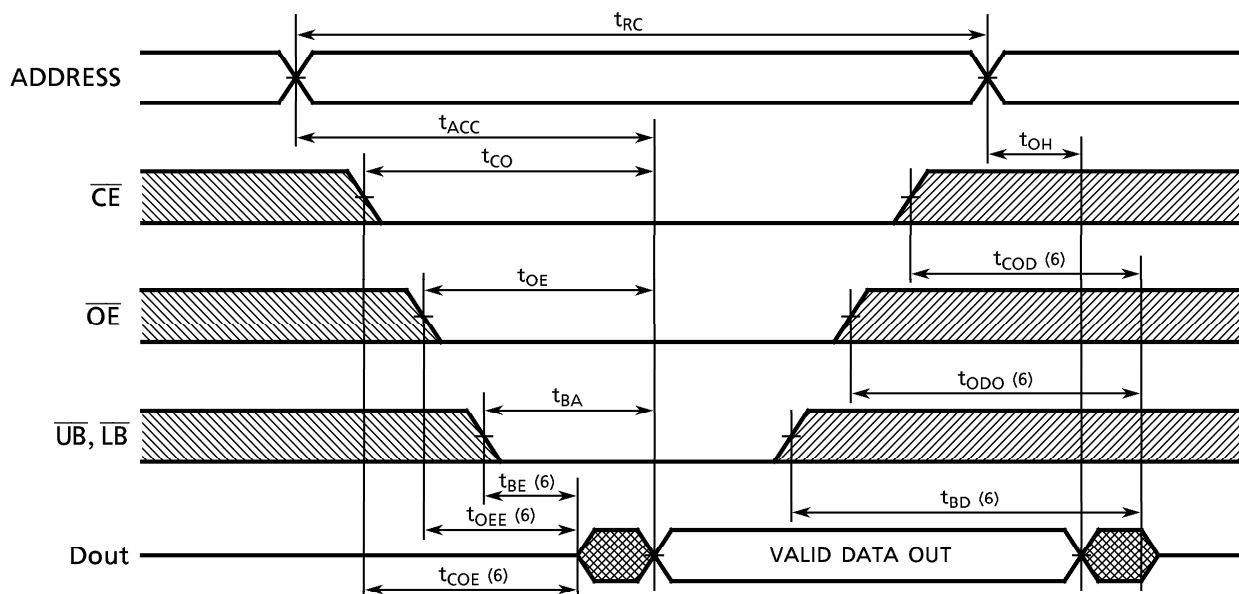
Input Pulse Level	3.0V/0.0V
Input Pulse Rise and Fall Time	2ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

**Fig. 1**

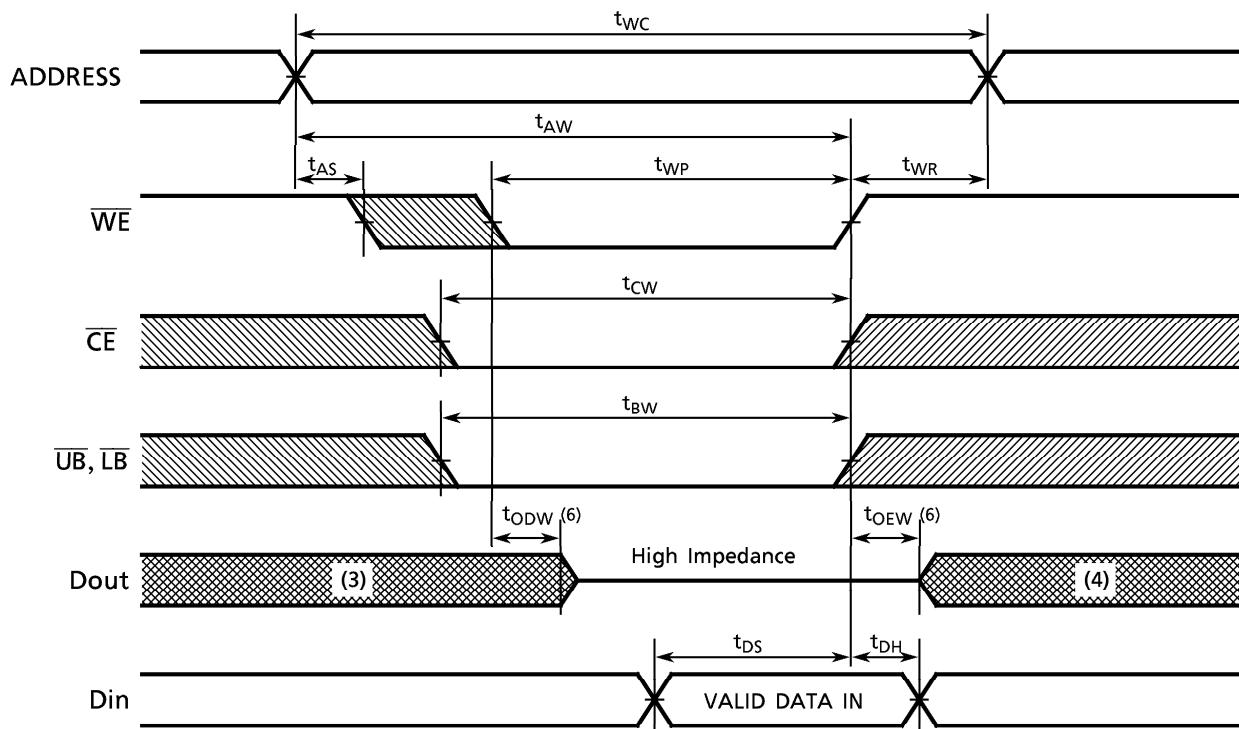


**TIMING WAVEFORMS**

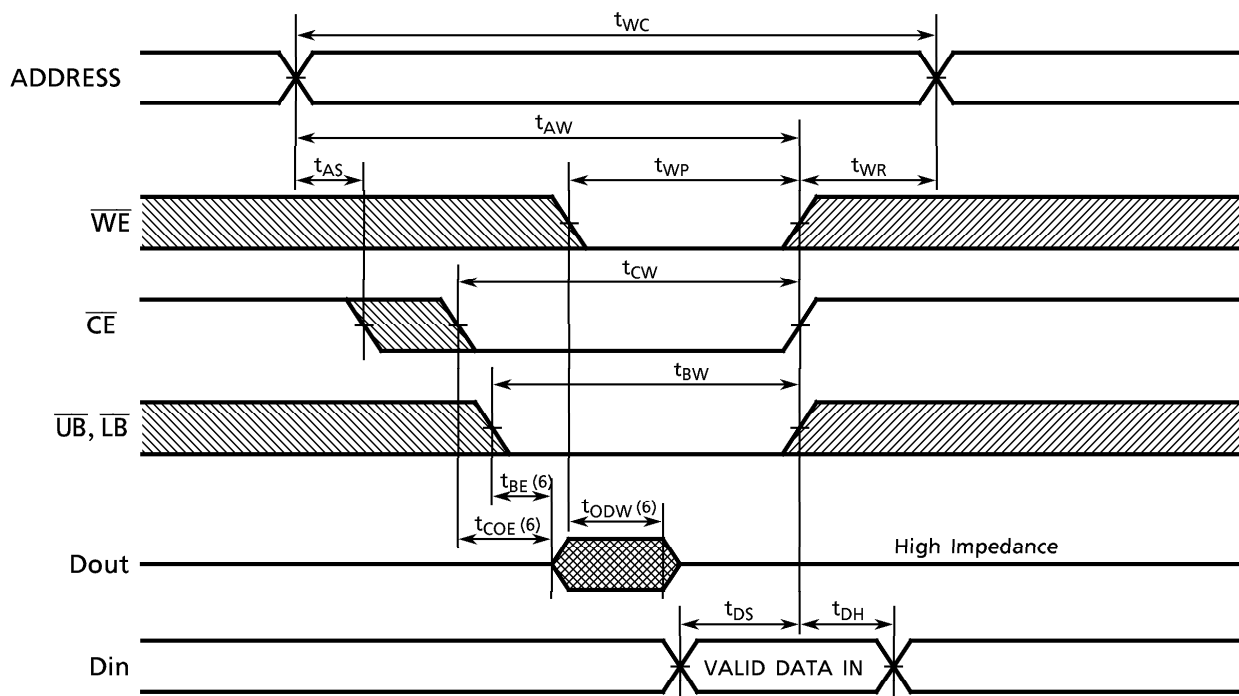
**READ CYCLE (2)**



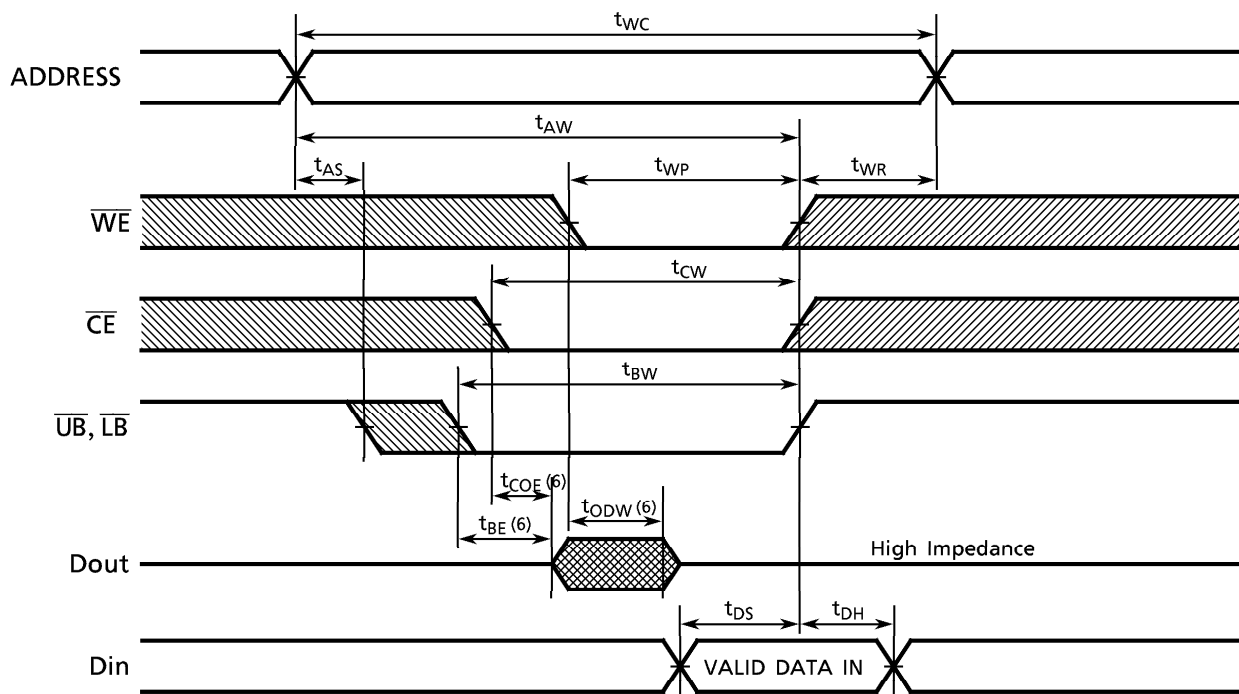
**WRITE CYCLE 1 (5) ( $\overline{WE}$  Controlled)**



WRITE CYCLE 2 (5) ( $\overline{CE}$  Controlled)



WRITE CYCLE 3 (5) ( $\overline{UB}$ ,  $\overline{LB}$  Controlled)

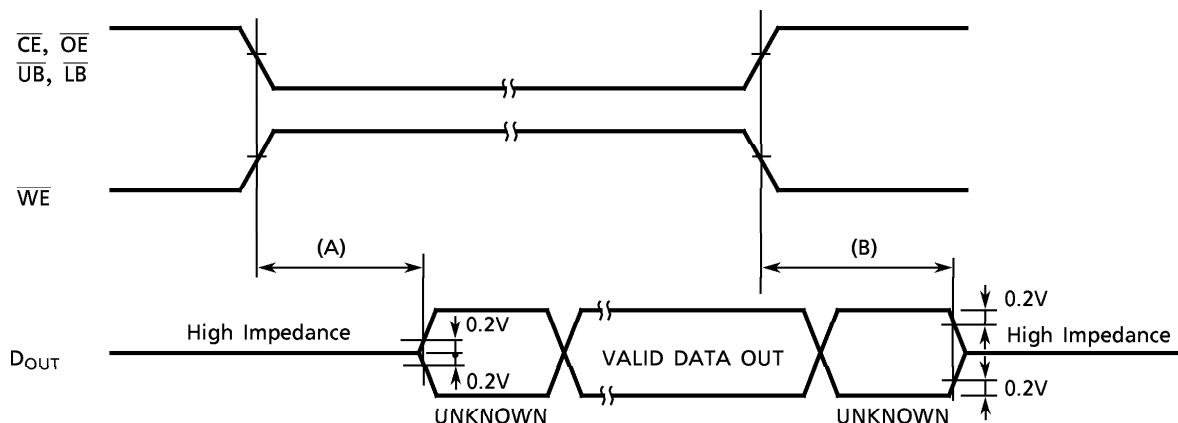


NOTE :

1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2.  $\overline{WE}$  is High for Read Cycle.
3. Assuming that  $\overline{CE}$  Low transition occurs coincident with or after  $\overline{WE}$  Low transition, Outputs remain in a high impedance state.
4. Assuming that  $\overline{CE}$  High transition occurs coincident with or prior  $\overline{WE}$  High transition, Outputs remain in a high impedance state.
5. Assuming that  $\overline{OE}$  is High for Write Cycle, Outputs are in a high impedance state during this period.
6. These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A)  $t_{COE}, t_{OEE}, t_{BE}, t_{OEW}$       ..... Output Enable Time

(B)  $t_{COD}, t_{ODO}, t_{BD}, t_{ODW}$       ..... Output Disable Time

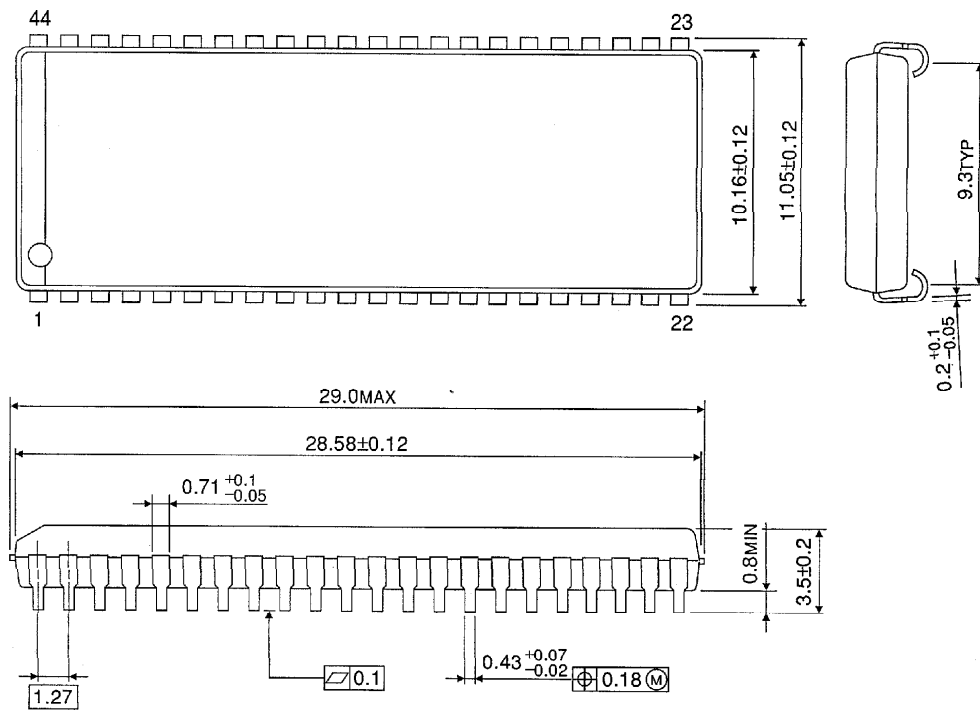




## PACKAGE DIMENSIONS

Plastic SOJ (SOJ44-P-400-1.27)

Unit in mm

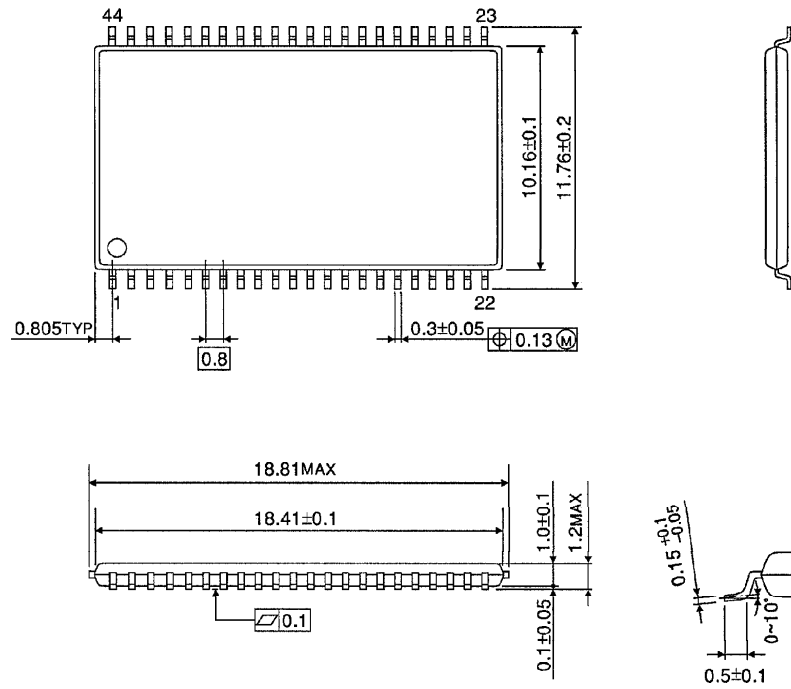


Weight : 1.64g (Typ)

**PACKAGE DIMENSIONS**

Plastic TSOP (TSOPII 44-P-400-0.80)

Unit in mm



Weight : 0.45g (Typ)