

## TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288 WORDS × 8 BIT STATIC RAM

### DESCRIPTION

The TC554001FL/FTL is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5V ± 10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 10mA/MHz(typ) and minimum cycle time of 70 ns. It is automatically placed in low-power mode at 100 μA standby current (max) when chip enable (CE) is asserted high. There are two control inputs. CE is used to select the device and for data retention control, and output enable (OE) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. The TC554001FL/FTL is available in a standard plastic 32-pin small-outline package(SOP) and 32-pin thin-small-outline package(TSOP).

### FEATURES

- Low-power dissipation  
Operating: 55 mW/MHz (typical)
- Standby current of 100 μA (maximum)
- Single power supply voltage of 5 V ± 10 %
- Power down features using CE
- Data retention supply voltage of 2.0 to 5.5 V
- Direct TTL compatibility for all inputs and outputs

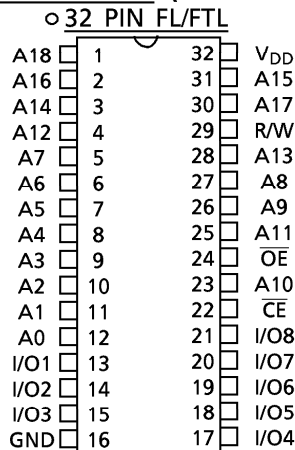
- Access Time (maximum)

	TC554001FL/FTL		
	-70	-85	-10
Access Time	70 ns	85 ns	100 ns
CE Access Time	70 ns	85 ns	100 ns
OE Access Time	35 ns	45 ns	50 ns

- Package:

SOP32-P-525-1.27 (FL) (Weight: 1.14 g typ)  
 TSOP II 32-P-400-1.27 (FTL) (Weight: 0.51 g typ)

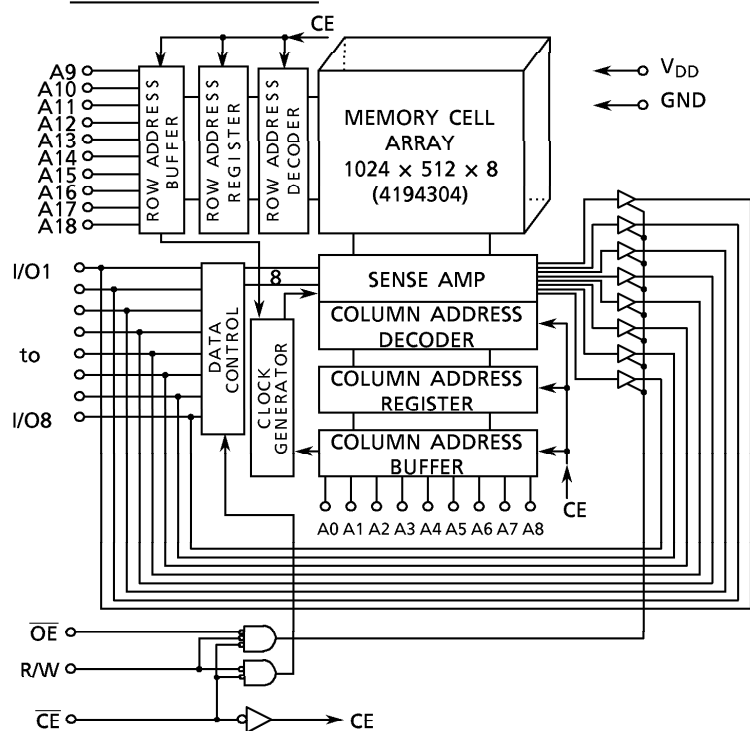
### PIN ASSIGNMENT (TOP VIEW)



### PIN NAMES

A0 to A18	Address Inputs
R/W	Read/Write Control
OE	Output Enable
CE	Chip Enable
I/O1 to I/O8	Data Input/Output
V <sub>DD</sub>	Power (+ 5 V)
GND	Ground

### BLOCK DIAGRAM



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**OPERATION MODE**

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 to I/O8	POWER
Read	L	L	H	D <sub>OUT</sub>	I <sub>DDO</sub>
Write	L	x	L	D <sub>IN</sub>	I <sub>DDO</sub>
Output Disabled	L	H	H	High-Z	I <sub>DDO</sub>
Standby	H	x	x	High-Z	I <sub>DDS</sub>

Note: X = don't care. H = logic high. L = logic low.

**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	RATING	VALUE	UNIT
V <sub>DD</sub>	Power Supply Voltage	- 0.3 to 7.0	V
V <sub>IN</sub>	Input Voltage	- 0.3* to 7.0	V
V <sub>I/O</sub>	Input and Output Voltage	- 0.5 to V <sub>DD</sub> + 0.5	V
P <sub>D</sub>	Power Dissipation	0.6	W
T <sub>solder</sub>	Soldering Temperature (10 s)	260	°C
T <sub>strg.</sub>	Storage Temperature	- 55 to 150	°C
T <sub>opr.</sub>	Operating Temperature	0 to 70	°C

\* - 3.0 V when measured at a pulse width of 50 ns

**DC RECOMMENDED OPERATING CONDITIONS** (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	–	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage	– 0.3*	–	0.8	V
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	–	5.5	V

\* – 3.0 V when measured at a pulse width of 50 ns

**DC CHARACTERISTICS** (Ta = 0° to 70°C, V<sub>DD</sub> = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT		
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V to V <sub>DD</sub>	–	–	± 1.0	μA		
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4 V	– 1.0	–	–	mA		
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V	2.1	–	–	mA		
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V <sub>IL</sub> or $\overline{OE} = V_{IH}$ V <sub>OUT</sub> = 0 V to V <sub>DD</sub>	–	–	± 1.0	μA		
I <sub>DDO1</sub>	Operating Current	$\overline{CE} = V_{IL}$ and R/W = V <sub>IH</sub> I <sub>OUT</sub> = 0 mA Other Inputs = V <sub>IH</sub> /V <sub>IL</sub>	Tcycle	min	–	–	80	mA
I <sub>DDO2</sub>		$\overline{CE} = 0.2 V$ and R/W = V <sub>DD</sub> – 0.2 V I <sub>OUT</sub> = 0 mA Other Inputs = V <sub>DD</sub> – 0.2 V/0.2 V		min	–	–	70	
I <sub>DDS1</sub>	Standby Current	$\overline{CE} = V_{IH}$	–	–	3	mA		
I <sub>DDS2</sub>		$\overline{CE} = V_{DD} - 0.2 V$ V <sub>DD</sub> = 2.0 to 5.5 V, Ta = 0° to 70°C	–	–	100	μA		

**CAPACITANCE** (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

**AC CHARACTERISTICS AND OPERATING CONDITIONS** ( $T_a = 0^\circ$  to  $70^\circ\text{C}$ ,  $V_{DD} = 5\text{ V} \pm 10\%$ )

**READ CYCLE**

SYMBOL	PARAMETER	TC554001FL/FTL						UNIT
		-70		-85		-10		
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{RC}$	Read Cycle Time	70	-	85	-	100	-	ns
$t_{ACC}$	Address Access Time	-	70	-	85	-	100	
$t_{CO}$	Chip Enable Access Time	-	70	-	85	-	100	
$t_{OE}$	Output Enable Access Time	-	35	-	45	-	50	
$t_{COE}$	Chip Enable Low to Output Active	10	-	10	-	10	-	
$t_{OEE}$	Output Enable Low to Output Active	5	-	5	-	5	-	
$t_{OD}$	Chip Enable High to Output High-Z	-	25	-	30	-	35	
$t_{ODO}$	Output Enable High to Output High-Z	-	25	-	30	-	35	
$t_{OH}$	Output Data Hold Time	10	-	10	-	10	-	

**WRITE CYCLE**

SYMBOL	PARAMETER	TC554001FL/FTL						UNIT
		-70		-85		-10		
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{WC}$	Write Cycle Time	70	-	85	-	100	-	ns
$t_{WP}$	Write Pulse Width	50	-	55	-	60	-	
$t_{CW}$	Chip Enable to End of Write	60	-	70	-	80	-	
$t_{AS}$	Address Setup Time	0	-	0	-	0	-	
$t_{WR}$	Write Recovery Time	0	-	0	-	0	-	
$t_{ODW}$	R/W Low to Output High-Z	-	25	-	30	-	35	
$t_{OEW}$	R/W High to Output Active	5	-	5	-	5	-	
$t_{DS}$	Data Setup Time	30	-	35	-	40	-	
$t_{DH}$	Data Hold Time	0	-	0	-	0	-	

**AC TEST CONDITIONS**

Output Load: 30 pF + one TTL gate (-70)

100 pF + one TTL gate (-85, -10)

Input Pulse Level: 0.6 V, 2.4 V

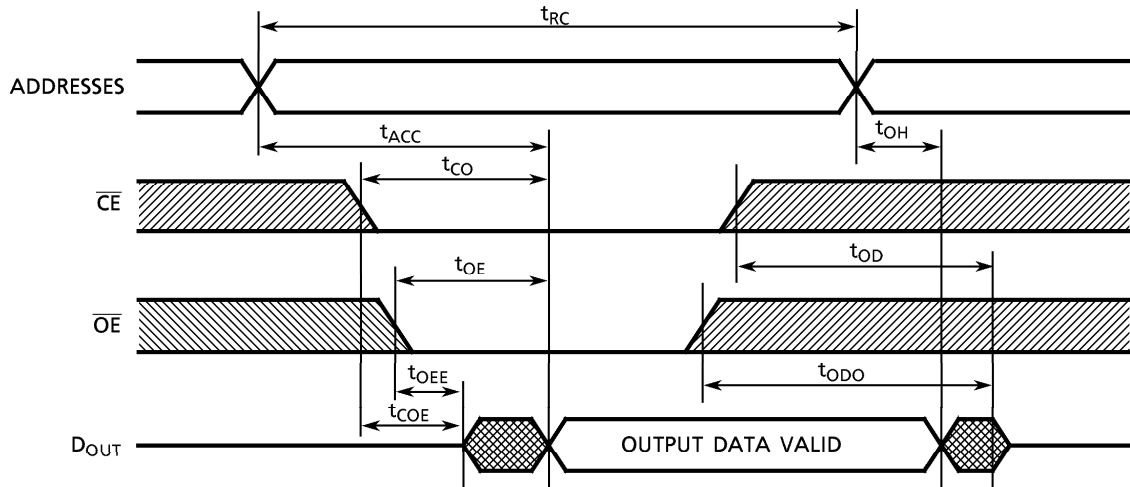
Timing Measurements: 1.5 V

Reference Level: 1.5 V

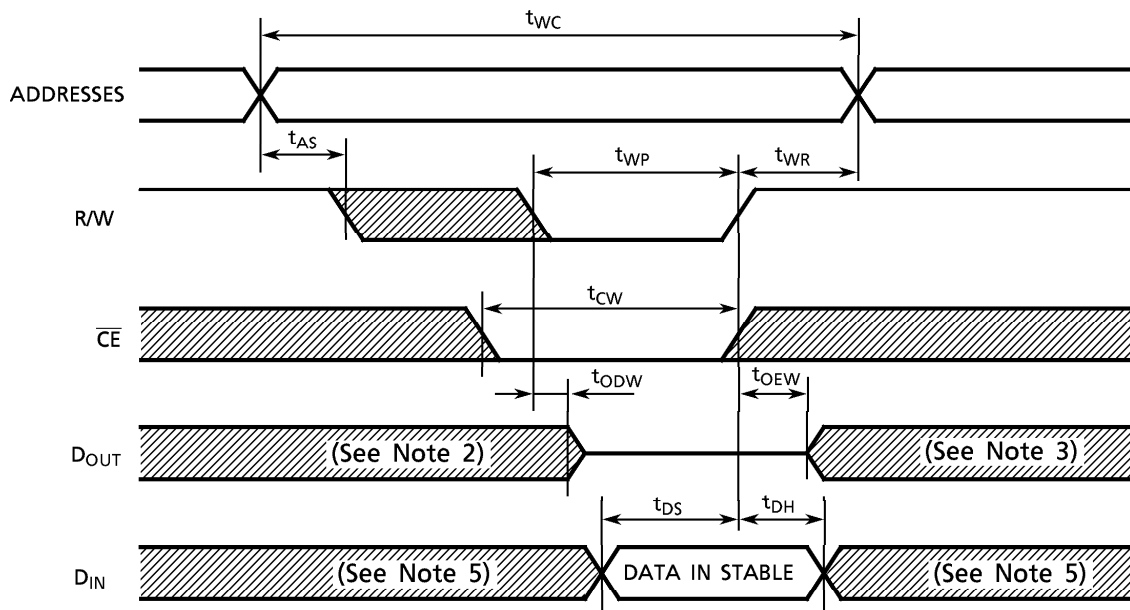
$t_r, t_f$ : 5 ns

**TIMING WAVEFORMS**

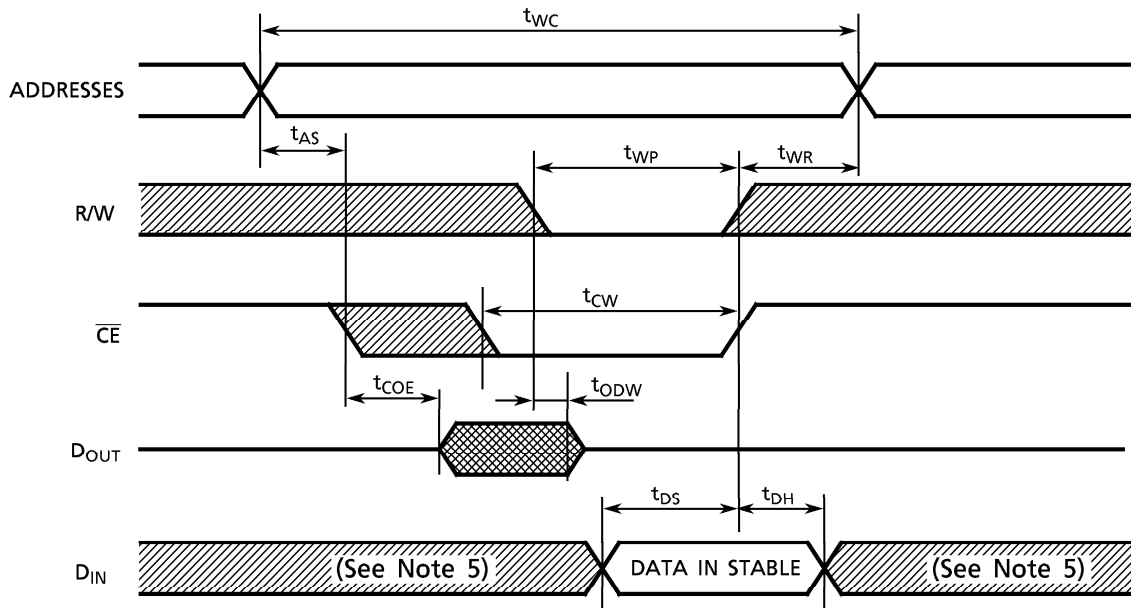
**READ CYCLE (See Note 1)**



**WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)**



WRITE CYCLE 2 ( $\overline{CE}$  CONTROLLED) (See Note 4)

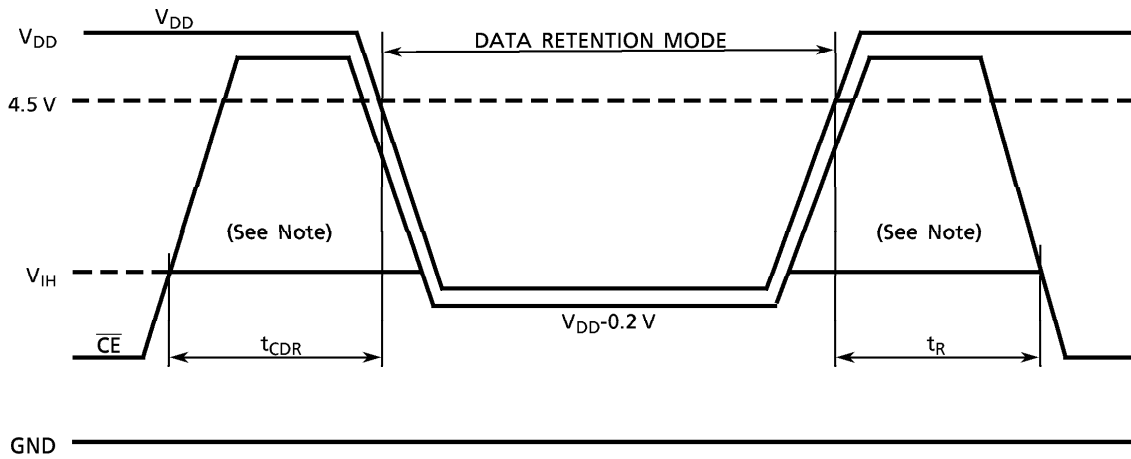


- (1) R/W remains High for Read Cycle.
- (2) If  $\overline{CE}$  goes coincident with or after R/W goes LOW, the output will remain at high impedance.
- (3) If  $\overline{CE}$  goes HIGH coincident with or before R/W goes HIGH, the output will remain at high impedance.
- (4) IF  $\overline{CE}$  is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

**DATA RETENTION CHARACTERISTICS (Ta = 0° to 70°C)**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	–	5.5	V
I <sub>DDS2</sub>	Standby Current	V <sub>DH</sub> = 3.0 V	–	50	μA
		V <sub>DH</sub> = 5.5 V	–	100	
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode Time	0	–	–	nS
t <sub>R</sub>	Recovery Time	5	–	–	mS

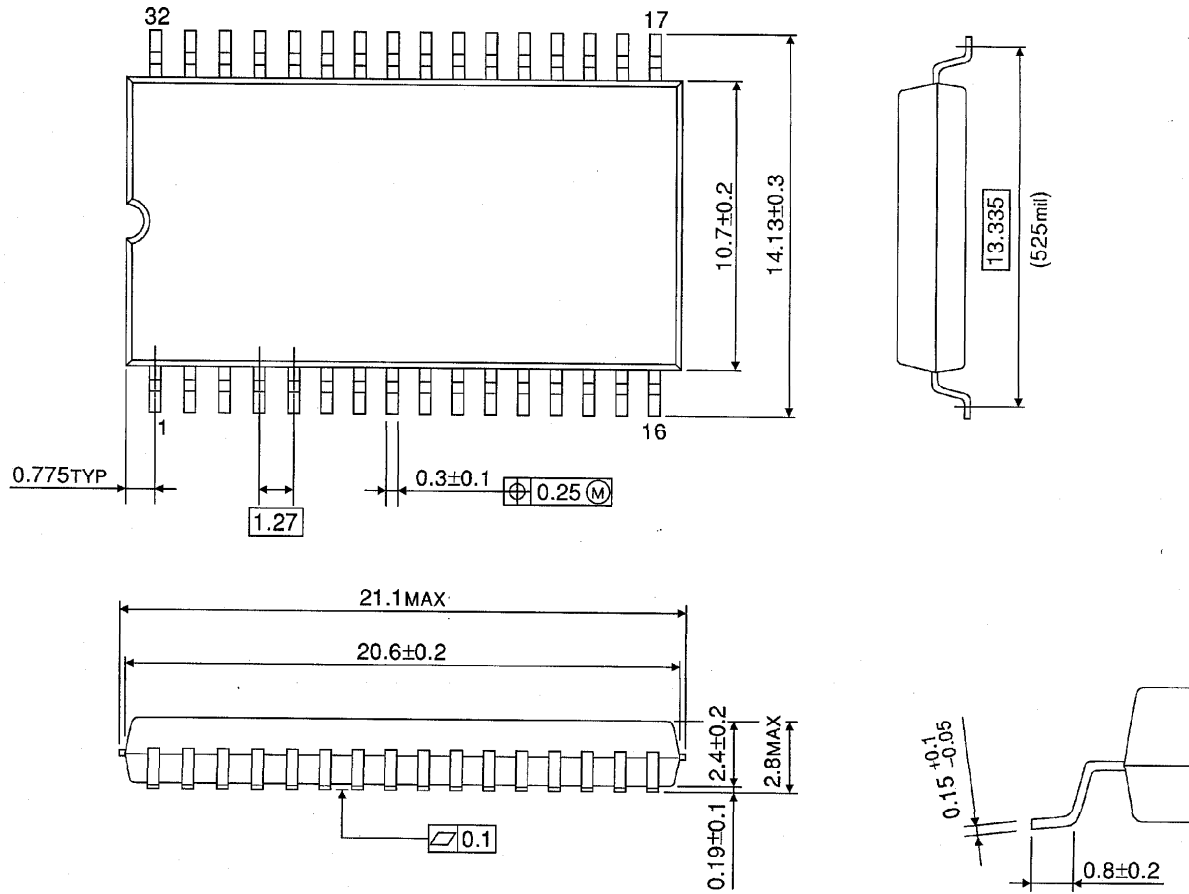
**CE Controlled Data Retention Mode**



Note: When  $\overline{CE}$  is operating at the  $V_{IH}$  level (2.2V), the standby current is given by  $I_{DDS1}$  during the transition of  $V_{DD}$  from 4.5 to 2.4V.

PACKAGE DIMENSIONS (SOP32-P-525-1.27)

Unit in mm

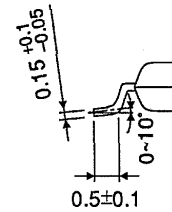
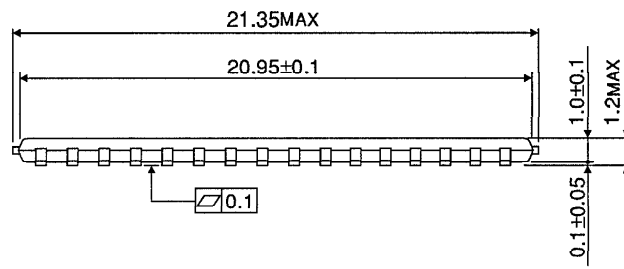
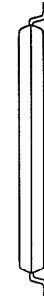
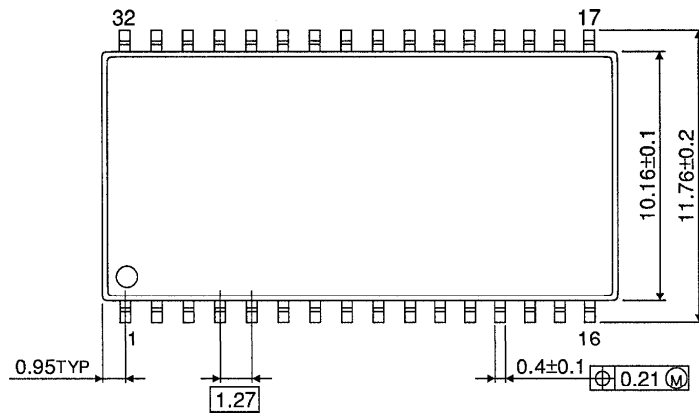


Weight: 1.14 g (typ)



PACKAGE DIMENSIONS (TSOPII 32-P-400-1.27)

Unit in mm



Weight: 0.51 g (typ)