TEXAS INSTRUMENTS

TSB42AA4/42AA4I
TSB42AB4/42AB4I (ceLynx)

IEEE 1394.a Consumer Electronics Link Layer Controller

Data Manual

September 2003

Mixed Signal Products

SLLS341F

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1 Introduction

1.1 Device Package Information

ORDERING NUMBER	NAME	VOLTAGE	PACKAGE
TSB42AA4PDT TSB42AA4IPDT	ceLynx	3.3 V	PQFP 128
TSB42AB4PDT TSB42AB4IPDT	ceLynx-DV	3.3 V	PQFP 128
TSB42AA4PGE	ceLynx	3.3 V	PQFP 144
TSB42AB4PGE	ceLynx-DV	3.3 V	PQFP 144

1.2 References

The following sources of information were used in the generation of this document:

- *IEEE Standard for a High Performance Serial Bus,* IEEE Standard 1394−1995 and IEEE Standard 1394a−2000
- *Digital Interface for Consumer Audio/Video Equipment,* IEC Document 61883
- *Open Cable™, Home Digital Network (HDND) 1394 Interface Specification, Version 2.0*
- 1394 TA Document 1998017, ITU-R BO 1294 System B Signal Transmission 1.0

Open Cable is a registered trademark of CableLabs.

2 ceLynx Overview

2.1 ceLynx Description

Consumer Electronics Link (ceLynx) is a high-performance 1394 link layer device designed specifically to support advanced consumer electronics applications, particularly those applications which require the transmission of Moving Picture Expert Group 2 (MPEG2) transport streams and encryption/decryption of those streams across a 1394 network. The device supports both digital video broadcasting (DVB) and DirecTV™ type MPEG2 streams using the digital transmission content protection method (DTCP) method of encryption, as well as digital video (DV) encoded streams. The ceLynx supports both the IEC 61883 standard for DVB and DV streams over 1394 and the 1394 Trade Association standard for DirecTV over 1394.

The ceLynx is also versatile enough to handle asynchronous data and asynchronous streams. A key feature of the ceLynx is its ability to handle multiple data type streams simultaneously; the user may transport DVB, DirecTV, DV data streams, and asynchronous data *simultaneously.* The ceLynx can also support multiple streams of the same data type simultaneously, (for example, transmit or receive two DVB transport streams or two DV streams).

The ceLynx is full duplex, allowing simultaneous playback and recording of audio/video data. Full duplex support also includes the capability of using the DTCP method, simultaneously using the two embedded M6 cipher modules. The large internal 8-Kbyte FIFO is very flexible, allowing the user to partition it into eight independent first in first out (FIFOs) and allowing the user to determine the exact configuration of each of these FIFOs to fit the application. Advanced features have been added to support program ID (PID) filtering and packet insertions.

The ceLynx is also designed to interface seamlessly with popular MPEG2 decoder chipsets. This decreases the design-in effort of customers when using these popular chipsets.

2.2 Key Features

- DTCP content protection (TSB42AA4 only). A separate document explains the DTCP hardware errata for TSB42AA4. It is available upon request to DTLA licensees only.
- Interfaces directly to industry standard 400-, 200-, and 100-Mbps physical layer devices, including Texas Instruments TSB41LV0X and TSB41AXX family of physical layer devices
- Compliant with IEEE 1394-1995 and IEEE 1394a−2000 standards
- MPEG2 time stamp-based release, as described in IEC 61883-4
- High-speed data interface (HSDI):
  - Byte-wide or serial mode
  - Two independent HSDI ports
  - Bidirectional
  - Several control modes for a variety of applications
  - Connects seamlessly to common MPEG2 decoder chipsets
- 16-bit microprocessor interface supports Motorola 68000/68020-style bus
- Large 8K-byte FIFO can be configured up to eight independent Tx or Rx FIFOs
- 8K-byte FIFO supports the following data types:
  - DVB MPEG2 transport streams (IEC 61883-4)
  - DirecTV transport streams

DirecTV is a trademark of Hughes Communications, Inc.

  - DV program streams (IEC 61883-2)
  - Asynchronous streams
  - Support for external processor DMA
- Programmable data-/space-available indications for flow control; *almost full* and *almost empty* indicators
- Supports bus manager functions and automatic 1394 self-ID verification
- Interrupt driven to minimize host polling
- Single 3.3-V supply
- Separate async acknowledge buffer decreases the ack-tracking burden on host
- JTAG interface to support post-assembly scan of device I/O
- Bus holder isolation
- Embedded support for DTCP content protection:
  - Two M6 baseline ciphers (one per HSDI port)
  - Random number generator in hardware
  - SHA-1 secure hash algorithm in hardware
  - Authentication key cipher in hardware
- Optional auto-configuration for MPEG2/DV transmit and receive functions
- PID filtering and packet insertion for MPEG2 transport stream

2.3 Application Information

Figure 2−1 through Figure 2−4 show several applications where the ceLynx fulfills various functional requirements for consumer electronic devices.

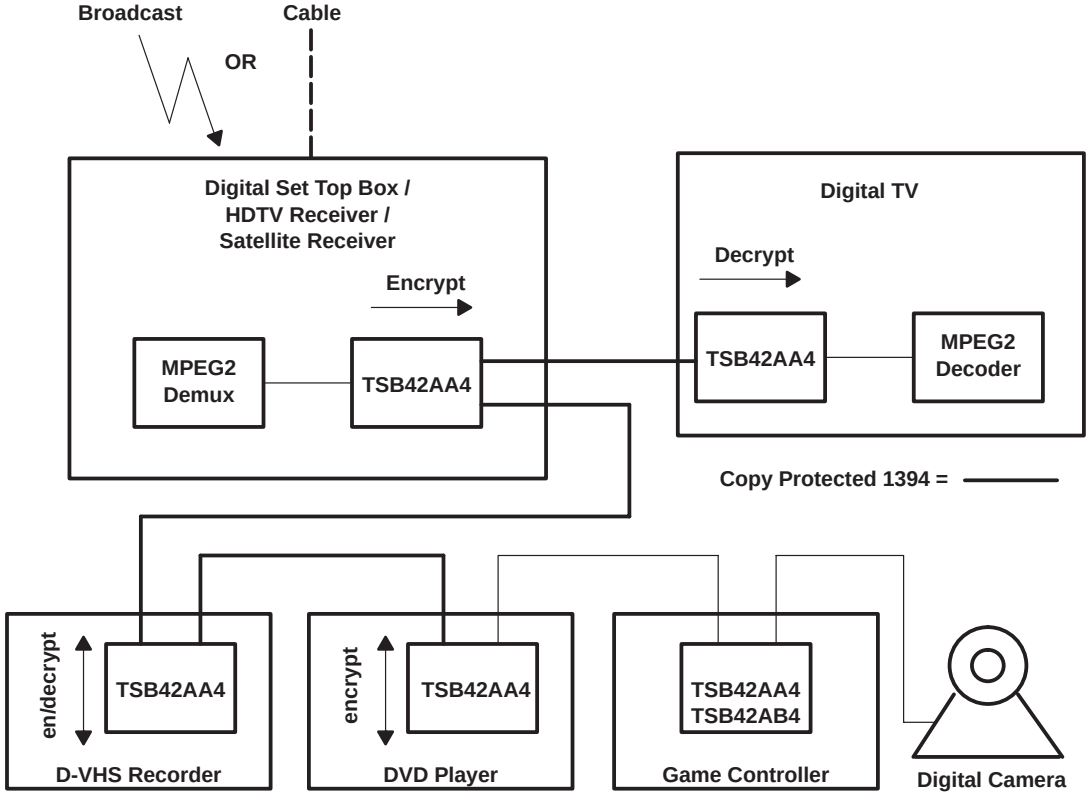


Figure 2−1. Home Entertainment System Interconnect With Content Protection

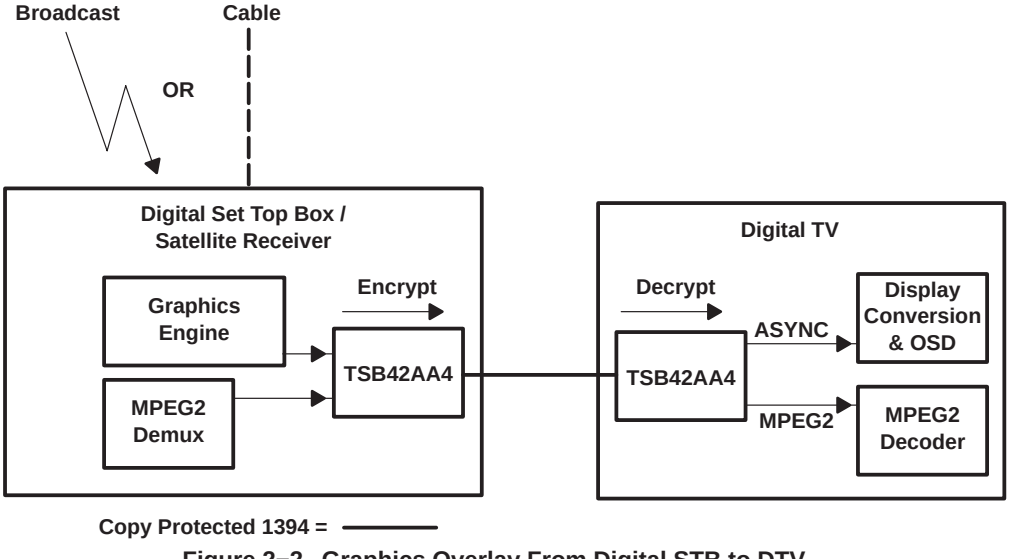


Figure 2−2. Graphics Overlay From Digital STB to DTV

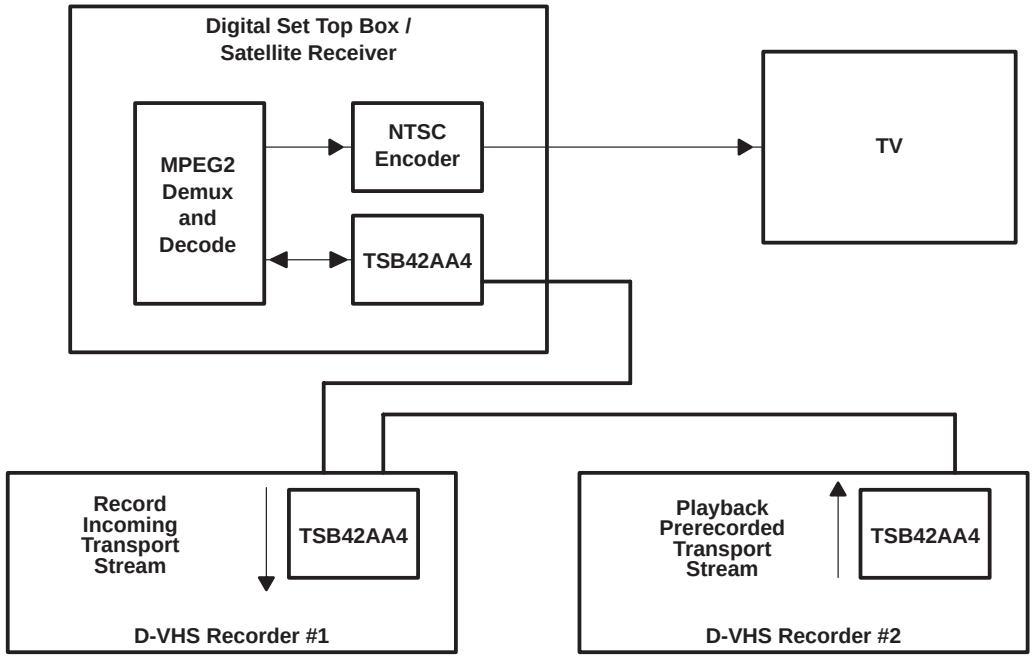
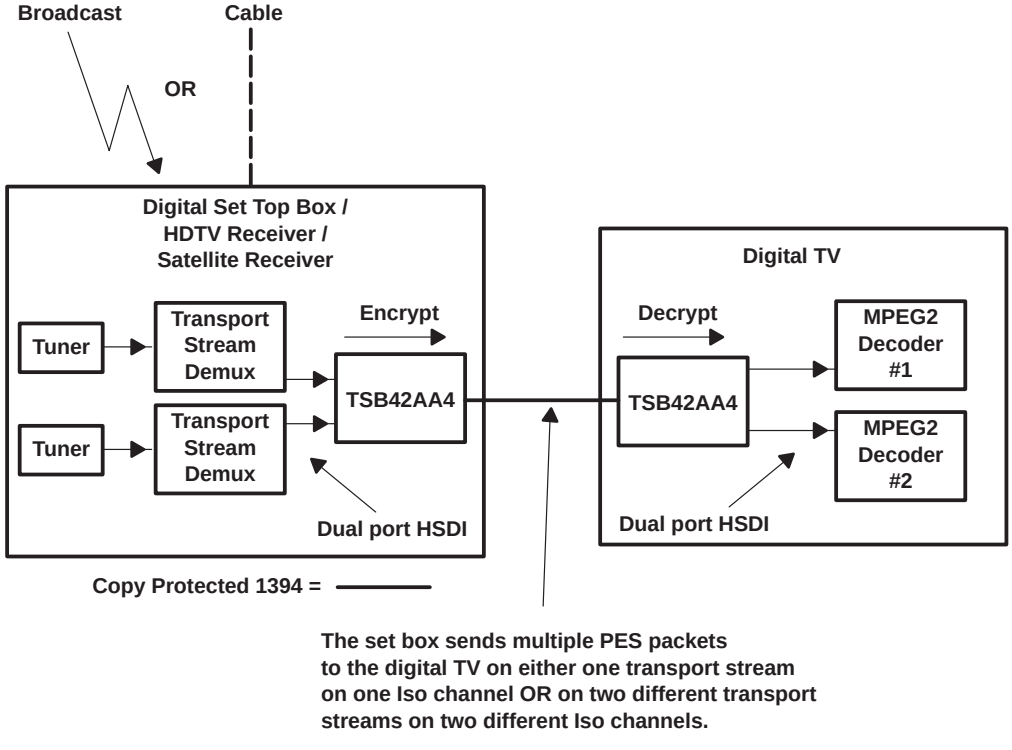


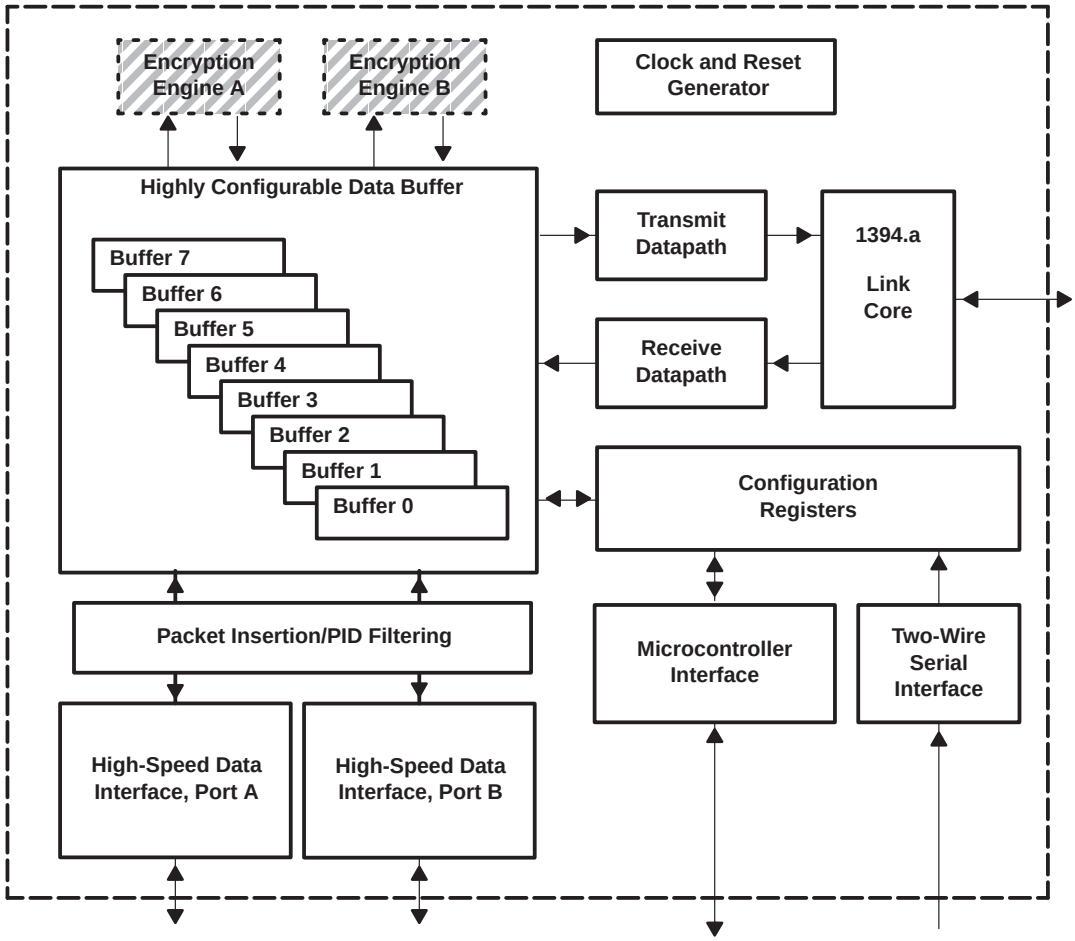
Figure 2−3. Simultaneous Playback and Record of Video (Full Duplex)



The set box sends multiple PES packets to the digital TV on either one transport stream on one Iso channel OR on two different transport streams on two different Iso channels.

Figure 2−4. Picture in Picture Capability Inside Digital TV

2.4 ceLynx Functional Block Diagram

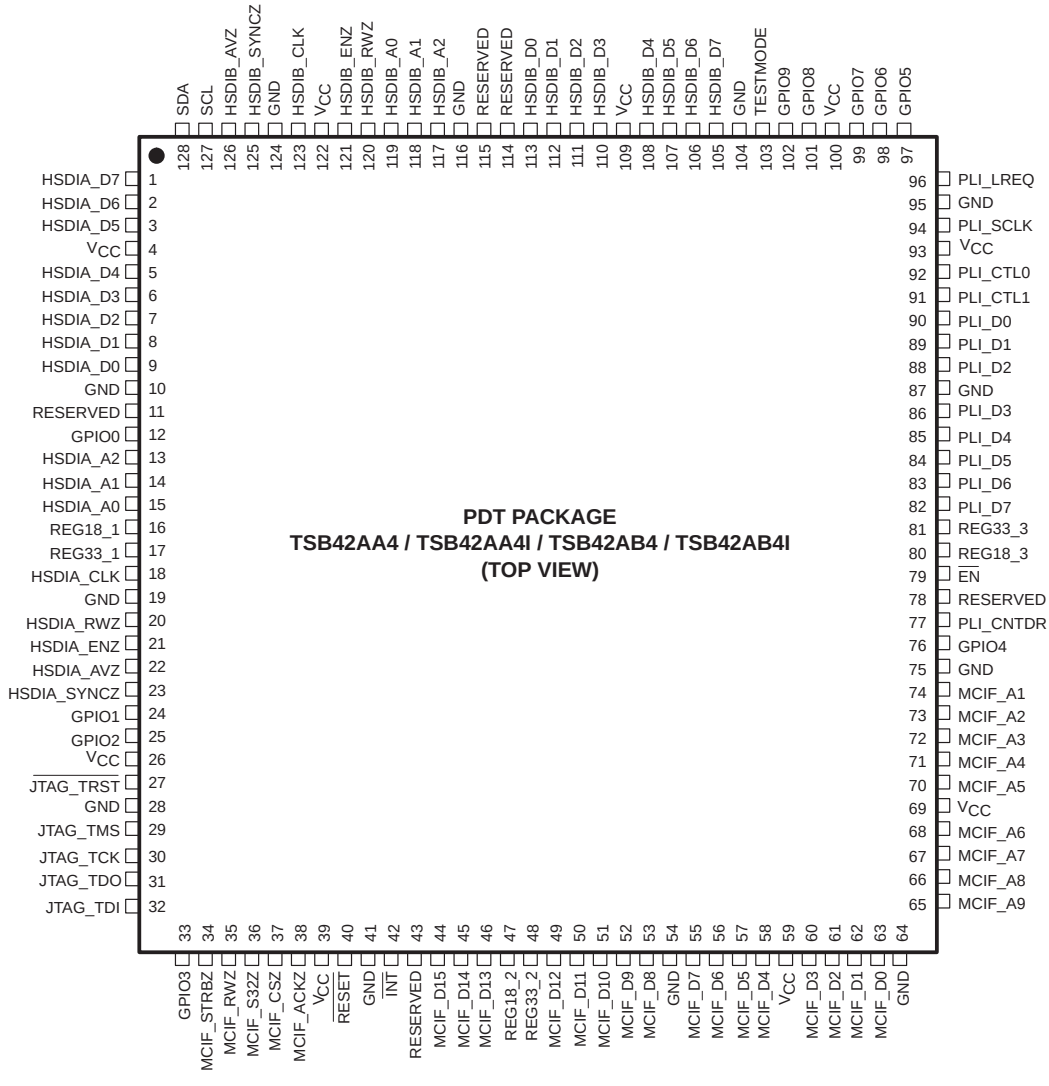


† Shaded region (encryption engines A and B) are only implemented in TSB42AA4.

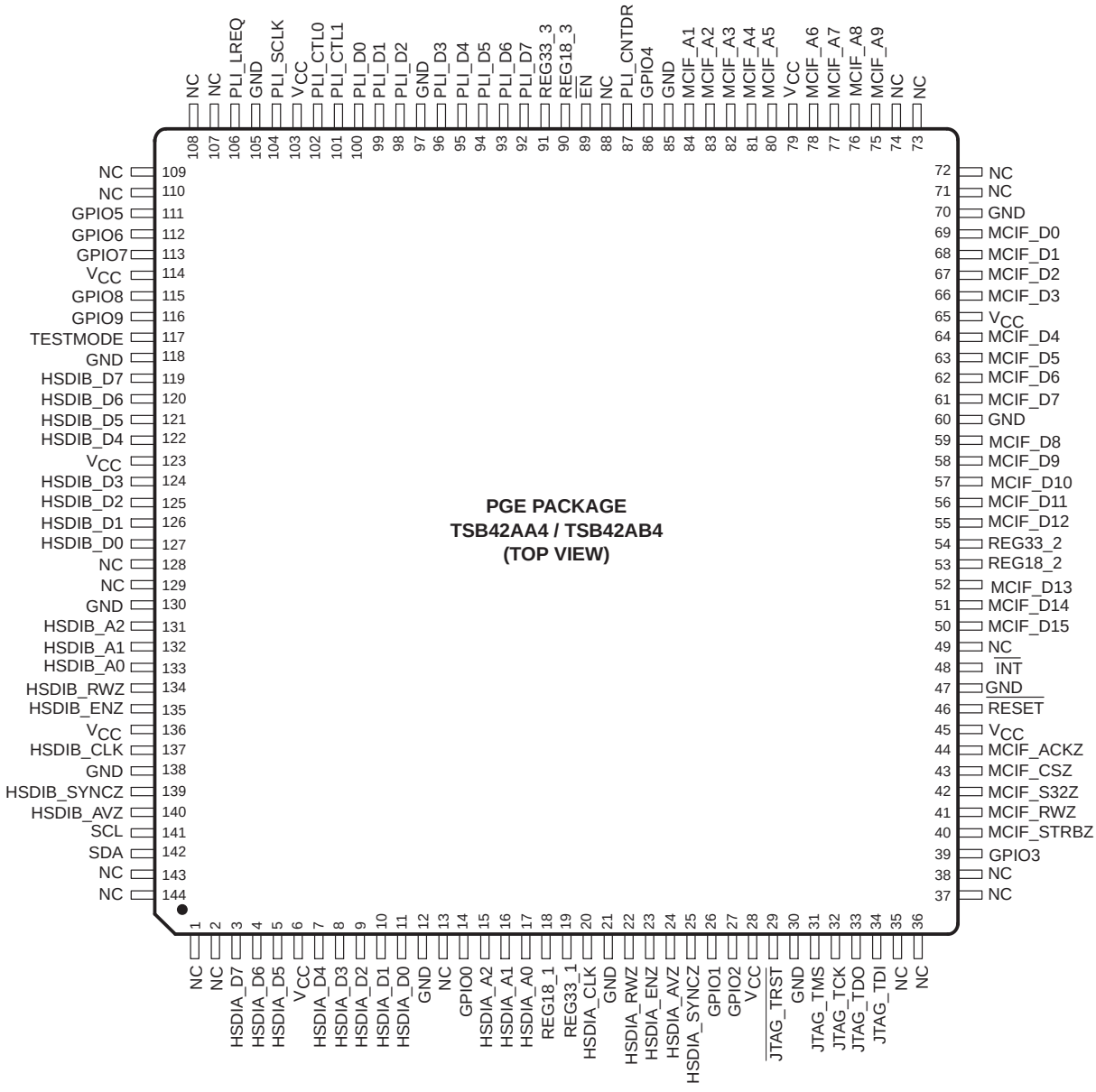
Figure 2–5. ceLynx Functional Block Diagram

2.5 Pin Assignments

PDT Package



PGE Package


PGE PACKAGE
TSB42AA4 / TSB42AB4
(TOP VIEW)
1 NC
2 NC
3 HSDIA_D7
4 HSDIA_D6
5 HSDIA_D5
6 VCC
7 HSDIA_D4
8 HSDIA_D3
9 HSDIA_D2
10 HSDIA_D1
11 HSDIA_D0
12 GND
13 NC
14 GPIO0
15 HSDIA_A2
16 HSDIA_A1
17 HSDIA_A0
18 REG18_1
19 REG33_1
20 HSDIA_CLK
21 GND
22 HSDIA_RWZ
23 HSDIA_ENZ
24 HSDIA_AVZ
25 HSDIA_SYNCZ
26 GPIO1
27 GPIO2
28 VCC
29 JTAG_TRST
30 GND
31 JTAG_TMS
32 JTAG_TCK
33 JTAG_TDO
34 JTAG_TDI
35 NC
36 NC
37 NC
38 NC
39 GPIO3
40 MCIF_STRBZ
41 MCIF_RWZ
42 MCIF_S32Z
43 MCIF_CSZ
44 MCIF_ACKZ
45 VCC
46 RESET
47 GND
48 INT
49 NC
50 MCIF_D15
51 MCIF_D14
52 MCIF_D13
53 REG18_2
54 REG33_2
55 MCIF_D12
56 MCIF_D11
57 MCIF_D10
58 MCIF_D9
59 MCIF_D8
60 GND
61 MCIF_D7
62 MCIF_D6
63 MCIF_D5
64 MCIF_D4
65 VCC
66 MCIF_D3
67 MCIF_D2
68 MCIF_D1
69 MCIF_D0
70 GND
71 NC
72 NC
73 NC
74 NC
75 MCIF_A9
76 MCIF_A8
77 MCIF_A7
78 MCIF_A6
79 VCC
80 MCIF_A5
81 MCIF_A4
82 MCIF_A3
83 MCIF_A2
84 MCIF_A1
85 GND
86 GPIO4
87 PLI_CNTDR
88 NC
89 EN
90 REG18_3
91 REG33_3
92 PLI_D7
93 PLI_D6
94 PLI_D5
95 PLI_D4
96 PLI_D3
97 GND
98 PLI_D2
99 PLI_D1
100 PLI_D0
101 PLI_CTL1
102 PLI_CTL0
103 VCC
104 PLI_SCLK
105 GND
106 PLI_LREQ
107 NC
108 NC
109 NC
110 NC
111 GPIO5
112 GPIO6
113 GPIO7
114 VCC
115 GPIO8
116 GPIO9
117 TESTMODE
118 GND
119 HSDIB_D7
120 HSDIB_D6
121 HSDIB_D5
122 HSDIB_D4
123 VCC
124 HSDIB_D3
125 HSDIB_D2
126 HSDIB_D1
127 HSDIB_D0
128 NC
129 NC
130 GND
131 HSDIB_A2
132 HSDIB_A1
133 HSDIB_A0
134 HSDIB_RWZ
135 HSDIB_ENZ
136 VCC
137 HSDIB_CLK
138 GND
139 HSDIB_SYNCZ
140 HSDIB_AVZ
141 SCL
142 SDA
143 NC
144 NC

2.5.1 Pin Descriptions

2.5.1.1 Power

NAME	PDT PIN NO.	PGE PIN NO.	I/O	DESCRIPTION
GND	10, 19, 28, 41, 54, 64, 75, 87, 95, 104, 116, 124	12, 21, 30, 47, 60, 70, 85, 97, 105, 118, 130, 138		Device ground terminals
V_{CC}	4, 26, 39, 59, 69, 93, 100, 109, 122	6, 28, 45, 65, 79, 103, 114, 123, 136		3.3 V power supply terminals
$\overline{\text{RESET}}$	40	46	I	Reset input. This signal is active low.

2.5.1.2 Voltage Regulators

NAME	PDT PIN NO.	PGE PIN NO.	I/O	DESCRIPTION
REG18_1 REG18_2 REG18_3	16 47 80	18 53 90	O	Internal 1.8-V voltage regulator outputs. These pins should be connected to ground through a 0.1 µF decoupling capacitor. They provide decoupling for the internal voltage regulator.
REG33_1 REG33_2 REG33_3	17 48 81	19 54 91	I	Internal voltage regulator inputs. The regulator provides the 1.8 V needed for the ceLynx internal logic. These pins should be connected to 3.3 V (V_{CC}.)
$\overline{\text{EN}}$	79	89	I	Internal power supply enable. Active low. This pin must be tied low to enable the ceLynx internal 1.8-V power supply.

2.5.1.3 High-Speed Data Interface

NAME	PDT PIN NO.	PGE PIN NO.	I/O	DESCRIPTION
HSDIA_D[7:0]	1, 2, 3, 5, 6, 7, 8, 9	3, 4, 5, 7, 8, 9, 10, 11	I/O	HSDI port A data bus. Bidirectional HSDIA_D7 is the MSB and HSDIA_D0 is the LSB.
HSDIB_D[7:0]	105, 106, 107, 108, 110, 111, 112, 113	119, 120, 121, 122, 124, 125, 126, 127	I/O	HSDI port B data bus. Bidirectional HSDIB_D7 is the MSB and HSDIB_D0 is the LSB.
HSDIA_A[2:0]	13, 14, 15	15, 16, 17	I	HSDI port A address bus. HSDIA_A2 is the MSB and HSDIA_A0 is the LSB. Selects the internal buffer used to store data prior to 1394 transmission or after 1394 reception. This bus is unused when HSDI port A is configured in single-stream mode.
HSDIB_A[2:0]	117, 118, 119	131, 132, 133	I	HSDI port B address bus. HSDIB_A2 is the MSB and HSDIB_A0 is the LSB. Selects the internal buffer used to store data prior to 1394 transmission or after 1394 reception. This bus is unused when HSDI port B is configured in single-stream mode.
HSDIA_CLK	18	20	I	HSDI port A clock. (Data is clocked on the rising clock edge.) Max throughput in byte mode is 27 Mbytes/sec.

2.5.1.3 High-Speed Data Interface (continued)

NAME	PDT PIN NO.	PGE PIN NO.	I/O	DESCRIPTION
HSDIB_CLK	123	137	I	HSDI port B clock. (Data is clocked on the rising clock edge.) Max throughput in byte mode is 27 Mbytes/sec.
HSDIB_SYNCZ	125	139	I/O	HSDI port B synchronization signal. Used to determine data packet boundaries. In 1394 transmit mode, the external host device drives the signal, marking the beginning or end of a data block. In 1394 receive mode, the ceLynx drives the pin, signaling the beginning or end of a data block. The exact operation of the HSDIB_SYNCZ depends on the synchronization mode. HSDIB_SYNCZ polarity is programmable and defaults to *active high.* In default HSDIB configuration, this signal is not used.
HSDIA_SYNCZ	23	25	I/O	HSDI port A synchronization signal. Used to determine data packet boundaries. In 1394 transmit mode, the external host device drives the signal, marking the beginning or end of a data block. In 1394 receive mode, the ceLynx drives the pin, signaling the beginning or end of a data block. The exact operation of the HSDIA_SYNCZ depends on the synchronization mode. HSDIA_SYNCZ polarity is programmable and defaults to *active high.* In default HSDIA configuration, this signal is not used.
HSDIA_RWZ	20	22	I	HSDI port A read/write signal. Used to indicate either a host read or a host write transaction to the HSDIA port. HSDIA_R/WZ polarity is programmable and defaults to *active high* for read operations and *active low* for write operations.
HSDIB_RWZ	120	134	I	HSDI port B read/write signal. Used to indicate either a host read or a host write transaction to the HSDIB port. HSDIB_R/WZ polarity is programmable and defaults to *active high* for read operations and *active low* for write operations.
HSDIA_AVZ	22	24	O	HSDI port A data available. Used during 1394 receive operations. Indicates when a packet of data is available in the selected receive buffer (as indicated by HSDIA_A[2:0]). HSDIA_AVZ polarity is programmable and defaults to *active high*.
HSDIB_AVZ	126	140	O	HSDI port B data available. Used during 1394 receive operations. Indicates when a packet of data is available in the selected receive buffer (as indicated by HSDIB_A[2:0]). HSDIB_AVZ polarity is programmable and defaults to *active high*.

2.5.1.3 High-Speed Data Interface (continued)

NAME	PDT PIN NO.	PGE PIN NO.	I/O	DESCRIPTION
HSDIA_ENZ	21	23	I	HSDIA port access enable. Used to indicate valid data for 1394 transmit (host write) or 1394 receive (host read) operations. Asserting HSDIA_ENZ during host writes latches the data on the next HSDIA_CLK rising edge. Asserting HSDIA_ENZ during host reads, presents received 1394 data from internal buffers on the next HSDIA_CLK rising edge. HSDIA_ENZ polarity is programmable and defaults to *active high*.
HSDIB_ENZ	121	135	I	HSDIB port access enable. Used to indicate valid data for 1394 transmit (host write) operations or 1394 receive (host read) operations. Asserting HSDIB_ENZ during host writes latches the data on the next HSDIB_CLK rising edge. Asserting HSDIB_ENZ during host reads presents received 1394 data from internal buffers on the next HSDIB_CLK rising edge. HSDIB_ENZ polarity is programmable and defaults to *active high*.

2.5.1.4 Microcontroller Interface (MCIF)†

NAME	PDT PIN NO.	PGE PIN NO.	I/O	DESCRIPTION
$\overline{\text{INT}}$	42	48	O	Interrupt. This is the ceLynx interrupt output to the host. This signal is active-low. When this pin is not used, add a weak pull-up (1 kΩ to 10 kΩ).
MCIF_A[9:1]	65, 66, 67, 68, 70, 71, 72, 73, 74	75, 76, 77, 78, 80, 81, 82, 83, 84	I	Microcontroller interface address bus. MCIF_A9 is the MSB and MCIF_A1 is the LSB. Users should connect their LSB+1 address pin to MCIF_A1 (byte access is not allowed).
MCIF_ACKZ	38	44	O	Acknowledge signal. Indicates to the host controller the completion of the current read or write access. When MCIF_ACKZ asserts (low) during host writes, data has been successfully written to the specified address. When MCIF_ACKZ asserts (low) during host reads, this indicates that data is valid and may be read by the host. The MCIF_ACKZ polarity is programmable and defaults to *active low*. When this pin is not used, add a weak pull-up (1 kΩ to 10 kΩ).
MCIF_CSZ	37	43	I	ceLynx chip select. Enables the ceLynx to perform read or write transactions on the microcontroller interface. The MCIF_CSZ polarity is programmable and defaults to *active low*.
MCIF_D[15:0]	44, 45, 46, 49, 50, 51, 52, 53, 55, 56, 57, 58, 60, 61, 62, 63	50, 51, 52, 55, 56, 57, 58, 59, 61, 62, 63, 64, 66, 67, 68, 69	I/O	Microcontroller interface bidirectional data bus. MCIF_D15 is the MSB on this bus, and MCIF_D0 is the LSB.
MCIF_RWZ	35	41	I	Read/write indicator. Indicates whether the current pending access is a read or a write. MCIF_RWZ polarity is programmable and defaults to *active high* during read operations and *active low* during write operations.

† The microcontroller port does not support time stamping or encryption.

2.5.1.4 Microcontroller Interface† (continued)

NAME	PDT PIN NO.	PGE PIN NO.	I/O	DESCRIPTION
MCIF_S32Z	36	42	I	Data transfer size indicator. Indicates whether the host controller desires 16-bit or 32-bit transactions. When set to 32-bit transactions, the port address auto-increments on the second consecutive access. The MCIF_S32Z polarity is programmable to *active high* or *active low* and defaults to *active low*. Active signal indicates 32-bit access.
MCIF_STRBZ	34	40	I	Data strobe signal. During host write operations, this signal indicates that the data on MCIF_D[15:0] is valid and the ceLynx latches the data. During host read operations, this signal indicates to the ceLynx that the host is ready for data. The MCIF_STRBZ polarity is programmable to *active high* or *active low* and defaults to *active low*.

† The microcontroller port does not support time stamping or encryption.

2.5.1.5 JTAG

NAME	PDT PIN NO.	PGE PIN NO.	I/O	DESCRIPTION
$\overline{\text{JTAG\_TRST}}$	27	29	I	JTAG test reset. This signal has an internal pull-up. During normal device operation, there is no need for an external pull-up or pull-down.
JTAG_TMS	29	31	I	JTAG test mode select. This signal has an internal pull-up. During normal device operation, there is no need for an external pull-up or pull-down.
JTAG_TCK	30	32	I	JTAG clock. This signal has an internal pull-up. During normal device operation, there is no need for an external pull-up or pull-down.
JTAG_TDO	31	33	O	JTAG data output. During normal device operation, this signal is left unconnected.
JTAG_TDI	32	34	I	JTAG data in. This signal has an internal pull-up. During normal device operation, there is no need for an external pull-up or pull-down.

NOTES: 1. JTAG boundary scan EXTEST and SAMPLE/PRELOAD functions do not work. An error in the design prevents the test system from controlling the direction of the I/O signals.
2. The JTAG boundary scan BYPASS mode is functional. Customers can use JTAG with ceLynx where all I/Os are bypassed.

2.5.1.6 Two-Wire Serial Interface

NAME	PDT PIN NO.	PGE PIN NO.	I/O	DESCRIPTION
SCL	127	141	O	Serial interface clock. Open collector. SCL is sampled at power up to determine if an EEPROM is present. Connect to ground if no ceLynx serial EEPROM configuration device is used. Maximum operating frequency is 100 kHz.
SDA	128	142	I	Serial interface data input signal. Open collector input that typically interfaces to a serial EEPROM containing CFR data. Used during ceLynx power up and reset to auto configure CFRs.

2.5.1.7 PHY-Link Interface

NAME	PDT PIN NO.	PGE PIN NO.	I/O	DESCRIPTION
PLI_D[0:7]	90, 89, 88, 86, 85, 84, 83, 82	100, 99, 98, 96, 95, 94, 93, 92	I/O	PHY-link data bus. PLI_D[0] is the MSB and PLI_D[7] is the LSB.
PLI_SCLK	94	104	I	Physical layer system clock. Supplied by the physical layer device and is 49.152 MHz. PLI_SCLK is required for link layer operation.
PLI_CNTDR	77	87	I/O	Contender signal. When PLI_CNTDR is configured as an output in the SYSCFR.PINCFG register, the pin sets the IRM contender function in the PHY. When configured as an input, the pin reports the PHY contender status to the LCTRL (link control) register.
PLI_CTL[0:1]	92, 91	102, 101	I/O	PHY-link interface control signals. These bidirectional control signals control the passage of information between the link and PHY. PLI_CTL0 is the MSB and PLI_CTL1 is the LSB.
PLI_LPS	NC	NC		PLI_LPS is not implemented in the current design.
PLI_LREQ	96	106	O	Link request. Requests the physical layer controller to perform some service.

2.5.1.8 Optional Signals

NAME	PDT PIN NO.	PGE PIN NO.	I/O	DESCRIPTION
GPIO0	12	14	I/O	General-purpose I/Os. GPIO functions are programmed via CFRs (reg 0x008 GPIOSEL). GPIOs are configured as ceLynx inputs after reset or power up.
GPIO1	24	26	I/O	
GPIO2	25	27	I/O	
GPIO3	33	39	I/O	
GPIO4	76	86	I/O	
GPIO5	97	111	I/O	
GPIO6	98	112	I/O	
GPIO7	99	113	I/O	
GPIO8	101	115	I/O	
GPIO9	102	116	I/O	
NC	11, 43, 78, 114, 115	13, 49, 88, 128, 129		Reserved for future use. Leave unconnected.
NC	—	1, 2, 35, 36, 37, 38, 71, 72, 73, 74, 107, 108, 109, 110, 143, 144		Reserved for future use. Leave unconnected.
TESTMODE	103	117	I	Factory test pin. Connect to GND for normal device operation.

Table 2−1. Pin Name/Buffer Name Cross Reference, Sorted by Pin Number

PDT PIN #	PGE PIN #	PIN NAME	I/O	PDT PIN #	PGE PIN #	PIN NAME	I/O	PDT PIN #	PGE PIN #	PIN NAME	I/O
—	1	NC		19	21	GND		35	41	MCIF_RWZ†	I
—	2	NC		20	22	HSDIA_RWZ†	I	36	42	MCIF_S32Z†	I
1	3	HSDIA_D7	I/O	21	23	HSDIA_ENZ†	I	37	43	MCIF_CSZ†	I
2	4	HSDIA_D6	I/O	22	24	HSDIA_AVZ†	O	38	44	MCIF_ACKZ†	O
3	5	HSDIA_D5	I/O	23	25	HSDIA_SYNCZ†	I/O	39	45	V_{CC}	
4	6	V_{CC}		24	26	GPIO1	I/O	40	46	$\overline{RESET}$‡	I
5	7	HSDIA_D4	I/O	25	27	GPIO2	I/O	41	47	GND	
6	8	HSDIA_D3	I/O	26	28	V_{CC}		42	48	$\overline{INT}$ ‡	O
7	9	HSDIA_D2	I/O	27	29	$\overline{JTAG\_TRST}$	I	43	49	NC	
8	10	HSDIA_D1	I/O	28	30	GND		44	50	MCIF_D15	I/O
9	11	HSDIA_D0	I/O	29	31	JTAG_TMS	I	45	51	MCIF_D14	I/O
10	12	GND		30	32	JTAG_TCK	I	46	52	MCIF_D13	I/O
11	13	NC		31	33	JTAG_TDO	O	47	53	REG18_2	O
12	14	GPIO0	I/O	32	34	JTAG_TDI	I	48	54	REG33_2	I
13	15	HSDIA_A2	I	—	35	NC		49	55	MCIF_D12	I/O
14	16	HSDIA_A1	I	—	36	NC		50	56	MCIF_D11	I/O
15	17	HSDIA_A0	I	—	37	NC		51	57	MCIF_D10	I/O
16	18	REG18_1	O	—	38	NC		52	58	MCIF_D9	I/O
17	19	REG33_1	I	33	39	GPIO3	I/O	53	59	MCIF_D8	I/O
18	20	HSDIA_CLK	I	34	40	MCIF_STRBZ†	I	54	60	GND	
56	62	MCIF_D6	I/O	80	90	REG18_3	O	104	118	GND	
57	63	MCIF_D5	I/O	81	91	REG33_3	I	105	119	HSDIB_D7	I/O
58	64	MCIF_D4	I/O	82	92	PLI_D7	I/O	106	120	HSDIB_D6	I/O
59	65	V_{CC}		83	93	PLI_D6	I/O	107	121	HSDIB_D5	I/O
60	66	MCIF_D3	I/O	84	94	PLI_D5	I/O	108	122	HSDIB_D4	I/O
61	67	MCIF_D2	I/O	85	95	PLI_D4	I/O	109	123	V_{CC}	
62	68	MCIF_D1	I/O	86	96	PLI_D3	I/O	110	124	HSDIB_D3	I/O
63	69	MCIF_D0	I/O	87	97	GND		111	125	HSDIB_D2	I/O
64	70	GND		88	98	PLI_D2	I/O	112	126	HSDIB_D1	I/O
—	71	NC		89	99	PLI_D1	I/O	113	127	HSDIB_D0	I/O
—	72	NC		90	100	PLI_D0	I/O	114	128	NC	
—	73	NC		91	101	PLI_CTL1	I/O	115	129	NC	
—	74	NC		92	102	PLI_CTL0	I/O	116	130	GND	

† Denotes pin with programmable polarity.
‡ Denotes active low pin.

Table 2−1. Pin Name/Buffer Name Cross Reference, Sorted by Pin Number (Continued)

PDT PIN #	PGE PIN #	PIN NAME	I/O	PDT PIN #	PGE PIN #	PIN NAME	I/O	PDT PIN #	PGE PIN #	PIN NAME	I/O
55	61	MCIF_D7	I/O	79	89	$\overline{EN}$‡	I	103	117	TESTMODE	I
65	75	MCIF_A9	I	93	103	V_{CC}		117	131	HSDIB_A2	I
66	76	MCIF_A8	I	94	104	PLI_SCLK	I	118	132	HSDIB_A1	I
67	77	MCIF_A7	I	95	105	GND		119	133	HSDIB_A0	I
68	78	MCIF_A6	I	96	106	PLI_LREQ	O	120	134	HSDIB_RWZ†	I
69	79	V_{CC}		—	107	NC		121	135	HSDIB_ENZ†	I
70	80	MCIF_A5	I	—	108	NC		122	136	V_{CC}	
71	81	MCIF_A4	I	—	109	NC		123	137	HSDIB_CLK	I
72	82	MCIF_A3	I	—	110	NC		124	138	GND	
73	83	MCIF_A2	I	97	111	GPIO5	I/O	125	139	HSDIB_SYNCZ†	I/O
74	84	MCIF_A1	I	98	112	GPIO6	I/O	126	140	HSDIB_AVZ†	O
75	85	GND		99	113	GPIO7	I/O	127	141	SCL	I/O
76	86	GPIO4	I/O	100	114	V_{CC}		128	142	SDA	I/O
77	87	PLI_CNTDR	I/O	101	115	GPIO8	I/O	—	143	NC	
78	88	NC		102	116	GPIO9	I/O	—	144	NC	

† Denotes pin with programmable polarity.
‡ Denotes active low pin.

3 External Interfaces

The ceLynx has four external interfaces; the high-speed data interface (HSDI), the microcontroller interface (MCIF), the physical-layer interface, and a two-wire serial interface for an external EEPROM. The HSDI and MCIF each support multiple modes designed for maximum flexibility and ease of use. The physical layer interface conforms to the IEEE 1394-1995 and 1394.a standards and allows the ceLynx to operate seamlessly with industry standard 100-, 200-, and 400-Mbps physical-layer devices. This includes the Texas Instruments family of 400 Mbps PHYS (TSB41LV0X). The two-wire serial interface gives a connection to EEPROM for easy loading of CFR and CSR information

This section includes the interface, functional operation, and detailed timing information for all modes of each interface.

3.1 Microcontroller Interface (MCIF)

The ceLynx has a host controller interface that is designed to interface seamlessly with 68000/68020 style processors. This interface is completely asynchronous. The interface consists of 16 data lines, 9 address lines, and various control signals. All signals are resynchronized internally to a 50-MHz clock derived from the SCLK input from the physical layer device. The host controller interface operates seamlessly with various vendors' MPEG2 transport chipsets for ease of use.

Both 32-bit and 16-bit transactions are supported on the microcontroller interface. When using 32-bit accesses the host supplies only one address, then follows with two data phases. The link microcontroller interface automatically increments the address for the second data phase. For 16-bit access, each transaction requires a separate address. Each 16-bit access is independent of any other transaction. The microcontroller interface uses the MCIF_S32 signal to determine if the current access is 32- or 16-bit. The MCIF_S32 signal state should not change in the middle of an access. It can change in between accesses.

The 16-bit transaction capability allows the host more efficient access since it eliminates the need for the host to disable interrupts between upper and lower doublet accesses. Disabling interrupts is required if only full quadlet (32-bit) access is supported for every CFR access.

For a 32-bit read, the upper and lower doublets are time independent. When the first doublet is accessed, a snapshot of the entire 32-bit register is captured. The second doublet access uses the snapshot value.

The snapshot is not used for 16-bit register access. Each 16-bit access results in the most up-to-date doublet value.

Note that nonquadlet aligned addressing is not supported. The host controller can only access the upper half or lower half of any 32-bit CFR. For example, the version ID CFR is located at addresses 0x000 and 0x002. The host is not allowed to perform a 32-bit access starting at address 003h. This would, in effect, be an attempt to write to addresses 003h and 004h. The 004h is located within a separate CFR. However, using 16-bit transactions, the user can access either upper or lower half of all 32-bit CFRs independently.

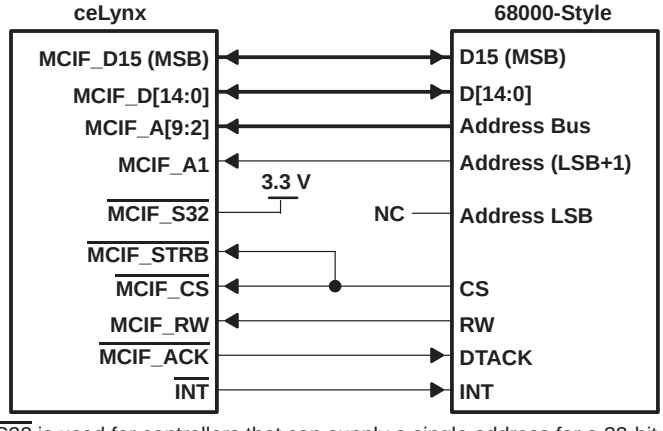
NOTE:

- The host interface does not support time stamping or encryption.
- For reads of time-sensitive registers (such as CYCLE TIMER), use 32-bit reads if high accuracy is required. For a 32-bit read, the register value is copied and is used for both the upper and lower 16-bit reads.
  During a 16-bit read operation, the current doublet being addressed returns the current data value. This may present problems for time-sensitive registers, such as the CYCLE TIMER. The first 16-bit read returns the upper 16 bits. The second 16-bit read returns the lower 16 bits, but the amount of time between the first and second reads results in a difference between the upper and lower cycle timer values.
- When ceLynx is programmed to use 32-bit host access, only big endian mode is supported for all data access through the host.
- Status of the MCIF_STRB pin. MCIF_ACK function depends on MCIF_STRB

timing. If the host asserts this signal, the ceLynx asserts the MCIF_ACK pin when either the data on MCIF_D[15:0] is valid (during a read access) or the data on MCIF_D[15:0] has been latched (during a write access). As soon as the host deasserts this signal, the ceLynx deasserts the MCIF_ACK.

- Status of the MCIF_CS pin. When this signal is asserted, the MCIF_ACK assumes that ceLynx is the only peripheral device currently selected on the MCIF interface, and as such, it drives the MCIF_ACK pin either asserted or deasserted.
- Setting of the PINCFG.MCACKZFLT bit at 0x004. When this register bit is set to 0, the MCIF_ACK signal is always in the high-impedance state and the ceLynx never asserts the MCIF_ACK pin. The ceLynx never asserts the MCIF_ACK pin. The user must never set this bit to 0, because this prevents communication with the host. If this register bit is set to 1 (default), then the MCIF_ACK pin output drivers are turned off when the pin is deasserted (assuming the MCIF_CS pin is deasserted).
- Setting of MCIFCFG.MCACKZDLY bits at 0x010. These bits work in conjunction with the MCACKZFLT mode to control the time that the MCIF_ACK pin is deasserted before the pin output drivers, described previously, are turned off. This delay can be adjusted from 0 ns (default) up to 10 ns. If the MCACKZFLT register bit is set to 0, the MCACKZDLY register bits are ignored.

Figure 3−1 shows the typical connection between ceLynx and a 68000-style processor.



NOTES: 1. MCIF_S32 is used for controllers that can supply a single address for a 32-bit transaction.
2. MCIF_STRB is provided for controllers that have separate strobe and chip select signals. The MCIF_STRB and MCIF_CS signals can be tied together if the application processor does not have a separate strobe signal.

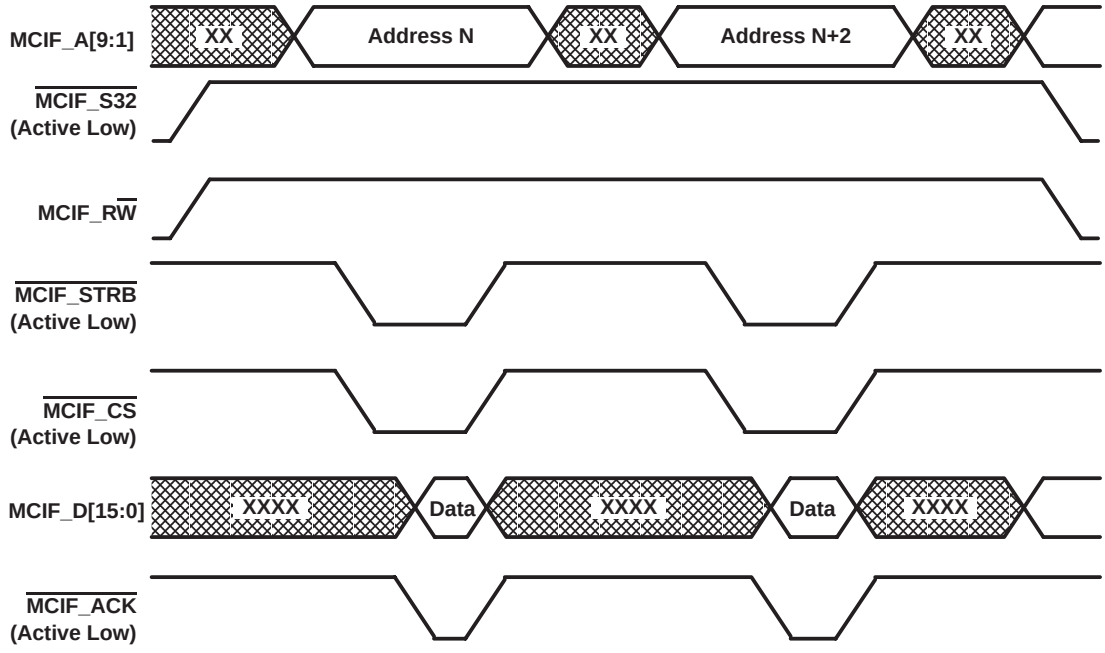
Figure 3−1. Interface Between ceLynx and 68000-Style Processor

3.1.1 Read Operation

Figure 3−2 depicts a typical read operation using 16-bit transactions. The host begins the read access by driving the address to be read from onto MCIF_A[9:1]. The host then drives MCIF_RW high to indicate a read. The host drives MCIF_STRB low to indicate that it is ready to receive the data. MCIF_CS selects the link as the peripheral being accessed. Note the MCIF_STRB signal acts as a master enable on the microcontroller interface. No transactions occur unless MCIF_STRB is active. The address is sampled on the falling edge of MCIF_CS and begins the internal read access to the specified CFR. After the 16-bit word is retrieved from the internal CFR, the link responds by driving the data onto the data bus and driving MCIF_ACK low to indicate that data is available

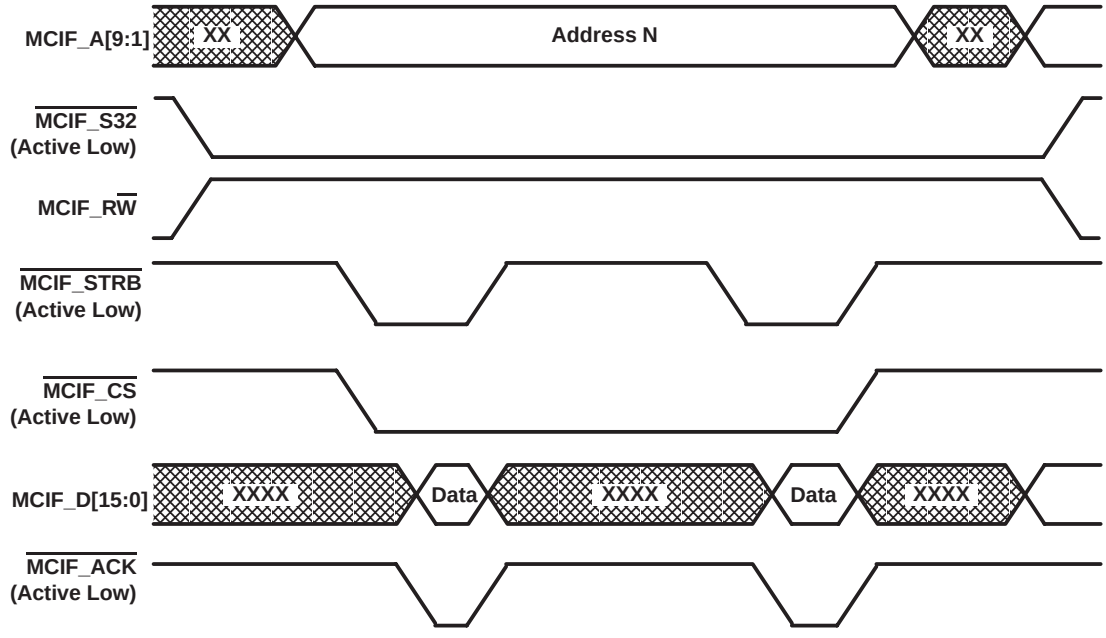
The difference in functionality of a 32-bit read transaction is that the host indicates a 32-bit access by driving MCIF_S32 active low. The host only gives one address for the entire transaction. In this mode, the MCIF

address signals should be driven for the entire 32-bit access. All other events remain the same. See Figure 3−3.



NOTE: MCIF_$\overline{CS}$ can be asserted during both 16-bit transactions. The MCIF_$\overline{STRB}$ acts as the master enable for the MCIF.

Figure 3−2. 16-Bit Read

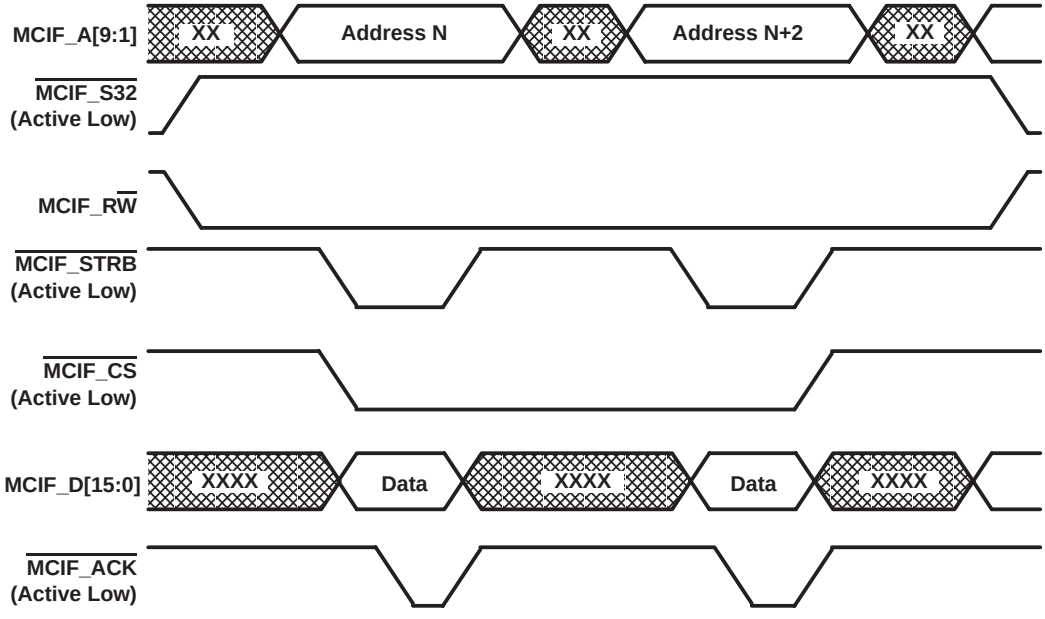


NOTE: MCIF_CS can be deasserted between data phases of 32-bit read. The MCIF_STRB acts as the master enable for the MCIF.

Figure 3−3. 32-Bit Read

3.1.2 Write Operation

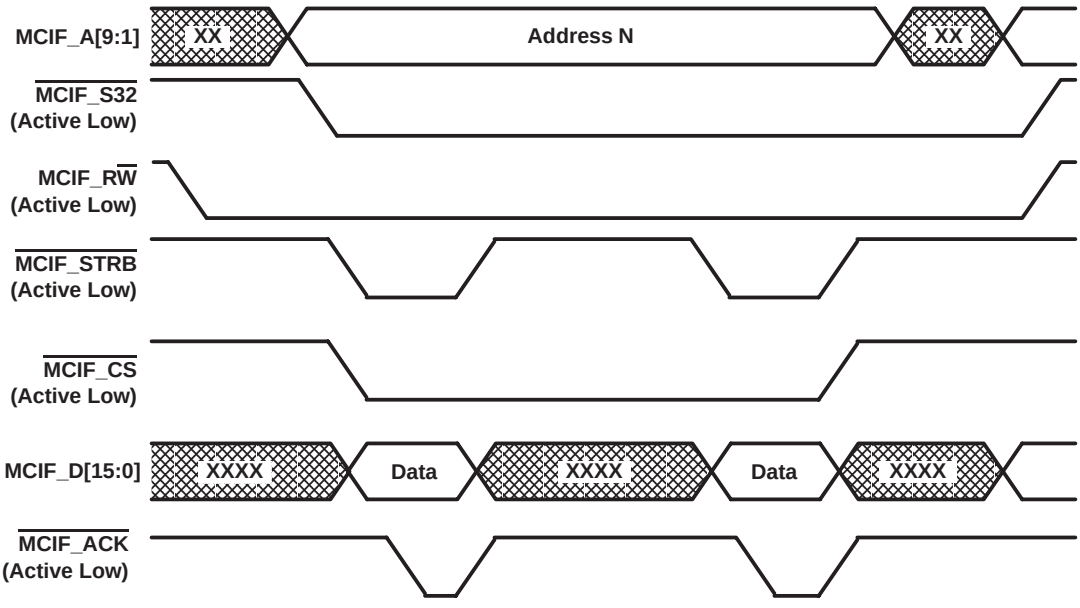
Figure 3−4 depicts a 16-bit write operation. The host begins the write access by driving the address to be written to MCIF_A[9:1]. The host drives MCIF_RW low to indicate a write, and MCIF_CS low to select the link as the peripheral being accessed. The host drives the data out onto MCIF_D[15:0] and MCIF_STRB low to indicate that data present on the data bus is valid. The link responds by driving MCIF_ACK low to indicate that this cycle is complete and data has been successfully written to the selected address.



NOTE: MCIF_CS can be deasserted between the two 16-bit transactions. The MCIF_STRB signal acts as the master enable for MCIF.

Figure 3−4. 16-Bit Write

Figure 3−5 depicts a 32-bit write operation. This works similarly to the 16-bit write. However, the $\overline{\text{MCIF\_S32}}$ signal is low for the entire access. This indicates a 32-bit access to ceLynx. ceLynx automatically increments the address for the second word access. Address N must be driven on the interface for the entire 32-bit access.



NOTE: $\overline{\text{MCIF\_CS}}$ can be deasserted between the data phases of a 32-bit access. The $\overline{\text{MCIF\_STRB}}$ signal acts as the master enable for MCIF.

Figure 3−5. 32-Bit Write

3.1.3 Critical Timing

Figure 3−6 and Figure 3−7 show critical timing for write and read transactions, respectively. The critical timing numbers for 16-bit and 32-bit accesses are identical. The various timing parameters are listed and described in Table 3−1.

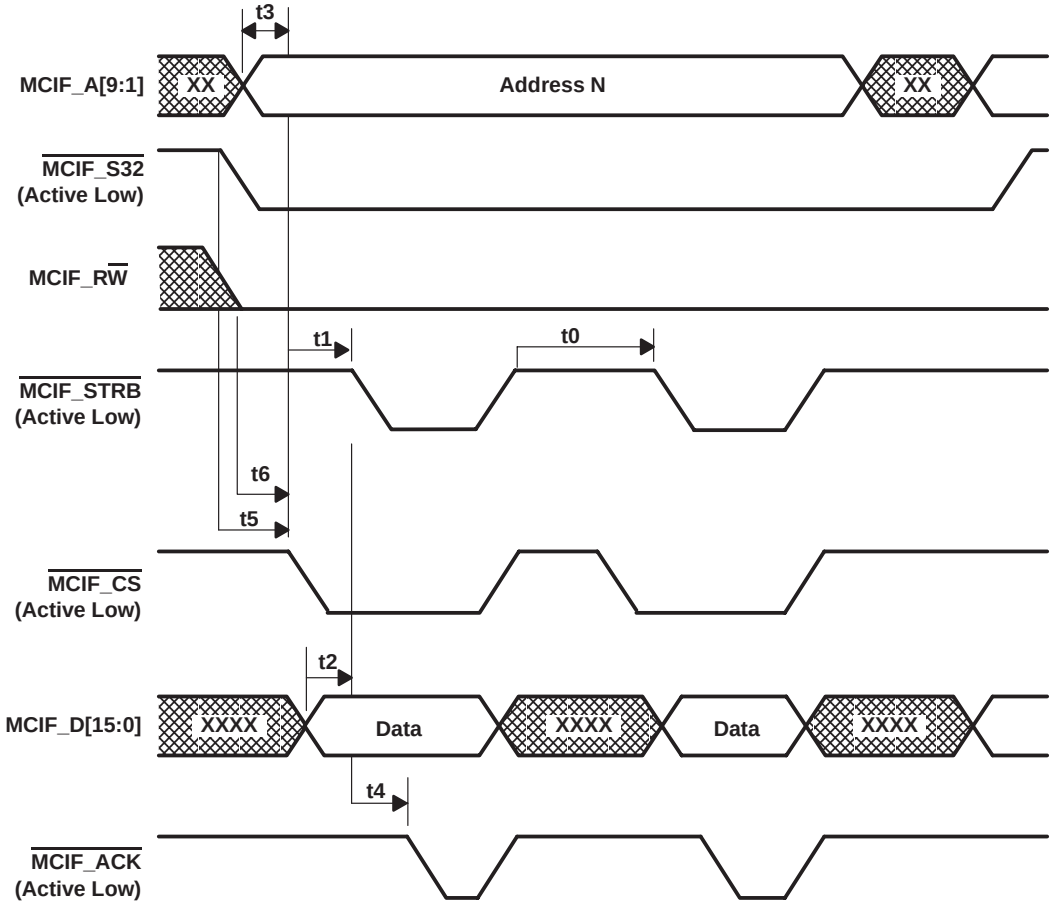


Figure 3−6. Microcontroller Interface Critical Write Timing

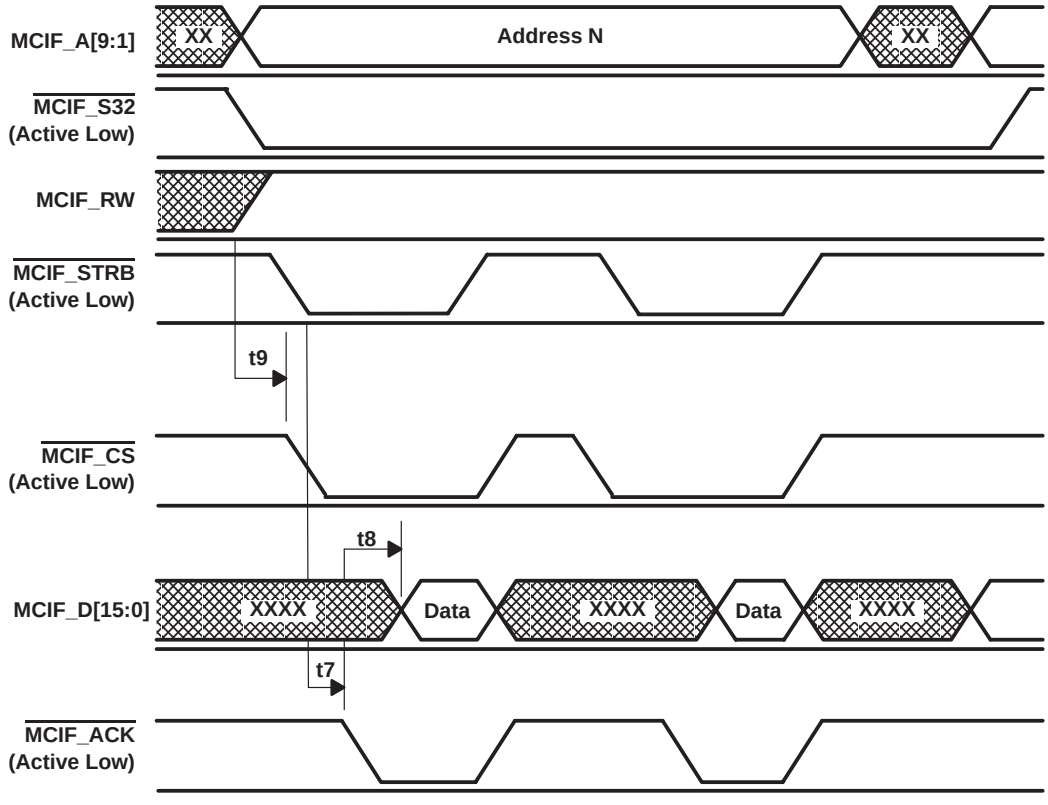


Figure 3−7. Microcontroller Interface Critical Read Timing

Table 3−1. MCIF Critical Timing Parameters

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t0	$\overline{\text{MCIF\_STRB}}$ to $\overline{\text{MCIF\_STRB}}$ (rising edge to falling edge)	9		ns
t1	Setup time, $\overline{\text{MCIF\_CS}}$ to $\overline{\text{MCIF\_STRB}}$	0		ns
t2	Setup time, MCIF_D[15:0] to $\overline{\text{MCIF\_STRB}}$	0		ns
t3	Setup time, address to $\overline{\text{MCIF\_CS}}$	0		ns
t4	Write access time, $\overline{\text{MCIF\_STRB}}$ to $\overline{\text{MCIF\_ACK}}$		114	ns
t5	Setup time, $\overline{\text{MCIF\_S32}}$ to MCIF_CS	0		ns
t6	Setup time, MCIF_$\overline{\text{RW}}$ (write) to $\overline{\text{MCIF\_CS}}$	0		ns
t7	Read access time, $\overline{\text{MCIF\_STRB}}$ to $\overline{\text{MCIF\_ACK}}$		114	ns
t8	Data output delay, $\overline{\text{MCIF\_ACK}}$ to MCIF_D[15:0] out	0		ns
t9	Setup time, MCIF_$\overline{\text{RW}}$ (read) to $\overline{\text{MCIF\_CS}}$	0		ns

NOTES: 3. All signals have 0 ns hold time in relation to MCIF_$\overline{\text{ACK}}$.

3.1.4 Host Interface − Multistrobe Mode

The ceLynx host port consists of separate 8-bit address and 16-bit data busses. In the default setting, reads and writes to the host port are controlled by one signal; MCIF_$\overline{\text{RW}}$. ceLynx has an additional mode, which can provide separate read and write strobes. ceLynx MCIF_$\overline{\text{RW}}$ signal can be programmed to operate as a read strobe signal only. When in this mode, it is referred to as output enable. ceLynx $\overline{\text{MCIF\_STRB}}$ signal operates as the write strobe signal. In this mode, it is referred to as write enable.

3.1.4.1 Register Settings for Multistrobe Host Interface

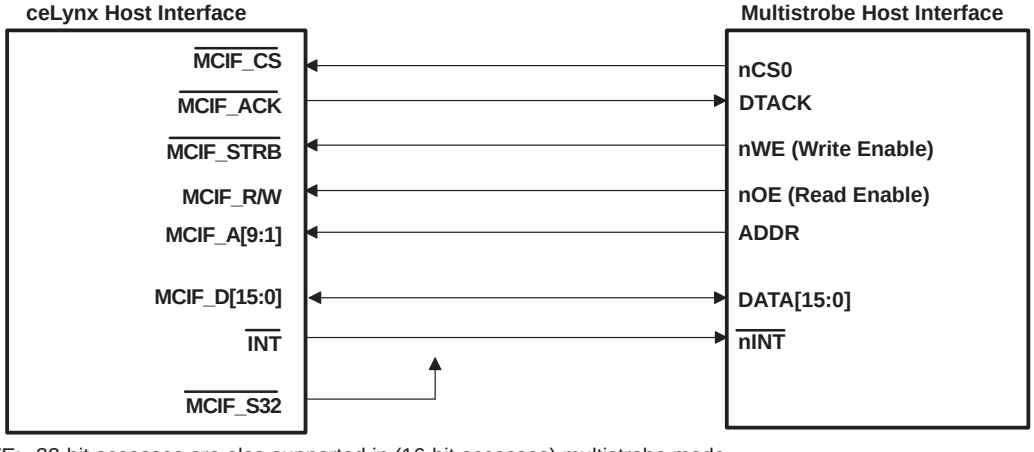
The application must use the two-wire serial interface to external EEPROM to configure these registers on power up and reset. Table 3−2 lists the register bits and their functionality. See Section 6.2.2 for the values to set in these bits.

Table 3−2. Multistrobe Mode Register Settings

REGISTER AND BIT NAME	DESCRIPTION
MCIFCFG.MCRWISOE	The host interface MCIF_$\overline{RW}$ signal operates as read (output enable) (see Note 5)
PINCFG.MCRWPOL	Controls the active level of the MCIF_$\overline{RW}$ pin (see Note 6).
PINCFG.MCCSZPOL	Controls the active-level of $\overline{\text{the MCIF\_CS}}$ pin.
PINCFG.MCSTRBZPOL	Controls the active level of $\overline{\text{the MCIF\_STRB}}$ pin. In multistrobe mode this signal is default active-low for a write request.

NOTES: 4. The $\overline{\text{MCIF\_STRB}}$ signal operates as write (input enable).
5. In multistrobe mode the default for a read request is active-low.

3.1.4.2 Connection Diagram for ceLynx − Multistrobe Mode Host Interface



NOTE: 32-bit accesses are also supported in (16-bit accesses) multistrobe mode.

Figure 3−8. Microcontroller Host Interface Connection Diagram

3.1.4.3 ceLynx − Host Port Multistrobe Functional Timing

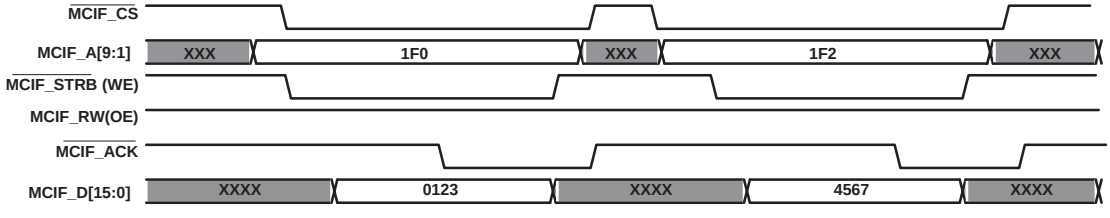


Figure 3−9. Host Port Multistrobe Timing − Write Operation

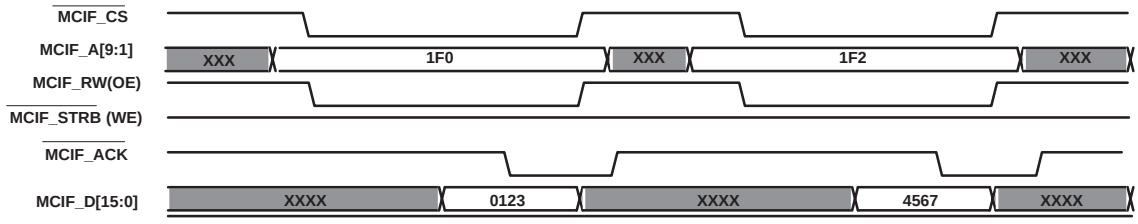


Figure 3−10. Host Port Multistrobe Timing − Read Operation

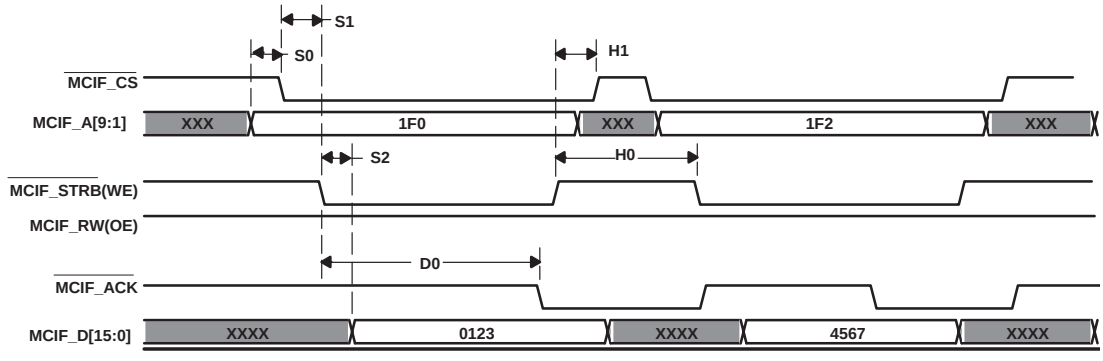


Figure 3−11. Multistrobe Mode − Write Critical Timing

Table 3−3. Multistrobe Mode − Write Critical Timing Numbers

VALUE	MIN	MAX	UNIT
S0 Setup time for address valid to MCIF_$\overline{CS}$ low	0		
S1 Setup time for MCIF_$\overline{CS}$ low to MCIF_$\overline{STRB}$ (WE) asserted	0		
S2 Setup time for MCIF_$\overline{STRB}$ (WE) asserted to beginning of data	0		
D0 Delay time from MCIF_$\overline{STRB}$ (WE) asserted to write data operation complete MCIF_$\overline{ACK}$		114	nS
H0 Hold time between two MCIF_$\overline{STRB}$ (WE) cycles	9		nS
H1 Hold time between MCIF_$\overline{STRB}$ (WE) high and MCIF_$\overline{CS}$ high	0		

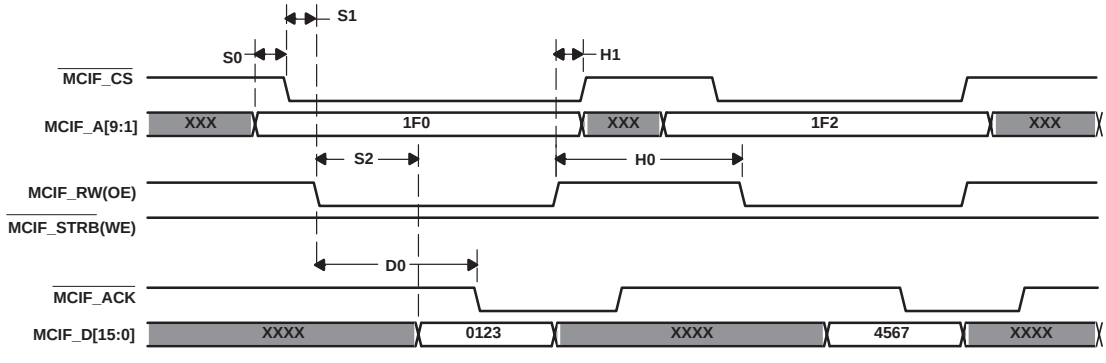


Figure 3−12. Multistrobe Mode − Read Critical Timing

Table 3−4. Multistrobe Mode − Read Critical Timing Numbers

VALUE	MIN	MAX	UNIT
S0 Setup time for address valid to $\overline{\text{MCIF\_CS}}$ low	0		
S1 Setup time for $\overline{\text{MCIF\_CS}}$ low to MCIF_$\overline{\text{RW}}$(OE) asserted	0		
S2 Setup time for MCIF_$\overline{\text{RW}}$(OE) asserted to beginning of data	0		
D0 Delay time from MCIF_$\overline{\text{RW}}$(OE) asserted to read data operation complete $\overline{\text{MCIF\_ACK}}$		114	nS
H0 Hold time between two MCIF_$\overline{\text{RW}}$(OE) cycles	9		nS
H1 Hold time between MCIF_$\overline{\text{RW}}$(OE) high and $\overline{\text{MCIF\_CS}}$ high	0		

3.2 High-Speed Data Interface (HSDI)

The high-speed data interface is designed to support high-bandwidth applications, where the access latency of the microcontroller interface is insufficient for the bandwidth of the streaming data. Examples include MPEG2 or DV streams where the upper limit of the incoming or outgoing data can be up to 60 Mbps. The HSDI can support throughputs of up to 27 MBps in byte-wide mode, and up to 66 MHz in serial mode. All supported data types can be transmitted and/or received at this interface, including asynchronous streams, asynchronous, DVB, DirecTV, and DV type data.

The high-speed data interface consists of two bidirectional, 8-bit data busses; HSDI ports A and B. Each bus has a corresponding 3-bit address bus used to select the internal FIFO that is to be written or read. The address bus is used only in multistream mode. HSDIA_A[2:0] determine the FIFO accessed by HSDI port A, and HSDIB_A[2:0] determine the FIFO accessed by HSDI port B. Each port has its own read and write control signals. Figure 3−13 shows the interface signals for each port. In general, the HSDI is a fully bidirectional interface.

The HSDI has two stream modes: single stream and multistream. In single stream mode, each HSDI port can only be connected to a maximum of one transmit buffer and one receive buffer. The HSDI accesses the buffers based on the HSDIx_$\overline{\text{RW}}$ signal.

In multistream mode, each HSDI port can be connected to multiple transmit or receive buffers. The HSDI determines which buffer to access by decoding the HSDIx_A[2:0] signals. The HSDIx_$\overline{\text{RW}}$ must be used to determine the interface direction.

The HSDI supports three synchronization modes: Mode A, Mode B and Mode C. The sync mode defines how the HSDIx_SYNC signal is used to determine packet boundaries on transmit and receive. The HSDIx_SYNC signal is input on transmit and output on receive.

The HSDIx_EN signal is an input used on transmit to indicate valid data. Data is not written to transmit buffers unless the HSDIx_EN signal is active. HSDIx_EN is also an input on receive to indicate the application is ready to receive the data. No data is received by the application until the HSDIx_EN signal is active.

The HSDIx_AV signal is an output used to indicate when data is available for reading. This signal is active once one cell of data is available in the receive buffer. For data types that use time-stamp based release, the HSDIx_AV signal is activated only after the timestamp matches the cycle timer. The signal is not used in transmit mode.

The HSDIx_$\overline{\text{RW}}$ signal is used to indicate the direction of the HSDIx. In multistream mode, the HSDIx_$\overline{\text{RW}}$ is used with the HSDIx_A[2:0] signals to determine the buffer and the direction of the access. In single stream mode, the HSDIx_$\overline{\text{RW}}$ signal is used to select the fixed transmit or receive buffer.

All HSDI control signals are programmable in their active level (*active high* or *active low*). The default is *active high*. The endianness of the byte stacking operation is programmable to either big (default) or little endian independently for transmit and receive mode.

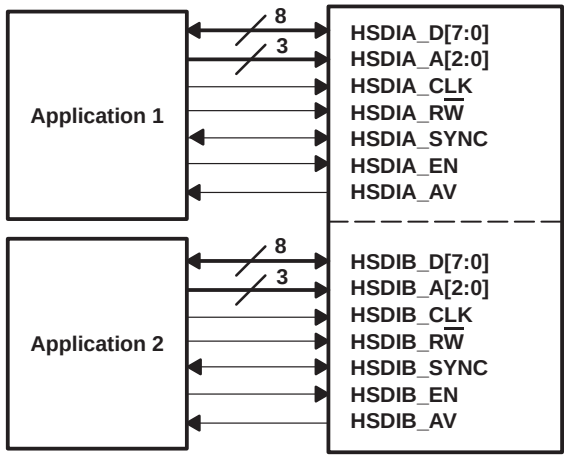


Figure 3−13. High-Speed Data Interface

Table 3−5. HSDIx_A[2:0] Bus Encoding Values

HSDx_A[2:0]	MEANING
000	HSDI Buffer 0
001	HSDI Buffer 1
010	HSDI Buffer 2
011	HSDI Buffer 3
100	HSDI Buffer 4
101	HSDI Buffer 5
110	HSDI Buffer 6
111	HSDI Buffer 7

3.2.1 Data Bus Modes

The HSDI is designed to support the widest range of applications and available MPEG2 transport demux devices. The HSDI provides two separate databus modes to address this concern: the byte wide mode and the serial mode.

3.2.1.1 Byte Wide Mode (default mode)

In byte wide mode, the full HSDIx_D[7:0] bus is used to input or output data to the HSDI ports. HSDIx_D7 is the most significant bit. This is the default mode for each HSDI port.

3.2.1.2 Serial Mode

In serial mode the HSDIx_D0 is used as a 1-bit wide mode input/output. This mode is selected using a control bit in the CFR.

The HSDIx_SYNC signal marks the packet boundaries on a bit basis. The HSDIx_EN signal should only be asserted on byte boundaries in either byte-wide or serial mode.

3.2.2 Stream Modes

The HSDI ports allow the user either to access multiple buffers from each HSDI port or to program the port to only support fixed buffers to simplify the control signals needed in the application. The two modes are multistream mode and single-stream mode (default).

3.2.2.1 Multistream Mode

Multistream mode supports all data types.

In *multistream* mode multiple data streams can be routed through a single *high-speed data interface* into different internal buffers. A three-bit buffer address is externally supplied on the *HSDIx_A[2:0] pins*. For both transmit and receive operations, this address is synchronous to the eight-bit *HSDIx_D[7:0]*. This address determines which buffer is accessed. The data must be written as complete packets. Different data types can not be mixed within packet boundaries.

The data streams on a single HSDI port can be of a different nature. For example, an asynchronous data stream can be routed to buffer 0, and two MPEG streams can be routed to buffer 1 and 2 respectively. The stream type is indicated by the buffer that is being addressed and the associated configuration.

This mode has been verified in design simulation only.

3.2.2.2 Single-Stream Mode (default mode)

The HSDI can be lined to a single transmit and signal receive buffer. The HSDIx_$\overline{RW}$ signal determines which buffer is accessed. Figure 3−14 shows an example for an application that operates both *high-speed data interfaces* in *single-stream transmit mode*. In this example the two *HSDI* modules are connected to external devices that supply a single type of data stream each. The two data streams are routed into two different transmit buffers.

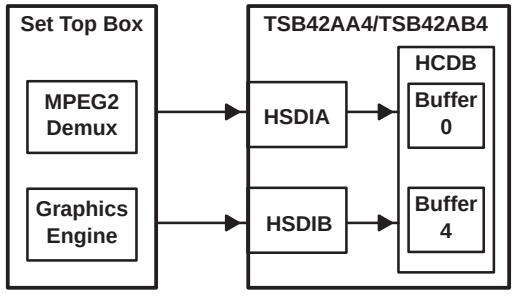


Figure 3−14. *HSDI* Single-Stream Mode Example

When operated in transmit mode, the targeted transmit FIFO is programmed in a CFR. All of the data presented to the HSDI interface is routed to this buffer. No externally supplied *HSDIx_A[2:0]* lines are needed.

When operated in receive mode, the targeted receive buffer is programmed in a CFR. The interface outputs only data received in this buffer. The HSDIx_A[2:0] lines are not driven.

In single-stream mode, each HSDI can receive one stream and transmit one stream. The HSDIx_$\overline{RW}$ signal is used to determine which buffer is accessed.

3.2.3 Data Block Synchronization Modes

The HSDI ports also allow the user to select between three different modes of identifying boundaries of data blocks when reading or writing to the HSDI ports. The synchronization mode is defined in the HSDI configuration registers. One mode can be defined per HSDI.

Data block boundaries are defined as the first and last bytes of a block of data that is input to or output from the HSDI port. Boundaries must be known by the link layer for several reasons; in order to determine when to insert a time stamp for MPEG2 type data, to distinguish between separate data blocks in a given transmit or receive FIFO, and to know when to add the 1394 header information and begin transmitting. Similar boundary considerations exist when reading data from the HSDI. Table 3−6 categorizes the synchronization modes.

Table 3−6. HSDI Synchronization Modes

SYNCHRONIZATION MODE	FIXED/VARIABLE LENGTH	DESCRIPTION
Mode A	Fixed	HSDIx_SYNC pin is ignored on transmit and high-impedance on receive. Used to receive or transmit data blocks that are a fixed length. The fixed data block length must be programmed in HSDIxCFG1.TXDBCNTREND.
Mode B	Fixed	HSDI_SYNC is active during the first byte of the data packet. Used when receiving or transmitting data packet that are fixed length. The fixed data packet length must be programmed in HSDIxCFG1.TXDBCNTREND.
Mode C	Variable	HSDI_SYNC is active during the last byte of the transfer. Used to transmit or receive variable length packets.

3.2.3.1 Mode A (default mode)

This mode is useful especially when a particular type of data with constant packet length is transmitted or received over the *HSDI*, e.g., DVB data with a packet length of 188 bytes only. The data length (in terms of bytes) must be written to the HSDIxCFG1 configuration register. An internal counter keeps track of the beginning of the data packets. During transmit operation, the externally supplied *HSDIx_SYNC* signal is ignored. During receive operation HSDIx_SYNC is in the high-impedance state.

In the transmit mode, the counter is started when the buffer is enabled. Once the counter reaches the packet length the packet is terminated and the next valid byte becomes the start of the next packet. To halt the count and prevent data from being latched, the user can deassert the HSDIx_EN enable. This disables the counter and prevents the loading of any data. Once the data is valid again the user can reassert the HSDI enable. In this mode, the *HSDIx_SYNC* signal value is ignored. In the transmit mode, sync mode A is designed for continuous back-to-back streaming only. For all noncontinuous video streaming, use sync mode B for correct synchronization of the data. If the application must use sync mode A, configure and enable the HSDI before the source starts transmitting the data onto the HSDI.

In receive mode, the first occurrence of the HSDIx_AV signal is used as an indication that data is available in the buffer. If the HSDIx_EN signal is asserted, the first word of the data is present on the data lines, and in the same cycle the HSDIx_AV signal goes high. The counter counts until the data block ends. If there is no additional data available, the HSDIx_AV signal goes low in the same cycle as the end of a packet. If additional data is still available, data continues to stream out of the HSDI. The HSDIx_EN signal can be deasserted to hold off the HSDI on any byte boundary. While the HSDIx_EN is low, the data does not change.

3.2.3.2 *Mode B*

Mode B is a common interface found on MPEG2 transport chips on the market today. The data interface functions exactly as in Mode A with the addition of a synchronization signal.

In mode B, the HSDIx_SYNC signal determines the start of a new packet. The end of a packet is determined by the internal counter. This means the application can leave enable high after the last byte of data but before the next active HSDIx_SYNC signal *without* writing incorrect data into the FIFO.

The signal is active during the same cycle as the first byte of each data block. In transmit mode this signal is an input to the HSDI. The length of a cell must be fixed and is programmed in a configuration register as in mode A.

3.2.3.3 *Mode C*

Mode C is provided for standard asynchronous packets. These packets are usually not a fixed length. In this mode the HSDIx_SYNC signal is used to indicate the end of a packet. The length of the packet is not programmed in CFRs. On transmit, data is clocked in when HSDIx_EN is active. An asserted HSDIx_SYNC

signal during a valid data byte indicates that the current byte is the last byte of a packet. Internally the packet is marked and sent to the internal buffer.

3.2.3.4 HSDI Functional Timing Diagrams − Read

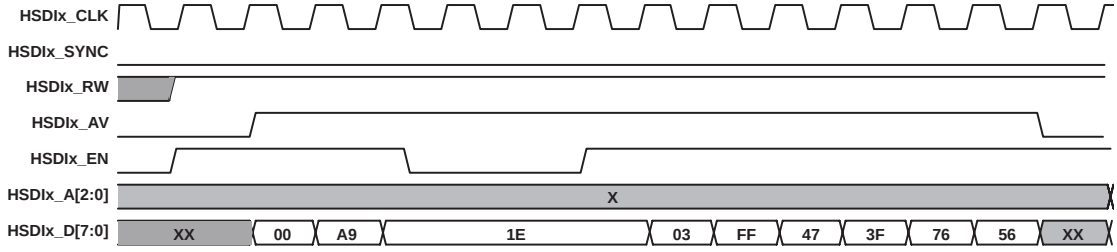


Figure 3−15. HSDI Read, Byte-Wide Data Bus, Sync Mode A

In sync mode A read in Figure 3−15 HSDIx_EN is showed going high before data is available. In this case, data is not read out until the HSDIx_AV signal is active as well. However, if HSDIx_EN is not active, all control signals on the HSDI are ignored.

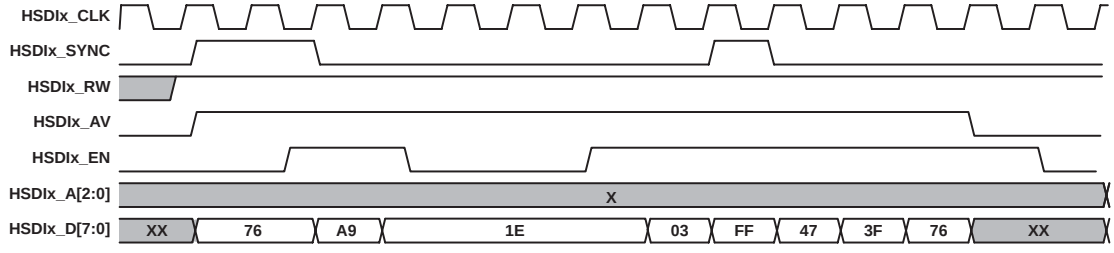


Figure 3−16. HSDI Read, Byte-Wide Data Bus, Sync Mode B

In sync mode B read in Figure 3−16, the packets are a fixed length of four bytes. The first packet consists of 76 A9 1E 03. The second packet consists of FF 47 3F 76. The HSDIx_AV signal goes high to indicate data is available in the FIFO. At the same time, the first byte of data is presented on HSDIx_D[7:0]. The data does not change until the HSDIx_EN signal is activated. On the next clock after the HSDIx_EN signal goes high, the HSDI outputs the next byte of data. The HSDIx_SYNC signal is high during the first byte of the packet. For the first packet, it is high during the 76. For the second packet, it is high during the FF.

HSDIx_EN can be deasserted to hold off reads from the HSDI. If HSDIx_EN is deasserted while data is still in the FIFO, ceLynx holds the current byte of data on the data bus until the HSDIx_EN signal is reasserted. In the example in Figure 3−16, the HSDIx_EN signal is deasserted in the middle of the transmission of the third byte of data, 1E. This byte is driven on the bus until the HSDIx_EN signal is sampled asserted on a rising clock edge.

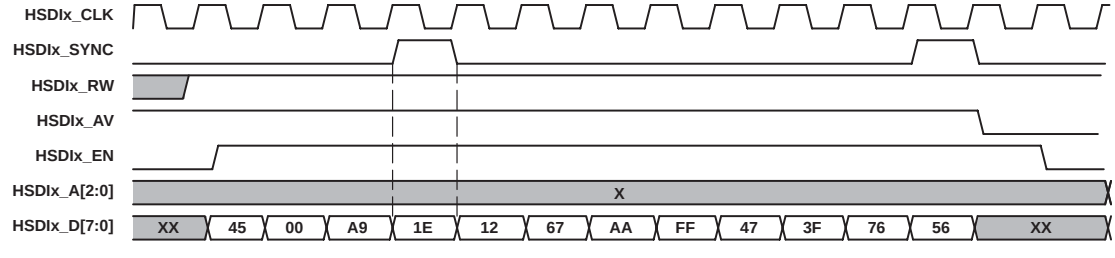


Figure 3−17. HSDI Read, Byte Wide Data Bus, Sync Mode C

In sync mode C, Figure 3−17, the HSDIx_SYNC signal is used to indicate the last byte of data. In this example, the last byte of the first packet is 1E. The last byte of the second packet is 56. Data is valid on the bus as soon as HSDIx_EN is active. Data does not change until the HSDIx_EN signal is active.

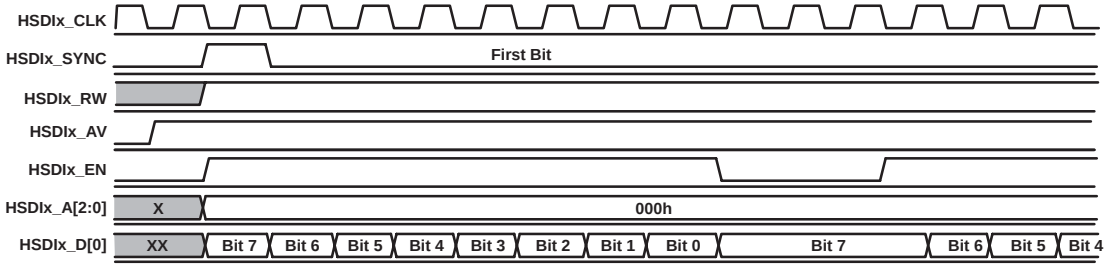


Figure 3−18. HSDI Read, Serial Data Bus, Sync Mode B

Figure 3−18 shows serial mode functional timing for sync mode B. Sync modes A and C would have similar timing. For sync mode A, no HSDIx_SYNC signal is used. For sync mode B, the HSDIx_SYNC signal indicates the first byte of the packet. For sync mode C, the HSDIx_SYNC signal indicates the last byte of the packet. The function of the HSDIx_SYNC signal is programmable in CFR. In Figure 3−18, the HSDIx_SYNC signal is driven for one bit. It can also be asserted for an entire byte.

The HSDIx_EN and HSDIx_AV signals function the same as byte mode. HSDIx_EN must be asserted and deasserted on quadlet boundaries, except in DirecTV 130 byte mode.

The bit ordering can be programmed. The default state is to read the most significant bit first.

This mode has been verified in design simulation only.

3.2.4 HSDI Functional Timing − Write

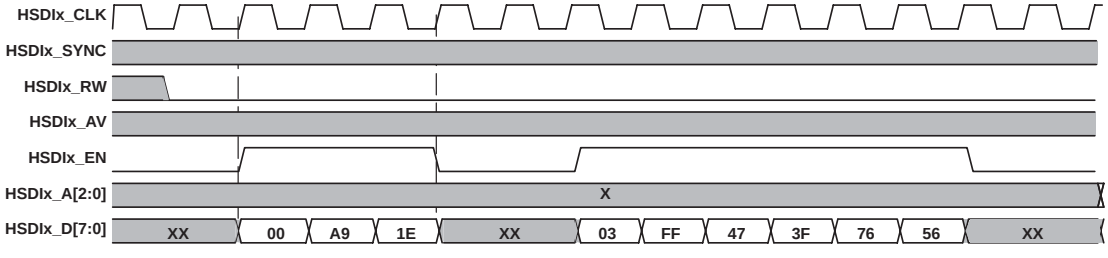


Figure 3−19. HSDI Write, Byte-Wide Data Bus, Sync Mode A

In sync mode A write, Figure 3−19, the HSDIx_SYNC signal is ignored by the HSDI. An internal counter keeps track of packet boundaries. The HSDIx_EN signal should only be asserted for valid data on the bus. Otherwise, invalid data is written into the FIFO.

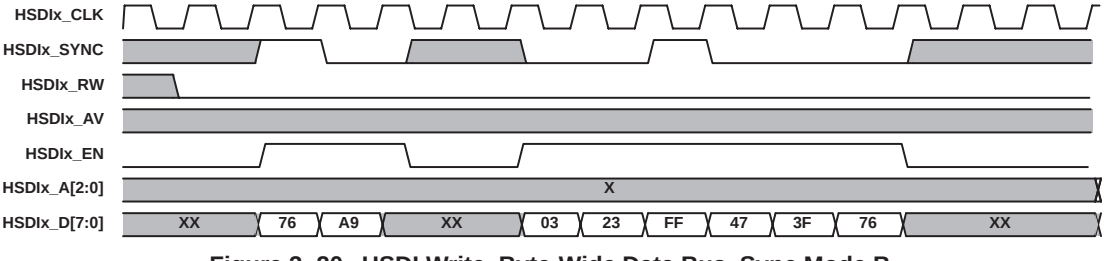


Figure 3−20. HSDI Write, Byte-Wide Data Bus, Sync Mode B

In sync mode B write, Figure 3−20, the HSDIx_SYNC signal indicates the start of the next packet. In this example, the first packet is 76 A9 03 23. The second packet is FF 47 3F 76. All packets must be at least 4 bytes long. The HSDIx_SYNC signals are ignored if HSDIx_EN is not active.

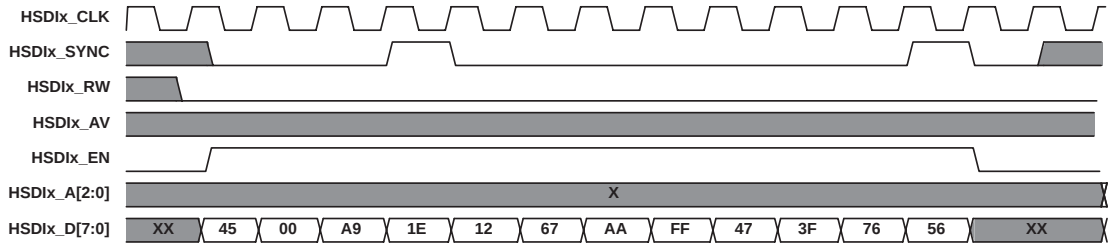


Figure 3−21. HSDI Write, Byte Wide Data Bus, Sync Mode C

In sync mode C write, Figure 3−21, the HSDIx_SYNC signal indicates the end of the packet. The packets can be variable lengths.

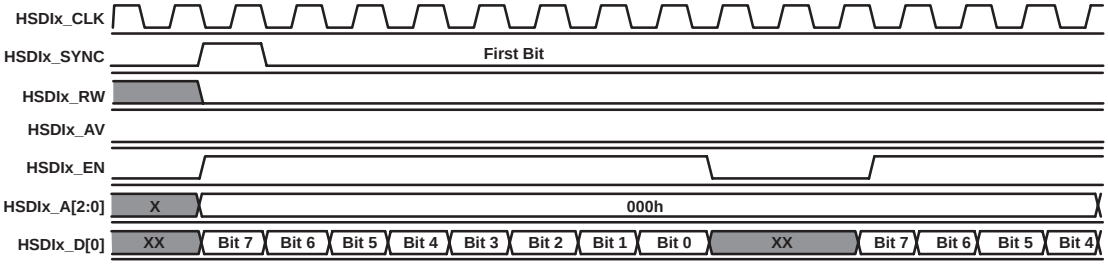


Figure 3−22. HSDI Write, Serial Data Bus, Sync Mode B

Figure 3−22 shows serial mode functional timing for sync mode B. Sync modes A and C have similar timing. For sync mode A, no HSDIx_SYNC signal is used. For sync mode B, the HSDIx_SYNC signal indicates the first byte of the packet. For sync mode C, the HSDIx_SYNC signal indicates the last byte of the packet. The function of the HSDIx_SYNC signal is programmable in CFR. In Figure 3−22, the HSDIx_SYNC signal is driven for one bit. It can also be asserted for an entire byte.

The HSDIx_EN functions the same as byte mode. HSDIx_EN must be asserted and deasserted on quadlet boundaries, except for DirecTV 130.

The bit ordering can be programmed. The default state is to write the most significant bit first.

3.2.5 System-Dependent Implementations

For any DirecTV or DVB application that does not provide the byte start, sync mode A is not recommended. Instead, use sync mode B to synchronize the data correctly on the first byte of each DirecTV or DVB cell latched into the TX buffer. An external byte start must be provided by adding external logic to enable the HSDIx_SYNC signal. An example of the byte start circuit is provided in Figure 3−23.

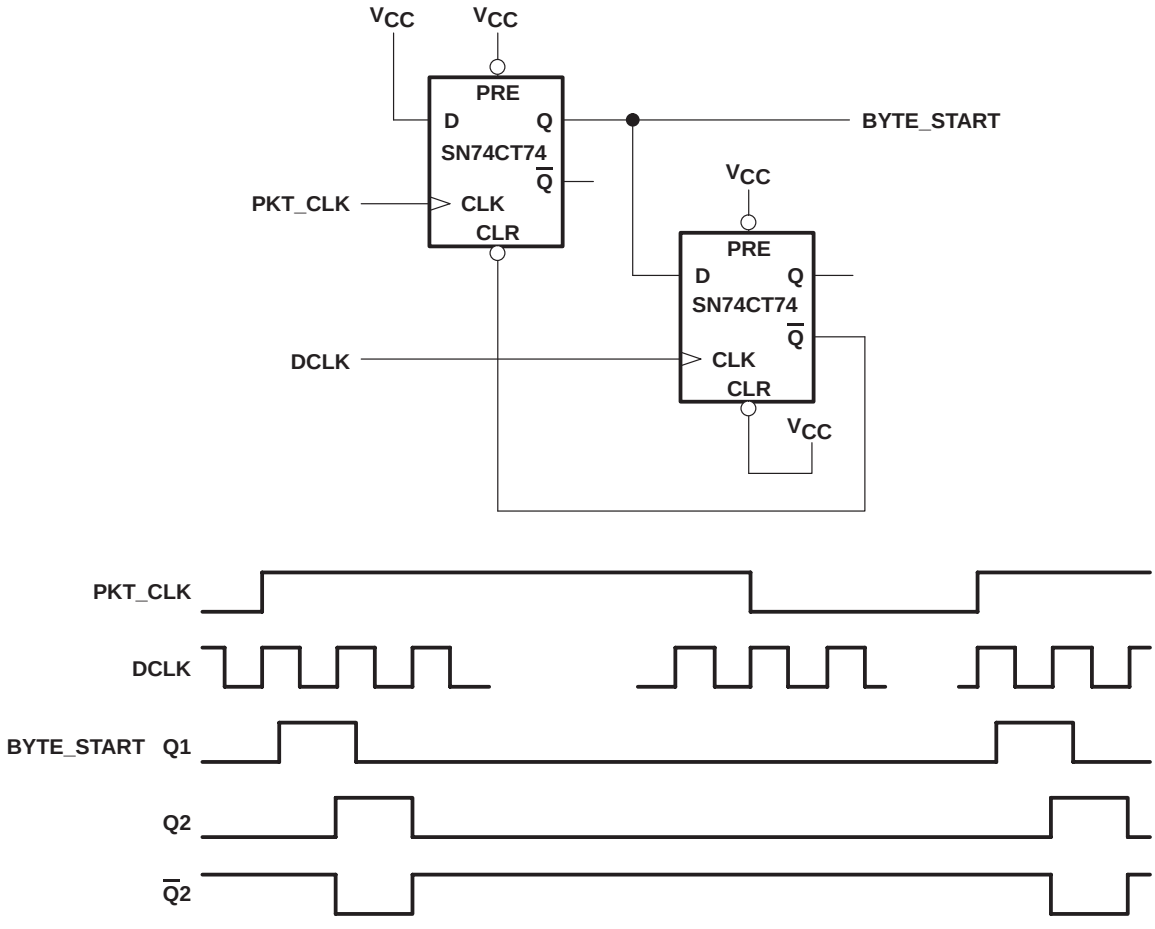


Figure 3−23. Typical Byte Start Circuit

For any video application, if the application provides the data clock only during the data-valid period, it must invert the DCLK to match the data clocking edge to the HSDIx_CLK to preclude dropping any bytes at the end of the data-valid period.

3.2.6 HSDI Functional Timing for Multistream Modes

The following explains timing for HSDI multistream modes. These are modes where the HSDI accesses different buffers by changing the HSDIx_ADDR lines.

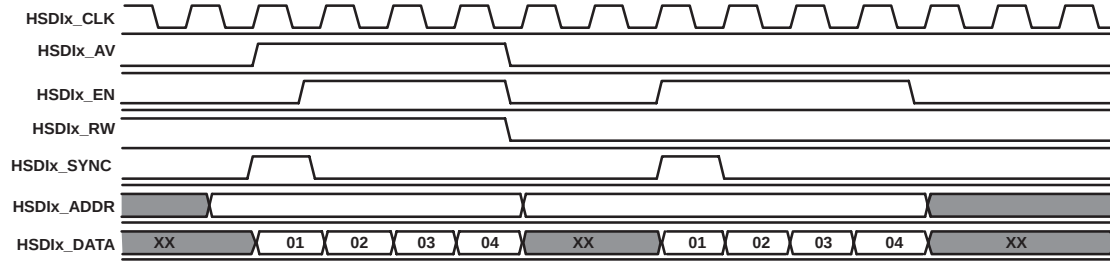


Figure 3−24. Functional Timing for Multistream Mode (Read and Write)

1. The first access is a read. The application should address the read buffer by default and monitor the HSDIx_AV signal. The HSDIx_AV signal is not asserted unless that specific read buffer is addressed. The application can also watch the RCVPKT interrupt for the specified read buffer to determine when to drive the HSDIx_ADDR line.
   a. The application drives the HSDIx_$\overline{RW}$ signal to indicate a read. It also drives the HSDIx_ADDR signals to address the read buffer. In general, these two signals must be driven for at least two HSDIx_CLK cycles before the HSDIx_EN can be driven.
   b. HSDIx_AV goes active at the same time as HSDIx_SYNC and HSDIx_DATA.
   c. The application asserts HSDIx_EN two clock cycles after the address and $\overline{RW}$ lines have been asserted. Data is read out of the interface. In this case, the application had asserted HSDIx_EN and HSDIx_$\overline{RW}$ one HSDIx_CLK before the HSDI_AV before driving the HSDIx_EN signal.
   d. The application drives HSDIx_EN low when HSDIx_AV is low. The read is complete.
2. The second access is a write.
   a. The HSDIx_RW signal is driven low to indicate a write. The HSDIx_ADDR is asserted for the specified buffer. These signals must be valid for two HSDIx_CLK cycles before enable or data.
   b. HSDIx_EN is driven high at the same time as HSDIx_SYNC and HSDIx_DATA.
   c. Data is written to the desired buffer. Write is complete when HSDIx_EN is disabled.

3.2.7 HSDI Critical Timing

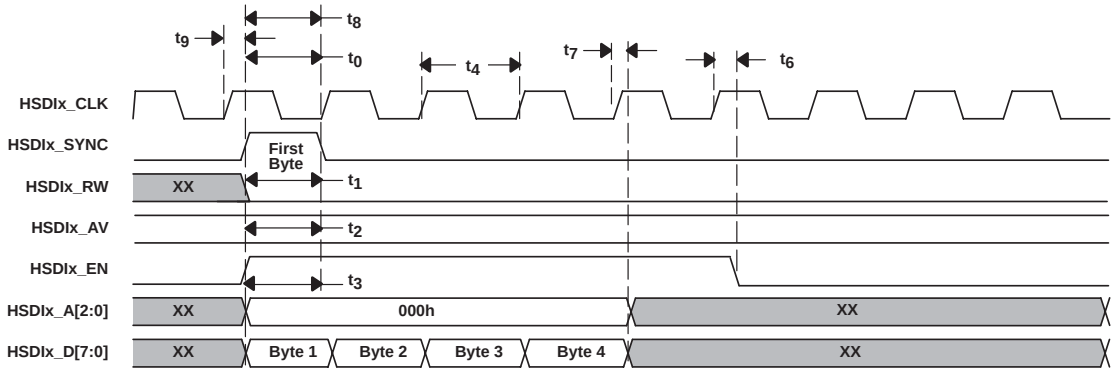


Figure 3−25. HSDI Interface Critical Timing

Table 3−7. HSDI Critical Timing Parameters

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
t_0	Setup time, HSDIx_SYNC to HSDIx_CLK	4		ns
t_1	Setup time, HSDIx_$R\overline{W}$ to HSDIx_CLK	12		ns
t_2	Setup time, HSDIx_EN to HSDIx_CLK	4.6		ns
t_3	Setup time, HSDIx_DATA to HSDIx_CLK	4		ns
t_4	Clock frequency, byte wide mode	10 K	27 M	Hz
	Clock frequency, serial mode	10 K	66 M	
t_5	Hold time, HSDIx_CLK to HSDIx_SYNC	0		ns
t_6	Hold time, HSDIx_CLK to HSDIx_EN	0		ns
t_7	Hold time, HSDIx_CLK to HSDIx_DATA, ADDR	0		ns
t_8	Setup time, address to HSDIx_CLK	14		ns
t_9†	HSDIx_CLK to HSDIx_D[7:0], byte wide mode		12	ns
	HSDIx_CLK to HSDIx_D[7:0], serial mode		8	

† For HSDI Read operation only

All timing examples are shown with a byte-wide data bus. Serial access would be identical. A full byte must be written or read before HSDIx_EN can be deactivated.

3.3 PHY-Link Interface

The physical layer interface (PHY) of the ceLynx conforms to the description and definition in Section 5 of the 1394.a specification. The interface is capable of transmitting and receiving at speeds up to 400 Mbps.

The TI bus holder method of dc isolation is included in the ceLynx device. Only a single capacitor on the PHY-link interface signals needs to be added to implement isolation.

3.4 Two-Wire Serial Interface

The two-wire serial interface gives the system an easy way to load ceLynx configuration registers on power up or reset. It also makes manufacturing easy, because the individual global unique ID (GUID) is easier to implement in EEPROM.

ceLynx automatically reads from the two-wire serial interface port on power up or reset. The host controller is not involved. The software can also initiate a two-wire serial interface reload by CFR. ceLynx can only interface to one EEPROM and is always the master. ceLynx samples the SCL pin at power up to determine if an EEPROM is present. The two-wire serial interface port can be disabled by tying the SCL signal to ground.

The ceLynx two-wire serial interface consists of two active signals, serial data line (SDA) and serial clock line (SCL), and an internal ground connection. These two signals interface to any 3.3-V EEPROM designed for two-wire serial interfaces. Since ceLynx is master, the SCL is used as an output. This clock frequency is generated by ceLynx and is a maximum of 100 kHz.

When ceLynx performs a read of the two-wire serial interface, the data is written directly to the intended hardware configuration register. No assistance from the application is necessary. The data and address can be monitored in the serial STAT0 and serial STAT1 registers for test purposes only. The information in these registers is valid for one two-wire serial interface clock, or 120 SCLKs.

The 1394 command and status registers that are not implemented in ceLynx hardware, such as the configuration ROM, can be configured to load from EEPROM to an internal buffer. When the two-wire serial interface read operation is finished, as signaled by an interrupt, the host controller can load these values from the data buffer to the correct address space.

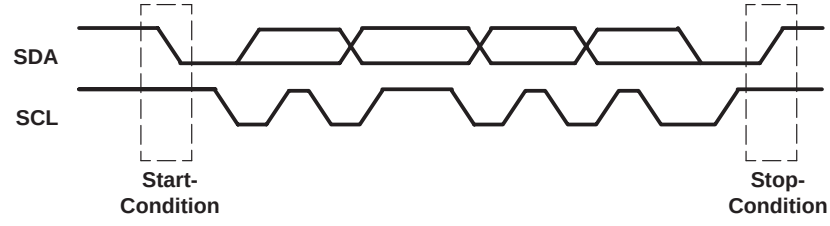
3.4.1 Two-Wire Serial-Interface Bus Protocol

A start-condition generated from ceLynx starts an action at the two-wire serial interface-bus. While every communication is 8 bits, a ninth bit acknowledge is needed. The first bit is the MSB, the eighth is the LSB.

ceLynx always generates the clock at the SCL line. The data at the SDA line has to be changed in the low phase of the clock only. Changing the SDA line in the clock-high-phase is interpreted as start- or stop-condition.

The first byte sent by ceLynx is the device address of the EEPROM. The data transfer begins with 8 bits of data and a 1-bit ACK. The ACK is given by the receiving unit. ceLynx generates a *stop-condition* to end the communication.

Start/Stop-Condition



Timing: Data-Transfer and Acknowledge

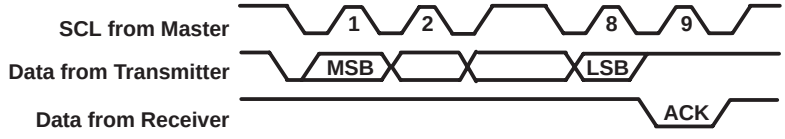


Figure 3−26. Two-Wire Serial Interface Bus Protocol

3.4.2 ceLynx/Two-Wire Serial-Interface EEPROM Protocol

Definitions:
MASTER: ceLynx
SLAVE: EEPROM

Device-Address Format

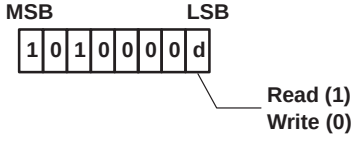


Figure 3−27. EEPROM Protocol Device Address Format

This operation sets the internal address counter of the EEPROM. Any read operation after that starts at the specified address.

Typical Read Operation

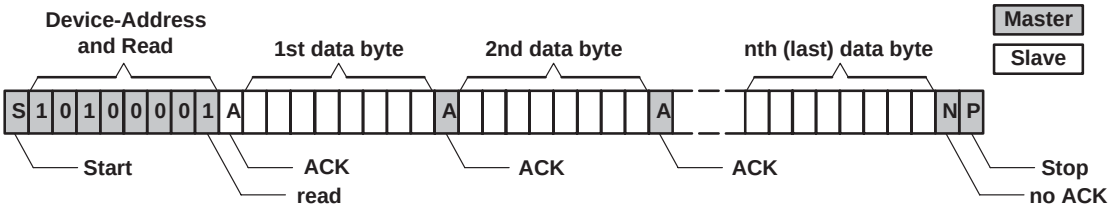


Figure 3−28. EEPROM Protocol Typical Read Operation

3.4.3 EEPROM Data Format

The data in the EEPROM is organized blockwise and each block is organized by quadlets. The first quadlet is the header of each block. The format of a header is as follows:

The block format for the EEPROM is shown in Figure 3−27. The header consists of one quadlet. However, the quadlet is stored byte-wise in the EEPROM. Figure 3−28 shows how the header for each block is stored in EEPROM.

Block 1 Header Data	Block 2 Header Data	Block 3 Header Data

Figure 3−29. Block Format for EEPROM

3.5 Block Header

Byte 0								Byte 1								Byte 2								Byte 3							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Last Block								Checksum								Length (Number of Quadlets)								Address [9:2]							

Figure 3−30. EEPROM Header Format

3.5.1 Header Addressing

The address is the starting ceLynx CFR offset address for the configuration block. This address is incremented for each data byte in the data block. ceLynx automatically programs the register with the EEPROM value. The address is calculated from bits [9:2] of the CFR offset address of ceLynx. For example, to write data from EEPROM to register 204 [DB(7)CFG0].

CFR Address 0x204 [DB(7)CFG)]												
Bit	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	1	0	0	0	0	0	0	1	0	0

EEPROM Address =
bits [9:2] =
1000 0001 = 0x81

The data loaded from EEPROM is written in reverse byte order. Byte 3 is programmed into the EEPROM first. Byte 0 is programmed into the EEPROM last. The bit positions are maintained.

Byte 0								Byte 1								Byte 2								Byte 3							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Programmed in EEPROM last																								Programmed in EEPROM first							

Example 1: Program the EEPROM to load the following values to ceLynx CFRs

REGISTER	VALUE
DB(7)CFG0	0000 0002
DB(7)CFG1	07F0 07FF
DB(7)CFG2	0000 0000
DB(7)CFG3	0000 0000
DB(7)ACC0	0123 4567
DB(7)ACC1	89AB CDEF

Solution:

Header Quadlet

81	Starting address = 81 for addr DB(7)CFG0
06	Number of quadlets = 6
A7	Check sum
80	Last block flag

Data Block

02	Byte 3 value for register 204
00	Byte 2 value for register 204
00	Byte 1 value for address 204
00	Byte 0 value for address 204
FF	Byte 3 value for register 208
07	Byte 2 value for register 208
F0	Byte 1 value for address 208
07	Byte 0 value for address 208
00	Byte 3 value for register 20C
00	Byte 2 value for register 20C
00	Byte 1 value for address 20C
00	Byte 0 value for address 20C
00	Byte 3 value for register 210
00	Byte 2 value for register 210
00	Byte 1 value for address 210
00	Byte 0 value for address 210
67	Byte 3 value for register 214
45	Byte 2 value for register 214
23	Byte 1 value for address 214
01	Byte 0 value for address 214
EF	Byte 3 value for register 218
CD	Byte 2 value for register 218
AB	Byte 1 value for address 218
89	Byte 0 value for address 218

If the application wants to load a 1394 CSR register not implemented in hardware, the EEPROM header must specify a data buffer for the data block address. The EEPROM data is loaded into the selected buffer. At the end of the two-wire serial interface transfer from EEPROM, the ceLynx signals the two-wire serial interface DONE interrupt. The host processor can read this data out of the data buffer and place it at the appropriate memory location. The selected buffer has some requirements.

- The buffer must be a receive buffer. Receive operation must not be enabled. Buffer 3 in the ceLynx default setting is a good example of an appropriate receive buffer.
- The buffer can not have time stamp stripping enabled.
- The HSDIA or HSDIB ports must not be enabled for the selected buffer.

Example: The data block programmed in EEPROM is the device Config ROM. Since there are no Config ROM registers in hardware, the EEPROM must write this data to a receive buffer. In this example, buffer 3 (default Reserved RX) is selected.

Only one quadlet of data can be written per data block using the method below. Every quadlet must have its own address in the header block. All quadlets except the last are written to DB(N)ACC0.The last quadlet is written to the DB(N)ACC1 register.

Example 2: Program the EEPROM to load the following values to ceLynx CSR via data buffer 3

REGISTER	VALUE
DB(3)ACC0	041F 6ED4
DB(3)ACC0	3133 3934
DB(3)ACC1	20FF 9000

Solution:

Header Quadlet 1

7D	Starting address = 7D for addr DB(3)ACC0
01	Number of quadlets = 1
0B	Check sum
00	Last block flag

Data Block 1

D4	Byte 3 value for register 1B4
6E	Byte 2 value for register 1B4
1F	Byte 1 value for address 1B4
04	Byte 0 value for address 1B4

Header Quadlet 2

7D	Starting address = 7D for addr DB(3)ACC0
01	Number of quadlets = 1
A5	Check sum
00	Last block flag

Data Block 2

34	Byte 3 value for register 1B4
39	Byte 2 value for register 1B4
33	Byte 1 value for address 1B4
31	Byte 0 value for address 1B4

Header Quadlet 3

7E	Starting address = 7E for addr DB(3)ACC1
01	Number of quadlets = 1
E5	Check sum
80	Last block flag

Data Block 3

00	Byte 3 value for register 1B8
90	Byte 2 value for register 1B8
FF	Byte 1 value for address 1B8
20	Byte 0 value for address 1B8

Example 3: Checksum Calculation

The EEPROM data block is made up of two quadlets:

	Byte 0	Byte 1	Byte 2	Byte 3
Quadlet 1	0000 0100	0001 1111	0110 1110	1101 0100
Quadlet 2	0011 0001	0011 0011	0011 1001	0011 0100

To calculate the checksum:

1010 1010	Start with 0xAA
0000 0100	XOR Quadlet 1 Byte0
1010 1110	
0001 1111	XOR Quadlet 1 Byte 1
1011 0001	
0110 1110	XOR Quadlet 1 Byte 2
1101 1111	
1101 0100	XOR Quadlet 1 Byte 3
0000 1011	
0011 0001	XOR Quadlet 2 Byte 0
0011 1010	
0011 0011	XOR Quadlet 2 Byte 1
0000 1001	
0011 1001	XOR Quadlet 2 Byte 2
0011 0000	
0011 0100	XOR Quadlet 2 Byte 3
0000 0100	Final Data Block Checksum

3.5.2 Header - Last Block Bit

The last-block flag indicates that this is the last valid block in the EEPROM. After this data block, no additional data blocks are expected.

3.6 CFR Address Location and Bit Assignment

Serial STAT0 **Address: 018h**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						Two-wire serial interface ADDR																					RELOAD	DONE	TIMINGER	CKSUMER	NOEEPROM

Serial STAT1 **Address: 01Ch**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Two-wire serial interface DATA																															

3.7 CFR Bits: Serial STAT0 and Serial STAT1 Registers

RELOAD	When RELOAD is 1, the EEPROM values are automatically loaded via the two-wire serial interface.
DONE	This bit indicates the completion of serial EEPROM download. The application can terminate the two-wire serial interface download prematurely by writing to this bit.
TIMINGER	This bit is set when an expected acknowledge is not received.
CKSUMER	This bit is set when the internally generated checksum does not match the EEPROM checksum.
NOEEPROM	No EEPROM is detected
ADDR[25:16]	Internal ceLynx location currently accessed by two-wire serial interface. This is provided for diagnostic purposes only.
DATA[31:0]	Current quadlet provided by two-wire serial interface. This is provided for diagnostic purposes only.

3.7.1 Operation

The two-wire serial interface is based on the functionality of a two-wire serial interface master. However, there is no collision detection and no bus synchronization implemented. This serial interface should be used as a single master without multimaster functionality.

The two-wire serial interface will perform one function only: after a reset is given it will read the contents of a connected EEPROM and write it to internal ceLynx-registers.

This function can be divided in three main phases:

- Check if EEPROM is present
- Set EEPROM-Address
- Read EEPROM-Data

3.7.1.1 Check

After a ceLynx hardware reset, the serial interface checks whether or not there is an EEPROM connected to the bus. This happens by sampling the SCL-line during the internal reset phase. If a 0 has been sampled, no EEPROM is connected to the bus and the state machine is set to the end state.

3.7.1.2 Set Address

If an EEPROM is detected, then the two-wire serial interface tries to send a write-request to the EEPROM. If the EEPROM responds, then the start address (0000h) will be written to ceLynx.

3.7.1.3 Read Data

After a successful address-setting the two-wire serial interface starts reading the data from the EEPROM. The first EEPROM address is 0000. The *last block* bit in the header indicates the end of the EEPROM data.

4 Internal Functions

4.1 Data Buffers

4.1.1 Byte Stacking and Endianness

All access to and from the internal transmit and receive FIFOs is 32 bits wide. Since the HSDI is only 8 bits (or one byte) wide, a byte stack/unstack operation must be performed at the HSDI data port. The order in which bytes are stacked/unstacked determines the endianness. This *endianness* is programmable. (note that the endianess setting does not affect the stacking of individual bits into the first byte buffer for the serial mode. This stacking is fixed and always expects to receive the bits in order

Selecting big endian would put the first byte received into the most significant bit location of the stacking buffer, and each consecutive byte into successively lower significant byte locations. Selecting little endian would put the first byte received into the least significant byte location and each consecutive byte into successively higher significant byte locations.

The endianess of the byte stacking operation can be programmed to either *little endian* or *big endian* (default) independently for each port.

4.1.2 Buffer Overflow/Underflow Status

The *GPIO* signals can be used for applications where the HSDI host needs to burst data into a ceLynx transmit buffer and will need a look ahead indicator of the buffer's content status. This allows for a more efficient memory transfer from the applications memory space to the transmit FIFO since the host controller could start and stop memory transfers on appropriate boundaries. The full and empty levels of each buffer are programmable via CFRs by the host controller to allow the user customization when the controller is notified of a pending full or empty status. Since these signals are application dependent, they are routed to multifunction pins (*GPIO*) on the device. The buffers also have programmable watermarks, which can cause interrupts to the external CPU.

4.1.3 Data Buffer Setup

The data buffer can be programmed in up to eight different partitions. Because of this, the registers are usually described once, but have eight different instances to control the eight different buffers. For example, the DB(N)CFG0 register is the description for HSDI buffer settings. The actual settings for buffer 0 are programmed in register 0x15C. The settings for buffer 1 are programmed in register 0x174.

The data buffers have default settings for data type and direction. The transmit data path has default values for header registers which match the buffer defaults.

If the buffer defaults are changed, the header registers must be reprogrammed to reflect the change.

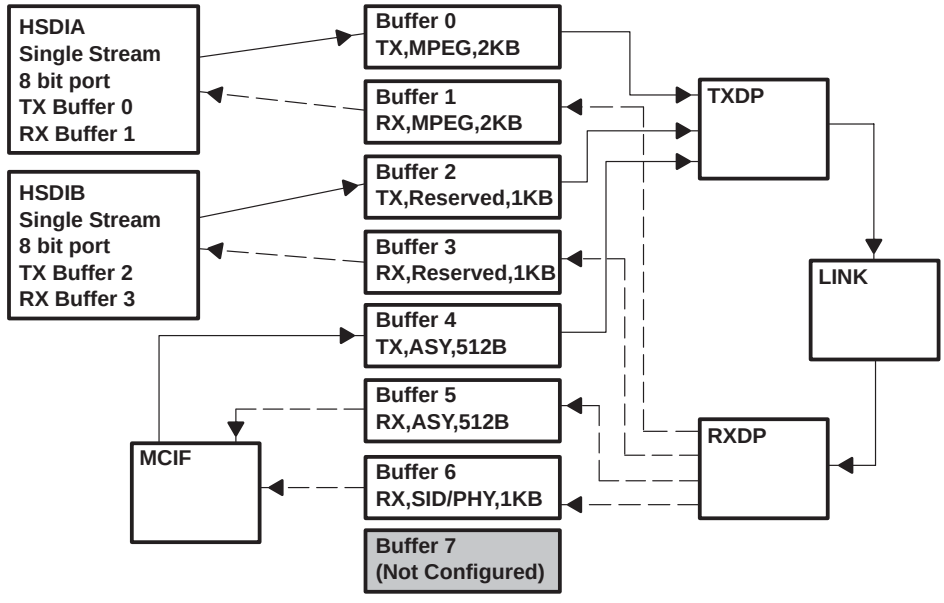


Figure 4−1. Data Buffer Default Settings

4.1.4 Buffer Flush (DBCTL.BUFxFLSH) for Video Data TX/RX

4.1.4.1 Buffer Flush in TX Buffer 0/1 Mapped to the HSDIx Port

When the direction of buffer 0/1 is configured for TX, the following sequence must be performed to completely flush the buffer. This sequence is necessary for buffer 0 and 1 only. For DV applications or any applications that do not require the use of the cipher, using a buffer other than 0 or 1 is recommended.

1. Source stops transmitting, application stops outputting data to the HSDI or disables the HSDI (HSDIx_CFG0.HSDIxEN = 0).
2. Disable the TX buffer (DBxCFG0.BUFEN = 0).
3. Write a dummy quadlet to the DB(N)_ACC1.BUFACCCFRM register.
4. Check for DBSTATx.BUFxCELLAV = 1.
5. Flush the buffer by setting DBCTL.BUFxFLSH = 1.
6. Reset the HSDI by setting HSDIx_CFG0.HSDIxRST = 1.
7. Enable TX buffer (DBxCFG0.BUFEN = 1)
8. Source starts. Re−enable the HSDI (HSDIx_CFG0.HSDIxEN = 1).

4.1.4.2 Buffer Flush in RX Buffer

When flushing the RX buffer, the following sequence needs to be performed to avoid any partial packets remaining in the receive data path (RXDP).

1. Disable the RX buffer (DBxCFG0.BUFEN = 0).
2. Wait for the next ISO cycle.
3. Flush the buffer by setting DBCTL.BUFxFLSH = 1.
4. Check for DBSTATx.BUFxCELLAV = 0.
5. Enable the RX buffer (DBxCFG0.BUFEN = 1).

4.2 Time Stamping and Aging

Most time stamp and aging functionality is controlled through register DB(N)CFG0. The critical control bits are listed in Table 4−1. Time stamping is not supported on the host port.

Table 4−1. Time Stamp and Aging Control Bits

BIT NAME	DESCRIPTION
DB(N)CFG0.TSRELEASE	For receive operation, this control bit holds a packet in the associated buffer until its time stamp is equal to current cycle timer value. It then releases the packet to the application. For transmit operation, this control bit is used to play back prerecorded MPEG2 data. It holds the data packet until the time stamp (without offset) is equal to the current cycle time before transmitting the packet over 1394.
DB(N)CFG0.TSAGE	For receive operation, this control bit flushes all packets with expired time stamps in an associated buffer. For transmit operation, this control bit flushes packets waiting to be transmitted whose time stamps equal the current cycle timer value. This is used to prevent ceLynx from transmitting old MPEG2 packets over 1394.
DB(N)CFG0.TSINSERT	For transmit operations, this control bit adds a time stamp to the transmitted data stream. This time stamp value is equal to the current cycle timer value plus a programmable offset.
DB(N)CFG0.TSSTRIP	For receive operations, this control bit strips time stamps from the data in the receive buffer. This control bit only operates if all other data headers are also stripped.

The ceLynx does not support time stamping of the formatted ISO packets transmitted or received through the host interface. Time stamp operations are supported only through the HSDI.

4.2.1 Time Stamp and Aging for MPEG2 Data

The ceLynx uses time stamping to preserve the temporal relationship of MPEG2 (DirecTV™) packets in a transport stream while being transmitted over 1394.

The transmitting ceLynx (transmitting onto 1394) places a time stamp on each MPEG2 cell it transmits. The time stamp value is the sum of the current value of the 1394 cycle timer and a user programmable transmit offset value. This value is programmed in register DB(N)CFG2.

The transmitting ceLynx can age a packet (or flush it from the FIFO) if it is not transmitted in time. This is to avoid transmitting invalid time stamps over 1394. If the packet is not transmitted before the time stamp plus transmit offset equals the cycle timer, the packet is aged. If transmit aging is used, a transmit offset must be used.

See Figure 4−2 for an explanation of packet aging.

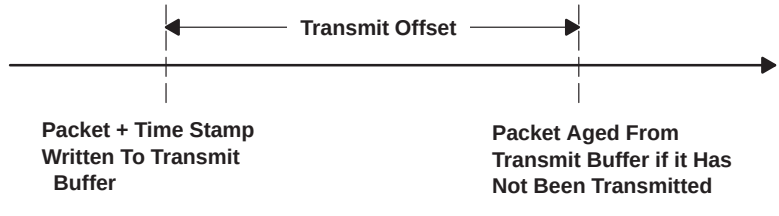


Figure 4−2. MPEG2 Transmit and Aging

The receiving ceLynx decodes the time stamp upon receive. The MPEG2 packet is released to the application when the incoming time stamp is equal to the current cycle timer. When the data is released to the application, the HSDI will indicate data is available then the application is able to read data from the buffer.

An offset, programmed in ceLynx CFRs, can be added to the receiver time stamp. The time stamp plus the the offset value determines when a packet is aged in the buffer. A packet is aged when the receive time stamp plus offset value is less than the current cycle time. At this point, the packet is flushed from the buffer. If receive aging is used, a receive offset must be added.

See Figure 4−3 for an explanation of packet again.

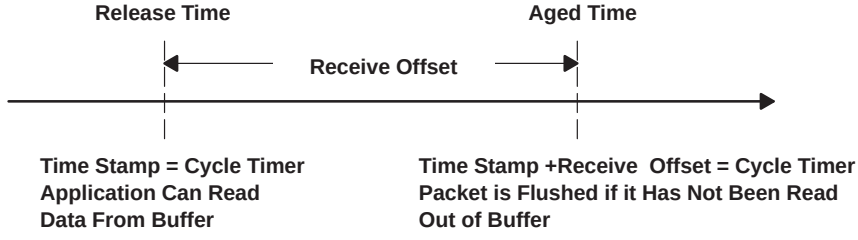


Figure 4−3. MPEG2 Receive, Release, and Aging

4.2.1.1 MPEG2 Time Stamp Calculation on Transmit

The transmit time stamp is computed by adding an offset value to the current cycle timer value. The offset is programmed in DB(N)CFG2 register. The determination of the transmit time stamp is shown in Figure 4−4.

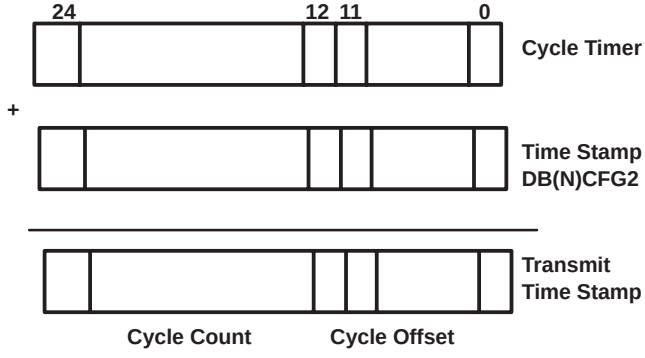


Figure 4−4. Determination of Transmit Time Stamp

The time stamp values are limited by the restraints of the 125 μs 1394 isochronous cycle. The cycle timer operates using the internal 24.576-MHz clock. When the cycle offset reaches *3071*, 125 μs have elapsed. (3071/24.576 MHz = 125 μs) It is necessary to limit the cycle offset value to equal or less than 3071 to avoid creating an invalid time stamp. When the cycle offset reaches 3071, it rolls over to zero and starts again. If the sum of the cycle timer value and the transmit offset results in cycle offset greater than 3071, the cycle count field is incremented by one and the new cycle offset is (cycle offset – 3072.)

The cycle count operates at a frequency of 8 kHz. (1/125 μs = 8 kHz). One second has elapsed every time the cycle count reached 8000. The cycle count rolls over after it reaches 7999. If the sum of the cycle timer value and the transmit offset results in cycle count greater than 7999, the seconds count field is incremented by one and the new cycle count is (cycle count – 8000.)

Table 4−2 shows the allowable values of the transmit time stamp.

Table 4−2. Allowable Values for 1394 Time Stamps

BIT NUMBER	VALUE	VALID RANGE
24:12	Cycle Count	Between 0 and 7999
11:0	Cycle Offset	Between 0 and 3071

4.2.1.2 MPEG2 Time Stamp Calculation on Receive

Receiving packets with time stamps works similarly to the transmit process. When a packet with a time stamp is received, the time stamp is captured and compared to the current cycle timer value. The time stamp determines when ceLynx releases the packet data to the application.

If receive aging is enabled, the received packet is flushed from the FIFO if its time stamp value has expired. The time stamp used for aging, is the received time stamp plus a time stamp offset.

4.2.2 Time Stamp on Transmit to 1394 − DV Data

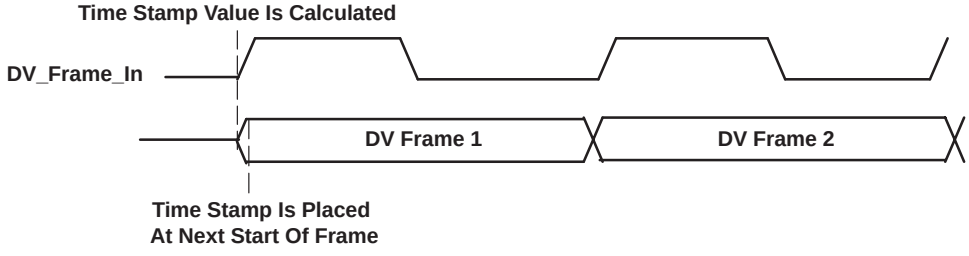


Figure 4−5. DV Transmit Timing

In Figure 4−5 the DV_Frame_In (programmable at GPIO) is used to create the time stamp for a DV packet. The signal should be 29.97 Hz for NTSC and 25 Hz for PAL, 50% duty cycle. The cycle timer is recorded at the time the DV_frame_In signal goes active. The value of the time stamp defined in IEC61883-2 is determined from the recorded value of the cycle timer register and transmit offset. The time stamp is then added to the next start of frame packet transmitted.

The DV_frame_In signal should be close to the start of a new frame or the transmit offset must be large enough to compensate for the delay.

The time stamp is calculated by adding an offset to the value of the cycle timer register. This offset is programmed in DB(N) CFG2 register. The 16 bit time stamp value is placed in the SYT field of the CIP header. The least significant 12 bits after the addition of cycle timer register and DB(N) CFG register is *lowadd*. The four most significant bits after the addition is *highadd*.

The time stamp can be placed in the first data packet of the frame (empty or full) or in the first full data packet of the frame. This is controlled by the TXDP(N) CFG register.

The cycle timer register is made up of the cycle count (4 most significant bits) and the cycle offset (12 least significant bits). The cycle-offset portion of the cycle timer register is modulo 3072. Each time this counter wraps around it signals the beginning of a new isochronous cycle. For a cycle master device, a cycle start packet is transmitted at the beginning of each new isochronous cycle. For a non-cycle master device a cycle start is decoded from a received cycle start packet.

Highadd specifies the offset in number of isochronous cycles, and lowadd specifies an offset into an isochronous cycle. If the computation results in a lowadd which is less than 3072 (125 μs) then the resultant time stamp is simply highadd and lowadd. If the computation results in a lowadd which is equal to or greater than 3072 then the resultant time stamp is highadd + 1 and the difference between the computed lowadd and 3072.

Time Stamp = highadd, lowadd : lowadd < 3072;
= (highadd + 1), (lowadd − 3072) : lowadd ≥ 3072;

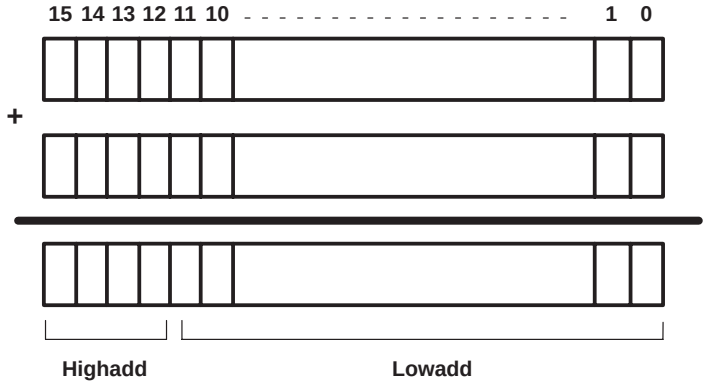


Figure 4−6. Determination of Highadd and Lowadd

If lowadd <3072, then the time stamp is simply highadd and lowadd:

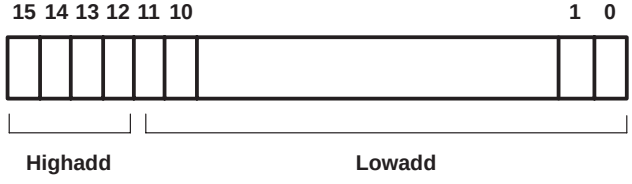


Figure 4−7. Time Stamp Value for Lowadd < 3072

If lowadd is equal to or greater than 3072 then the resultant time stamp is highadd + 1 and the difference between the computed lowadd and 3072.

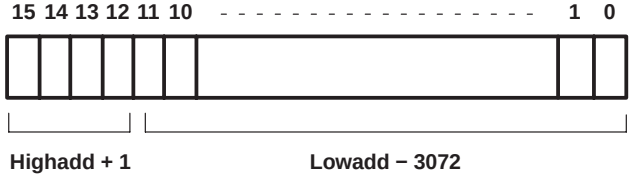


Figure 4−8. Time Stamp Value for Lowadd ≥ 3072

4.2.3 Time Stamp Determination on Receive − DV Data

When receiving a DV stream, the DV_Frame_Out toggles when the most recently received time stamp of the packet is equal to the current cycle timer. The DV_Frame_Out frequency is half of the original DV_Frame_In signal on transmit.

The DV data is released to the application as soon as it is received. Its release time is not dependent on the time stamp value. The time stamp based release and time stamp functions again are not valid for DV data.

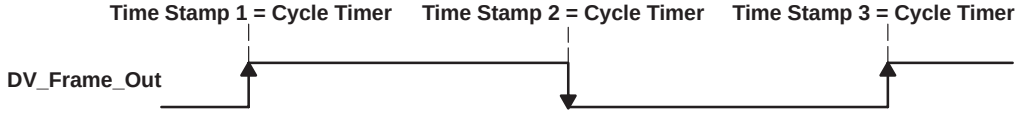


Figure 4−9. DV Transmit Timing

The time stamp is extracted from the SYT field of the CIP headers of the first source packet of a frame. An additional receive offset, which is programmable in CFR, is added to the time stamp value. Figure 4−10 shows how the time stamp is computed on receive. Lowadd is computed by adding as shown in the figure. Highadd is computed by adding also. The resultant time stamp is the concatenation of lowadd and highadd. The resulting time computation is used to signal the reception of a frame at regular intervals DV_Frame_Out.

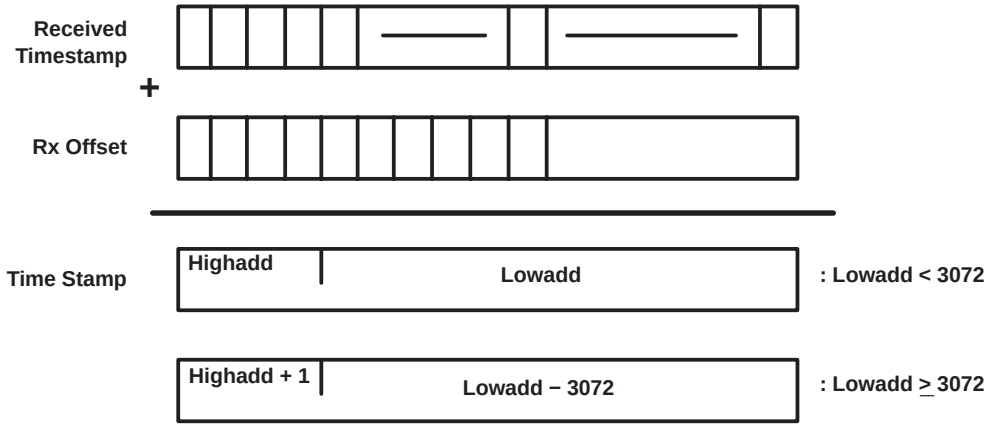


Figure 4−10. Time Stamp Calculation DV Data Received

4.3 ceLynx Interrupt Structure

ceLynx has several levels of interrupts for use by the host processor and application software. The interrupts can be programmed to output on the external $\overline{\text{INT}}$ terminal. Programming the interrupt mask registers determines which interrupts are output to the external $\overline{\text{INT}}$ terminal.

Should an $\overline{\text{INT}}$ event occur, the application software should read the SYSINT register first to determine which interrupt register was triggered. Then the application software should read and clear the specific interrupt register.

Table 4−3. Interrupt Enables and Descriptions

INTERRUPT REGISTER	INTERRUPT REGISTER ENABLE	DESCRIPTION
Reg 0x014h SYSINT	Reg 0x014h SYSINT	Gives visibility over all ceLynx interrupts. This register should be used to determine which interrupt register has triggered the external INT pin.
Reg 0x044h LINT	Reg 0x048h LINTEN	1394 bus interrupts
Reg 0x88h HSDIAINT	Reg 0x08Ch HSDIAINTEN	Interrupts for the HSDIA port
Reg 0x0C8h HSDIBINT	Reg 0x0CCh HSDIBINTEN	Interrupts for the HSDIB port
Reg 0x14Ch DBINT0	Reg 0x150h DBINT0EN	Interrupts 0 for data buffers
Reg 0x154h DBINT1	Reg 0x158h DBINT1EN	Interrupts 1 for data buffers
Reg 0x248h TXDPINT	Reg 0x24Ch TXDPINTEN	Interrupts for the transmit data path for all buffers
Reg 0x348h RXDPINT	Reg 0x34Ch RXDPINTEN	Interrupts for the receive data path for all buffers

When setting up the interrupts, the application software has to enable the individual interrupt, as well as the interrupt register in the SYSINT register. Refer to Figure 4−11 for the interrupt hierarchy.

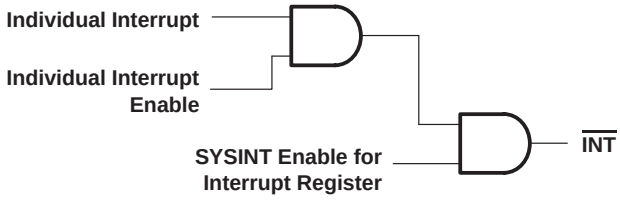


Figure 4−11. Interrupt Hierarchy

4.4 PID Filtering

ceLynx supports two PID (Program ID) filters for DirecTV™ or DVB data transmitted through the HSDI. Each filter, one per HSDI port, can filter on up to 16 PIDs each. The PID filters can only be used for DirecTV™ or DVB data transmitted with header and time stamp insert mode. The HSDI must be in single stream mode.

The PID filter only functions on transmit. The filter operation works as follows: If the input packet to the filter has a PID matching one of the 16 PID locations in the filter, then that packet passes through the filter and is written to the selected transmit buffer. All other packets do not pass through the filter.

Each PID filter has 16 possible values. The filter also has a mask register for masking the input word. The mask register masks the data before it is applied to the input of the filter. The filter ignores any bit that is masked. The first location that matches is used. If no match is found, the packet is ignored and data is not transferred to the transmit buffer.

4.4.1 PID Filtering Configuration Registers

Table 4−4. Configuration Registers for PID Filtering

CONFIGURATION REGISTERS		
REGISTER NAME	**BITS**	**FUNCTION**
PIDA_MASK PIDB_MASK	31:0	Determines which bits in the data stream PID field are used for comparison in the PID filter. A value of 1 indicates that bit is used by the PID filter. A setting of 0x0000 0000 means the PID filter ignores all bits of the PID field.
PIDA_ADDRFLTR1 PIDB_ADDRFLTR1		This register determines the buffer location of data streams that match the PID filter value.
	30:28	Buffer address for data streams that match a PID value programmed in filter location 7.
	26:24	Buffer address for data streams that match a PID value programmed in filter location 6.
	22:20	Buffer address for data streams that match a PID value programmed in filter location 5.
	18:16	Buffer address for data streams that match a PID value programmed in filter location 4.
	14:12	Buffer address for data streams that match a PID value programmed in filter location 3.
	10:8	Buffer address for data streams that match a PID value programmed in filter location 2.
	6:4	Buffer address for data streams that match a PID value programmed in filter location 1.
	2:0	Buffer address for data streams that match a PID value programmed in filter location 0.
PIDA_ADDRFLTR2 PIDB_ADDRFLTR2		This register determines the buffer location of data streams that match the PID filter value.
	30:28	Buffer address for data streams that match a PID value programmed in filter location 15.
	26:24	Buffer address for data streams that match a PID value programmed in filter location 14.
	22:20	Buffer address for data streams that match a PID value programmed in filter location 13.
	18:16	Buffer address for data streams that match a PID value programmed in filter location 12.
	14:12	Buffer address for data streams that match a PID value programmed in filter location 11.
	10:8	Buffer address for data streams that match a PID value programmed in filter location 10.
	6:4	Buffer address for data streams that match a PID value programmed in filter location 9.
	2:0	Buffer address for data streams that match a PID value programmed in filter location 8.
PIDA_FLTRACC PIDB_FLTRACC	31:0	PID filter access. Use this register to load 32-bit PID comparison values.
PIDA_CSR PIDB_CSR	1	PIDFLTR_RST Used to reset filter and pointer values.
	0	PIDFLTR_EN Enable for PID filter

NOTE: PIDA indicates HSDIA port.
PIDB indicates HSDIB port.

4.4.2 PID Filter Example

An MPEG2 transport stream containing PIDs 0x000, 0x001, 0x300, 0x301, 0x302, and 0x1FFF is transported from the application to the ceLynx HSDIA for transmission on the 1394 interface. The application needs to set up the ceLynx to transmit PIDs 0x000, 0x001, 0x301, and 0x302 only. Only packets with these PIDs are transmitted over 1394.

Step 1: Set up the PID filter mask for HSDIA. For the MPEG2 transport stream in this example, the PID is located in bits 20−8 of the first four bytes of MPEG2 data. A value of 1 in the PID filter mask register indicates which bits are used for the compare.

Register 0x090 PIDA_MASK = 0000 0000 0001 1111 1111 1111 0000 0000 = 0x001F FF00

Bit 20

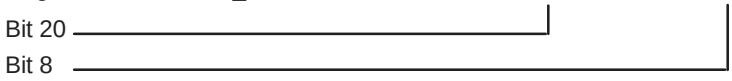
Bit 8

Step 2: Set the comparison values for the internal compare logic. The bits indicated by the mask register are compared with these values. If there is a match, the packet is transmitted. If there is no match, the packet is discarded.

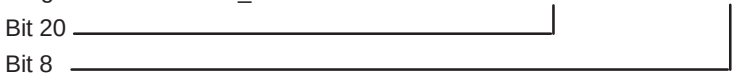
The application software can program up to 16 different values for PID compare. The software sets these PID compare values by writing to the PIDA_FLTRACC register (address offset 0x09C.) All 16 PID compare values must be used. If the application filters on less then 16 PID values, then the unused PID values should be filled in using the last PID value.

For this example, the first write to the PIDA_FLTRACC register sets PID filter location 0. The second write sets PID filter location 1, etc.

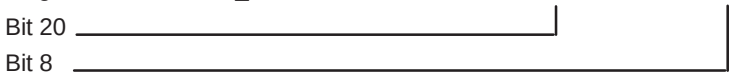
For PID filter location 0 – for PID = 0x000.
Register 0x09C PIDA_FLTRACC = 0000 0000 0000 0000 0000 0000 0000 0000 = 0x0000 0000



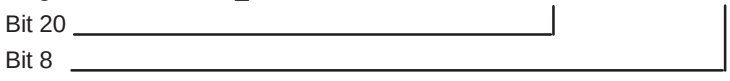
For PID filter location 1 – for PID = 0x001.
Register 0x09C PIDA_FLTRACC = 0000 0000 0000 0000 0000 0001 0000 0000 = 0x0000 0100



For PID filter location 2 – for PID = 0x301.
Register 0x09C PIDA_FLTRACC = 0000 0000 0000 0011 0000 0001 0000 0000 = 0x0003 0100

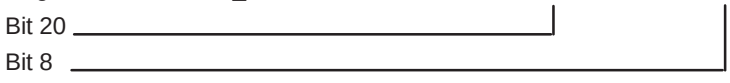


For PID filter location 3 – for PID = 0x302.
Register 0x09C PIDA_FLTRACC = 0000 0000 0000 0011 0000 0010 0000 0000 = 0x0003 0200



Because all 16 PID filter locations must be used, the software should set PID filter locations 4−16 to the last valid PID Filter value.

For PID filter location 4 through 15 for PID = 0x302.
Register 0x09C PIDA_FLTRACC = 0000 0000 0000 0011 0000 0010 0000 0000 = 0x0003 0200



Step 3: Assign buffers for each PID filter value.

In this example, packets with PID 300 or 301 are routed to buffer 0. Packets with PID 0 or 1 are routed to buffer 3. The buffer addressing is programmed in register 0x094: PIDA_ADDRFLTR1.

Register 0x094 PIDA_ADDRFLTR1 = 0000 0000 0000 0000 0000 0000 0011 0011
Register 0x084 PIDA_ADDRFLTR2 = 0000 0000 0000 0000 0000 0000 0000 0000

Step 4: Enable the PID filter. The filter is enabled in register 0x0A0 PIDA_CSR, bit 0. Once the PID filter is enabled, the application software can not write any values to the PIDA_FLTRACC register.

4.5 Isochronous Packet Insertion, Transmit Only

This feature has been included in ceLynx specifically to support modification of the PAT and PMT packets of the MPEG2 standard ISO/IEC 13818-1.

4.5.1 Functional Overview

ceLynx supports packet insertion into a sparse MPEG2 transport stream. A sparse MPEG2 stream is defined as a stream that contains gaps between some packets, and the gaps are larger than a single packet. There are two memory areas dedicated to packet insertion. The insertion buffers are a maximum of 188 bytes in length. These buffers are accessible via the microcontroller interface. Each buffer is dedicated to one HSDI.

ceLynx supports transmission of two independent MPEG2 transport streams. To minimize the complexity of the insertion buffer logic, the HSDI must be configured in fixed buffer mode. As a result of these requirements, no more than one transport stream, either DVB or DirecTV, can be input into each HSDI when the packet insertion logic is enabled. Supporting packet insertion for two independent MPEG2 transport steams requires that each HSDI be dedicated to one transport stream.

Both insertion buffers are write accessible via the microprocessor interface. Each insertion buffer has an address counter. Upon *system reset or power up* the address counter of each buffer is set to 0x0. The insertion buffers are written as follows:

1. The microcontroller writes a word to the insertion buffer address.
2. The data is written directly to the insertion buffer at the address pointed to by the address counter.
3. The address counter is incremented.

Once *n* words are written to an insertion buffer, the packet is enabled for transport by setting the insertion buffer enable bit. The setting of the enable bit is performed by software. The packet is inserted into the stream at the next available packet gap. Once an insertion buffer has its ENABLE bit set, all writes to that buffer are ignored.

If the number of *n* words is less than the insertion buffer size for a DVB stream, then the AUTOFILL function can be used. When AUTOFILL is set, the remainder of the packetsize-n words are written to 0xFFFFFFFF. The packet size for each insertion buffer is determined by DB(N)CFG0.STREAMTYPE.

Once a packet has been enabled for insertion into a transport stream, the hardware inserts the packet in the next available gap. Packets are inserted in the HSDI as if the data were coming in through the HSDI. When the HSDI is inactive (i.e., no data is being clocked in and the last packet has been completed) the insertion packet begins to be input into the system. The insertion packet is time-stamped just as a packet would be coming in through the HSDI. An insertion packet does not pass through the PID filter.

If a packet begins to enter the HSDI before the insertion packet has been completely input, the part of the insertion packet that has been written to the TX buffer is flushed and the pointers are reset. The incoming packet is accepted. The incoming packet is not delayed in any way. An aborted insertion attempt does not cause an interrupt. During the next available gap another attempt is made to insert the packet. This continues until the insertion buffer is disabled by software or the packet is successfully inserted into the buffer.

If the buffer overflows when the insertion packet is inserted, the part of the insertion packet that has been written to the TX buffer is flushed and the pointers are reset. An aborted insertion attempt does not cause an interrupt.

Once a packet has been inserted into the transport stream the microcontroller is interrupted. The packet insertion logic is then disabled. The software must re-enable the insertion buffer to insert another packet.

4.5.2 Packet Insertion Configuration Registers

NOTE:
A indicates HSDIA port. *B* indicates HSDIB port.

Table 4−5. Configuration Registers for Packet Insertion

CONFIGURATION REGISTERS		
REGISTER NAME	**BITS**	**FUNCTION**
INSBUFA_ACC INSBUFB_ACC	31:0	Access to insertion buffer. The microcontroller can only write the insertion packet to the insertion buffer when the packet insertion feature is disabled.
INSBUFA_CSR0 INSBUFB_CSR0	30	WRPTR_RST resets the packet insertion buffer write pointer to 0. Only valid when packet insertion feature is disabled.
	29:24	WRPTR indicates the pointer value of the next write access to INSBUFA_ACC. Only valid when packet insertion feature is disabled
	22	RDPTR_RST resets the packet insertion buffer read pointer to 0. Only valid when packet insertion feature is disabled
	21:16	RDPTR indicates the next location that will be returned by a read access to INSBUFA_ACC. Only valid when packet insertion feature is disabled
	10:8	INSRT_BUF indicates to which of the 8 data buffers the packet insertion buffer is mapped.
	7	AUTOFILL − all locations in the insertion buffer starting from INSBUFA_WRPTR are filled with 0xFFFF.
	6	PKTINSRT_EN enables the packet insertion feature.
	5:0	PKTSIZE indicates size of insertion packet.
INSBUFA_CSR1 INSBUFB_CSR1	15:0	OFPT is used to calculate the time stamp for inserted packets. The format of this register follows the 16 LSBs of the 1394 cycle timer register.

4.5.3 Packet Insertion Example

A transport stream is transmitted using ceLynx HSDIA port. ceLynx is configured to filter PID values of 0 out of the transport stream. The application must replace the information contained in PID 0 in the stream transmitted over 1394.

The application can create a packet to replace the PID 0 packet that was filtered from the transport stream. The application writes the packet to the ceLynx insertion buffer, and the ceLynx inserts this packet into the next available gap in the transport stream. These gaps are usually created by the PID filtering function or by the application not providing data at the interface.

Step 1: Ensure the packet insertion bit is disabled. This bit is located in INSBUFx_CSRO.PKTINSRT_EN.

Step 2: Set up packet insertion size. These bits are located in INBUFx_CSR0.PKTSIZE. For MPEG2-DVB, these bits are set to 2F, which is the number of quadlets in hex value.

Step 3: Specify into which stream the empty packets will be inserted. This is accomplished by programming the buffer of the selected stream in INSBUFx_CSR0.INSRT_BUF.

Step 4: Set offset packet time value. This time is programmable in INSBUFx_CSR1.

The offset packet time can be thought of as the amount of time allotted for one cell at the HSDI pins. For example, data is being streamed uniformly into the HSDI:

From the time cell A begins until cell B begins is the amount of time required by the system to transport cell A. This value is the offset packet time (OFPT) for an inserted packet. If a gap greater or equal to the OFPT value exists in the transport stream, then ceLynx inserts the packet.

The OFPT value is a 16-bit value that has the same format as the lower 16 bits of the 1394 link layer CYCLE_TIME register. The upper 4 bits represent the number of whole 125 μs 1394 cycles it takes to transport one MPEG2 cell, and the lower 12 bits represent the number of 25 ns clock cycles in the additional fraction of a cycle.

For instance, if the time from the beginning of cell A at the HSDI to the beginning of cell B at the HSDI is 140 μs, the OFPT value would be:

Upper 4 bits = (1 x 125 μs) = 0x1
Lower 12 bits = (15000 ns/40 ns) = 600 clock cycles = 0x258
OFPT = 0x1258

Step 5: Write the inserted packet to the insertion buffer. The external host can access the insertion buffer through the INSBUFx_ACC register. The host should write all quadlets to this register. If the application does not have enough data to fill the insertion buffer, it can use the INSBUFx_CSR0.AUTOFILL bit to fill the rest of the insertion buffer locations with FFh.

Step 6: Enable the insertion buffer. This control bit is located in INSBUFx_CSR0.PKTINSRT_EN. Once the bit is set to 1, ceLynx inserts the packet into the next available gap, as specified by OFPT. The INSBUFx_CSR0.PKTINSRT_EN bit is cleared by hardware after the packet is inserted.

5 ceLynx Data Formats

The data formats for transmission and reception of data are shown in the following sections. The transmit format describes the expected organization of data presented to ceLynx at the MCIF or HSDIx interface. The receive formats describe the data format that ceLynx presents to the MCIF or the HSDIx interface.

5.1 Asynchronous Transmit

Asynchronous transmit refers to the use of any of the configurable partitions in the 8-Kbyte data buffer. These buffers can be accessed by the HSDIx or the MCIF. There are two basic formats for transmitted asynchronous data. The first is for quadlet packets, and the second is for block packets.

The MCIF can access the data buffers through registers DB(N)ACC0 and DB(N)ACC1. All quadlets except the last must be written to DB(N)ACC0. The last quadlet must be written to DB(N)ACC1. The application can also transmit asynchronous data through the HSDI. The application must read out an entire packet from the same buffer using a single interface.

ceLynx can automatically provide the asynchronous 1394 transmit headers on packets transmitted through the data buffer (ee Note). In this case, the application must only supply the raw asynchronous data to the data buffer. The microcontroller can program the headers through the TXDP(N)H0−TXDP(N)H3 registers for the associated buffers. The format of these registers must match the formats described in Figure 5−2 and Figure 5−3.

NOTE:

Acknowledges for packets transmitted are received in the ACK tracking buffer. See Section 5−3, *Asynchronous Acknowledge Buffer*, for more information.

ceLynx can only automatically insert asynchronous transmit headers for packets with payload data. These include tCodes listed in Table 5−2.

If ceLynx does not supply the headers, the application must include the headers with the data before transmit. In this case, the application must supply all of the headers and data in the formats described in Figure 5−2 and Figure 5−3.

Table 5−1. Asynchronous Transmit Header Insert†

ASYNCHRONOUS TRANSMIT HEADERS†	REGISTERS USED FOR HEADER INSERT	DEFAULT ASYNCHRONOUS TRANSMIT VALUES
Speed/tLabel/rt/tCode/priority	TXDP(N)H0	0000 0000
Destination ID/Destination OffsetHi	TXDP(N)H1	0000 0000
Destination OffsetLow	TXDP(N)H2	0000 0000
Data Length/extended tcode (for block packets)	TXDP(N)H3	0000 0000

† See Figure 5−1, Figure 5−2, Figure 5−3, and Figure 5−4 for exact header format.

Table 5−2. tCodes Supported for Asynchronous Automatic Header Insertion

tCode	MEANING
0	Write request for data quadlet
1	Write request for data block
6	Read response for data quadlet
7	Read response for data block
9	Lock request

5.1.1 Quadlet Transmit

The quadlet-transmit format is shown in Figure 5−1 and Figure 5−2, and is described in Table 5−3. The first quadlet contains packet information. The second and third quadlets contain the 64-bit, quadlet-aligned address. The fourth quadlet is data used only for write requests and read responses. For read requests and write responses, the quadlet data field is omitted.

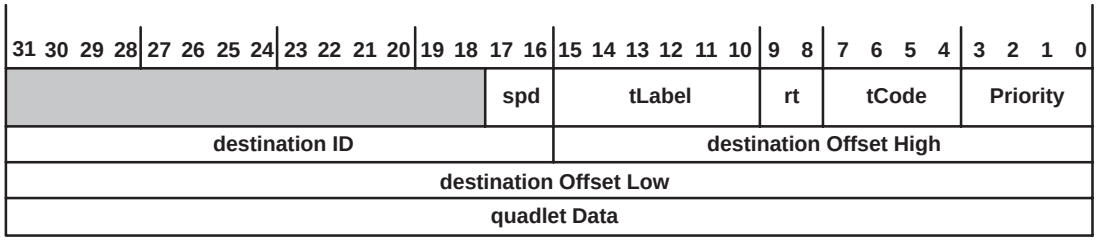


Figure 5−1. Quadlet Transmit Format (Write Request)

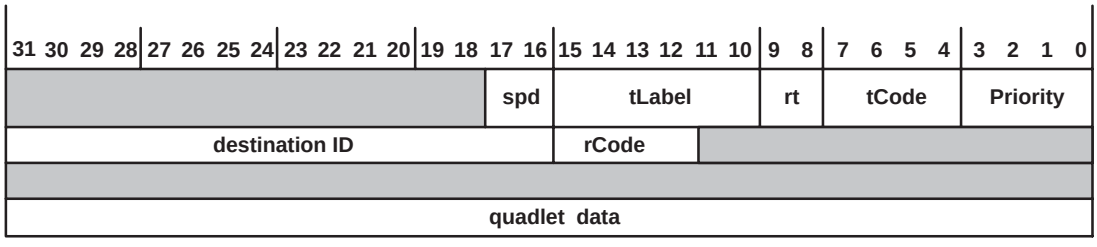


Figure 5−2. Quadlet Transmit Format (Read Response)

Table 5−3. Quadlet Transmit Format Functions

FIELD NAME	DESCRIPTION
spd	The spd field indicates the speed at which the current packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s. For this implementation, 11 is undefined.
tLabel	The tLabel field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This field is used to pair up a response packet with its corresponding request packet.
rt	The rt field is the retry code for the current packet: 00 = new, 01 = retry_X, 10 = retry_A, and 11 = retry_B.
tCode	The tCode field is the transaction code for the current packet (see Table 6−10 of IEEE–1394 standard).
priority	The priority field contains the priority level for the current packet. For cable implementation, the value of the bits must be zero (for backplane implementation, see clauses 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard).
destinationID	The destinationID field is the concatenation of the 10-bit bus number and the 6-bit node number that forms the destination node address of the current packet.
destination OffsetHigh, destination OffsetLow	The concatenation of these two fields addresses a quadlet in the destination node address space. This address must be quadlet aligned (modulo 4).
quadlet data	For write requests and read responses, the quadlet data field holds the data to be transferred. For write responses and read requests, this field is not used and should not be written into the FIFO.

Table 5−3. Quadlet Transmit Format Functions (Continued)

FIELD NAME	DESCRIPTION		
rcode	Specifies the result of the read request transaction. The response codes that can be returned to the requesting agent are defined as follows:		
	Response Code	Name	Description
	0	resp_complete	Node successfully completed requested operation
	1−3	reserved	
	4	resp_conflict_error	Resource conflict detected by responding agent. Request can be retried.
	5	resp_data_error	Hardware error. Data not available.
	6	resp_type_error	Field within request packet header contains unsupported or invalid value.
	7	resp_address_error	Address location within specified node not accessible
	8−Fh	reserved	

5.1.2 Block Transmit

The block-transmit format is shown in Figure 5−3 and is described in Table 5−4. The first quadlet contains packet information. The second and third quadlets contain the 64-bit address. The first 16 bits of the fourth quadlet contains the dataLength field. This is the number of bytes of data in the packet. The remaining 16 bits represent the extended_tCode field (see Table 6−11 of the IEEE-1394 standard for more information on extended_tCodes). The block data, if any, follows the extended_tCode.

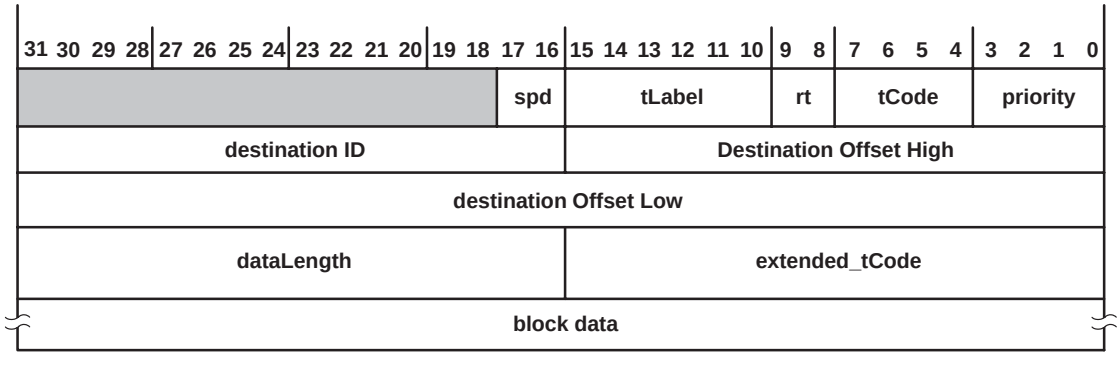


Figure 5−3. Block Transmit Format (Write Request)

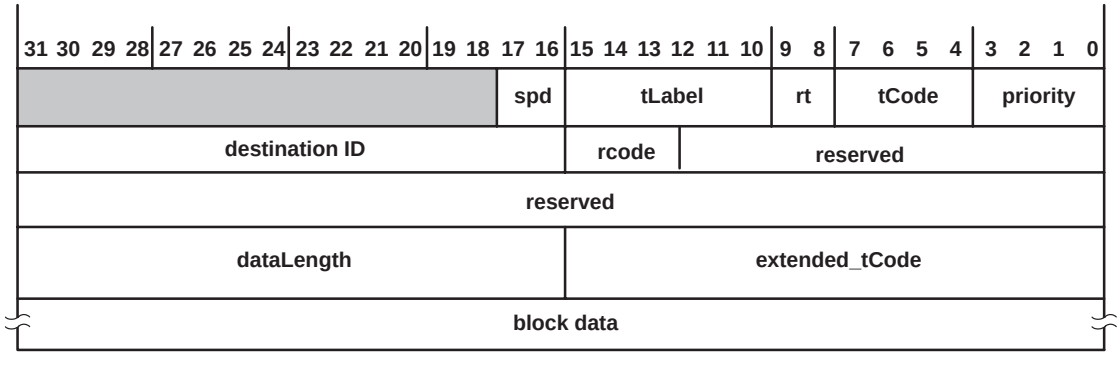


Figure 5−4. Block Transmit Format (Read Response)

Table 5−4. Block Transmit Format Functions

FIELD NAME	DESCRIPTION
spd	The spd field indicates the speed at which the current packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s. For this implementation, 11 is undefined.
tLabel	The tLabel field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This field is used to pair up a response packet with its corresponding request packet.
rt	The rt field is the retry code for the current packet is 00 = new, 01 = retry_X, 10 = retry_A, and 11 = retry_B.
tCode	tCode is the transaction code for the current packet (see Table 6−10 of IEEE-1394 standard).
priority	The priority level for the current packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clauses 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
destinationID	The destinationID field is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which the current packet is being sent.
destination OffsetHigh, destination OffsetLow	The concatenation of the destination OffsetHigh and the destination OffsetLow fields addresses a quadlet in the destination node address space. This address must be quadlet aligned (modulo 4). The upper 4 bits of the destination OffsetHigh field are used as the response code for lock-response packets and the remaining bits are reserved.
dataLength	The dataLength field contains the number of bytes of data to be transmitted in the packet.
extended_tCode	The block extended_tCode to be performed on the data in the current packet (see Table 6−11 of the IEEE-1394 standard)
block data	The block data field contains the data to be sent. If dataLength is 0, no data should be written into the FIFO for this field. Regardless of the destination or source alignment of the data, the first byte of the block must appear in byte 0 of the first quadlet.

5.2 Asynchronous Receive

There are two basic formats for received asynchronous data. The first is for quadlet packets, and the second is for block packets. The asynchronous receive data buffer can be accessed by either the HSDI or the MCIF. The data buffers can be accessed by the MCIF through the DB(N)ACC0 register.

The full received packet format with headers and data is shown in Figure 5−5 and Figure 5−6. ceLynx can strip received packet headers on a quadlet basis. This is controlled in the RXDPB(N)CFG0 register bits 0−3. For example, the application can choose to strip quadlet headers 0, 1, and 2. The application receives header 3 and the data. In this example, if ceLynx received an asynchronous block read response packet, the application receives the dataLength and extended t-code quadlet and the packet data only.

The packet control token gives information about the received packet. For asynchronous packets, the quadlet is included with the data in the data buffer according to the RXDPB(N)CFG0.INSERTPKT TOKEN bit. The control token is always attached to receive self-ID packets regardless of the RXDPB(N)CFG0.INSERTPKTTOKEN setting. The packet control token format for asynchronous and PHY packets is shown in Figure 5−5 and Table 5−5.

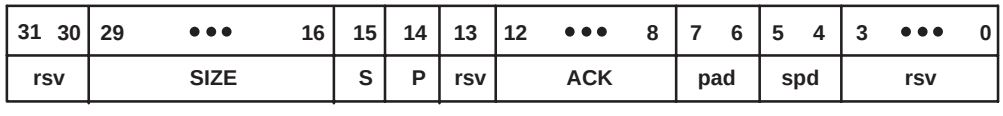


Figure 5−5. Packet Control Token Format for Asynchronous, Self-ID, and PHY Packets

Table 5−5. Bit Description for Packet Control Token

BIT NAME	DESCRIPTION
Size	Size of the packet in quadlets
S	This bit is set when the token is attached to a self-ID packet.
P	This bit is set when the token is attached to a PHY packet.
rsv	Reserved
ACK	ACK code from the link receiver (5 bits). ACK code meanings are explained in Table 5−10.
pad	Number of bytes padded (e.g. data_length = 9 → pad = 3)
spd	Speed code of the received packet

The default configuration for ceLynx is receive asynchronous data through buffer 5. The self-ID packets and PHY configuration packets are received through buffer 6. These configurations can be changed in the STREAMTYPE bits in the DB(N)CFG0 registers.

The asynchronous receive control bits are located in register RXDP(N)CFG1. These bits are active only when the associated buffer is configured and enabled for asynchronous receive. Table 5−6 includes information on asynchronous receive control. There are four general categories for asynchronous receive control: nonbroadcast asynchronous, broadcast asynchronous, self-IDs, and PHY packets. Any combination of control bits can be used for a selected buffer, *except* broadcast and nonbroadcast packets cannot be received in the same buffer with a fixed configuration.

The receive asynchronous packet is steered to the lowest numbered buffer whose requirements are satisfied.

Table 5−6. Asynchronous Receive Control

CONTROL BIT	ASYNCHRONOUS PACKET RECEIVED
BROADCAST	If set, then *only* broadcast packets are received by the selected buffer. This includes packets with 3FF destination ID only.
RCVPHYPKT	If set, then PHY packets are received by the selected buffer. This control bit can be used in conjunction with any of the other control bits.
RCVSELFID	If set, then self-ID packets are received to the selected buffer. This control bit can be used in conjunction with any of the other control bits.
RCVALLADDR	If set, then all nonbroadcast asynchronous packets addressed to this node are received by the selected buffer regardless of the 48-bit serial bus address contained in the asynchronous packet header. This does not include PHY packets, self-ID packets, or broadcast packets.
INITMEMLO	Destination address: bus, node, 00000, 0000000 → bus, node, 7FFFF, FFFFFFF If set, then all asynchronous packets addressed to lower half of initial space of IEEE 1394-1995 are received by the selected buffer. This only includes packets with destination address between (bus, node, 00000,0000000 → bus, node, 7FFFF, FFFFFFF). This does not include PHY packets, self-ID packets, or broadcast packets.
INITMEMHI	Destination address: bus, node, 80000, 0000000 → bus, node, FFFFD, FFFFFFF If set, then all asynchronous packets addressed to upper half of initial space of IEEE 1394-1995 are received to the selected buffer. This only includes packets with destination address between (bus, node, 80000, 0000000 → bus, node, FFFFD, FFFFFFF). This does not include PHY packets, self-ID packets, or broadcast packets.
PRIVATE	Destination address: bus, node, FFFFE, 0000000 → bus, node, FFFFE, FFFFFFF If set, then all asynchronous packets addressed to private memory space specified by IEEE 1394-1995 are received by the selected buffer. This only includes packets with destination address between (bus, node, FFFFE, 0000000 → bus, node, FFFFE, FFFFFFF). This does not include PHY packets, self-ID packets, or broadcast packets.

Table 5−6. Asynchronous Receive Control (Continued)

CONTROL BIT	ASYNCHRONOUS PACKET RECEIVED
CSR	Destination address: bus, node, FFFFF, F000000 → bus, node, FFFFF, F0001FF If set, then all asynchronous packets addressed to CSR space specified by IEEE 1212.r and 1394−1995 are received by the selected buffer. This only includes packets with destination address between (bus, node, FFFFF, 00001FF → bus, node, FFFFF, F0003FF). This does not include PHY packets, self-ID packets, or broadcast packets.
SERBUS	Destination address: bus, node, FFFFF, F000200 → bus, node, FFFFF, F0003FF If set, then all asynchronous packets addressed to serial bus space specified by IEEE 1212.r and 1394−1995 are received by the selected buffer. This only includes packets with destination address between (bus, node, FFFFF, 0000200 → bus, node, FFFFF, F0003FF). This does not include PHY packets, self-ID packets, or broadcast packets.
ROM	Destination address: bus, node, FFFFF, F000400 → bus, node, FFFFF, F0007FF If set, then all asynchronous packets addressed to configuration ROM space specified by IEEE 1394−1995 are received by the selected buffer. This only includes packets with destination address between (bus, node, FFFFF, F000400 → bus, node, FFFFF, F0007FF). This does not include PHY packets, self-ID packets, or broadcast packets.
INITUNIT	Destination address: bus, node, FFFFF, F000800 → bus, node, FFFFF, FFFFFFF If set, then all asynchronous packets addressed to initial unit space specified by IEEE 1394−1995 are received by the selected buffer. This only includes packets with destination address between (bus, node, FFFFF, F000800 → bus, node, FFFFF, FFFFFFF). This does not include PHY packets, self-ID packets, or broadcast packets.

In addition to the asynchronous control bits listed in Table 5−6, the RXDPB(N)CFG2 and RXDPB(N)CFG3 registers allow the ceLynx to receive packets with selected values of the source ID, header 0 values, or data length. The application must program the selected value in the RXDPB(N)CFG2 and RXDPB(N)CFG3 registers. For example, to receive only asynchronous packets with source ID 1, the application would program the SRCIDMSK bits (bits 31:16) to 0xFFFF. A 1 in the SRCIDMSK field indicates that bit is compared with the SRCIDFLTR value. The SRCIDFLTR bits (bits 15:0) program the compare value. In this example, the application only wants to receive source ID 1. The setting for bits 15:0 would be 0x0001.

Table 5−7. Asynchronous Receive Header Strip

ASYNCHRONOUS RECEIVE HEADERS†	REGISTERS USED FOR HEADER STRIP
Asynchronous packet control token	RXDPB(N)CFG0.INSERTPKTTOKEN (Packet control token is included if INSERTPKTTOKEN = 1)
Destination ID/tLabel/retry code/tCode/priority	RXDPB(N)CFG0.STRIPHDR0
Source ID/Destination offset high	RXDPB(N)CFG0.STRIPHDR1
DestinationOffsetLow	RXDPB(N)CFG0.STRIPHDR2
DataLength/ Extended tCode (if block packet)	RXDPB(N)CFG0.STRIPHDR3

† See Figure 5−6 for exact header format.

5.2.1 Quadlet Receive

The quadlet-receive format is shown in Figure 5−6 and is described in Table 5−8. The first quadlet contains the packet-control token that is added by ceLynx. The first 16 bits of the second quadlet contain the destination node and bus ID, and the remaining 16 bits contain packet information. The first 16 bits of the third quadlet contain the node and bus ID of the source, and the remaining 16 bits of the third quadlet and the fourth quadlet contain the 48-bit, quadlet-aligned destination offset address. The last quadlet contains data that is used by write requests and read responses. For read requests and write responses, the quadlet data field is omitted.

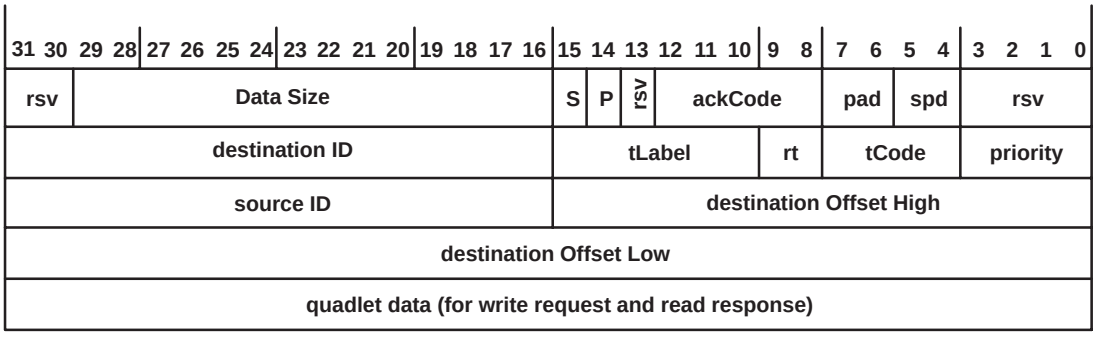


Figure 5−6. Quadlet − Receive Format

Table 5−8. Quadlet − Receive Format Functions

FIELD NAME	DESCRIPTION
Data Size	Packet control token − Size of the packet in quadlets
S	Packet control token - This bit is set to 1 whenever the packet control token is attached to a self-ID packet.
P	Packet control token - This bit is set to 1 whenever the packet control token is attached to a PHY packet.
ackCode	Packet control token - This 5-bit field holds the acknowledge code sent by the receiver for the current packet. See Table 5−10 for ACK codes.
pad	Packet control token - Number of padding bytes added
spd	Packet control token - The spd field indicates the speed at which the current packet was sent. 00 = 100 Mbits/s, 01 = 200 Mbits/s, 10 = 400 Mbits/s, and 11 is undefined for this implementation.
destination ID	The destinationID field contains the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which the current packet is being sent.
tLabel	The tLabel field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This field is used to pair up a response packet with its corresponding request packet.
rt	The rt field is the retry code for the current packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	The tCode field is the transaction code for the current packet (see Table 6−10 of the IEEE-1394 standard).
priority	The priority field contains the priority level for the current packet. For cable implementation, the value of the bits must be zero (for backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard).
source ID	The sourceID field contains the node ID of the sender of the current packet.
destination Offset High, destination Offset Low	The concatenation of the destination OffsetHigh and the destination OffsetLow fields addresses a quadlet in the destination nodes address space. This address must be quadlet aligned (modulo 4). (The upper four bits of the destination OffsetHigh field are used as the response code for lock-response packets, and the remaining bits are reserved.)
quadlet data	For write requests and read responses, the quadlet data field holds the transferred data. For write responses and read requests, this field is not present.

5.2.2 Block Receive

The block-receive format through the data buffer is shown in Figure 5−6 and is described in Table 5−9.The first quadlet contains the packet control token which is added by ceLynx. The first 16 bits of the second quadlet contain the node and bus ID of the source node, and the last 16 bits of the second quadlet and all of the third quadlet contain the 48-bit, quadlet-aligned destination offset address. All remaining quadlets, except for the last one, contain data that is used only for write requests and read responses. For block read requests and block write responses, the data field is omitted.

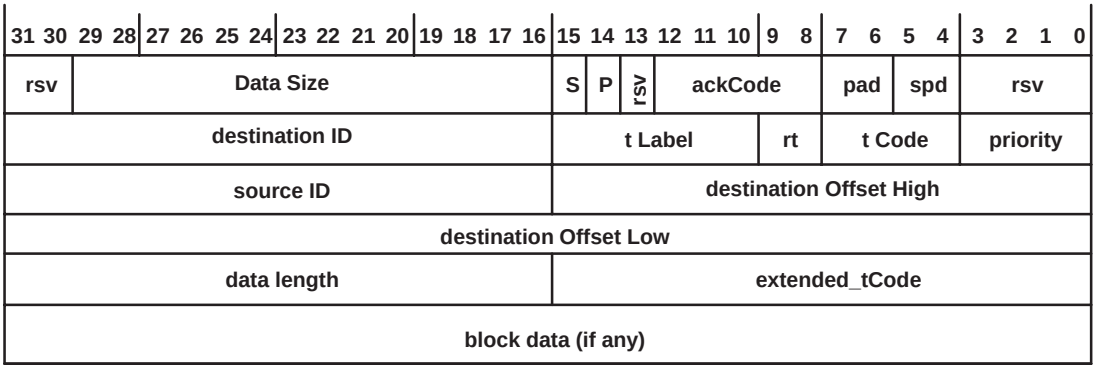


Figure 5−7. Block Receive Format

Table 5−9. Block Receive Format Functions

FIELD NAME	DESCRIPTION
S	Packet control token - This bit is set to 1 whenever the packet control token is attached to a self-ID packet.
Data Size	Packet control token - Size of the packet in quadlets
P	Packet control token - This bit is set to 1 whenever the packet control token is attached to a PHY packet.
ackCode	Packet control token - This 5-bit field holds the acknowledge code sent by the receiver for the current packet. See Table 5−10 for ACK codes.
pad	Packet control token - Number of padding bytes added
spd	Packet control token - The spd field indicates the speed at which the current packet was sent. 00 = 100 Mbits/s, 01 =200 Mbits/s, 10 = 400 Mbits/s, and 11 is undefined for this implementation.
destination ID	The destinationID field is the concatenation of the 10–bit bus number and the 6-bit node number that forms the node address to which the current packet is being sent.
tLabel	The tLabel field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This field is used to pair up a response packet with its corresponding request packet.
rt	The rt field contains the retry code for the current packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	The tCode field is the transaction code for the current packet (see Table 6−10 of the IEEE-1394 standard).
priority	The priority field contains the priority level for the current packet. For cable implementation, the value of the bits must be zero (for backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard).
source ID	The sourceID field contains the node ID of the sender of the current packet.

Table 5−9. Block − Receive Format Functions (Continued)

FIELD NAME	DESCRIPTION
destination OffsetHigh, destination OffsetLow	The concatenation of the destination OffsetHigh and the destination OffsetLow fields addresses a quadlet in the destination nodes address space. This address must be quadlet aligned (modulo 4). The upper 4 bits of the destination OffsetHigh field are used as the response code for lock-response packets and the remaining bits are reserved.
dataLength	For write request, read responses, and locks, the dataLength field indicates the number of bytes being transferred. For read requests, the dataLength field indicates the number of bytes of data to be read. A write-response packet does not use this field. Note that the number of bytes does not include the head, only the bytes of block data.
extended_tCode	The extended_tCode field contains the block extended_tCode to be performed on the data in the current packet (see Table 6−11 of the IEEE–1394 standard).
block data	The block data field contains any data being transferred for the current packet. Regardless of the destination address or memory alignment, the first byte of the data appears in byte 0 of the first quadlet of this field. The last quadlet of the field is padded with zeros out to four bytes, if necessary.
spd	The spd field indicates the speed at which the current packet was sent. 00 = 100 Mb/s, 01 = 200 Mb/s, 10 = 400 Mb/s, and 11 is undefined for this implementation.

5.3 Asynchronous Acknowledge Buffer

The acknowledge buffer retains the last six acknowledges returned by external nodes in response to the last six async packets transmitted from the ceLynx. The host processor can track which acknowledge was returned for each of the last six asynchronous packets by accessing this buffer via the TXDPSTAT register.

The acknowledge tracking buffer contains a 32-bit quadlet for every asynchronous packet transmitted from the node. This quadlet contains information on the acknowledge received, the destination ID, the tlabel, retry code, tcode, and ack count for a transmitted packet.

The TXDPSTAT register (CFR 204h) also gives information on transmitted asynchronous packets. This register is updated after each full read from the TXDPSTAT register (upper and lower 16 bits). Bits 27:24 give the ACK code for the transmitted packet. The ACK codes are described in Table 5−10. This ACK code is from the receiving node if the asynchronous packet was transmitted correctly, or from the transmitter logic if an error occurred on transmission. An ACK_CODE_COMPLETE (0001b) is written to bits 27:24 for asynchronous stream packets or broadcast asynchronous packets. The fifth bit (bit 28), which is the first bit shown in Table 5−10, is the error bit.

Table 5−10. ACK Code Meanings

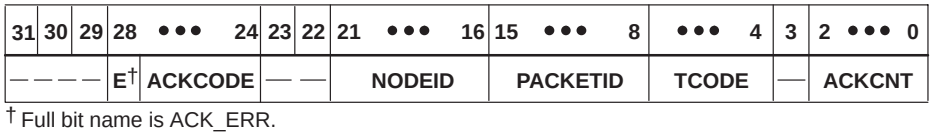
ERRORBIT_ACK CODE	MEANING	DESCRIPTION
0_0001	ACK_CODE_COMPLETE	The node has successfully accepted the packet. If the packet was a request subaction, the destination node has successfully completed the transaction, and no response subaction follows.
0_0010	ACK_CODE_PENDING	The node has successfully accepted the packet. If the packet was a request subaction, a response subaction will follow later. This code is not returned for a response subaction.
0_0100	ACK_CODE_BUSY_X	The packet could not be accepted. The destination transaction layer may accept the packet on a retry of the subaction.
0_0101	ACK_CODE_BUSY_A	The packet could not be accepted. The destination transaction layer will accept the packet when the node is not busy during the next occurrence of retry phase A.
0_0110	ACK_CODE_BUSY_B	The packet could not be accepted. The destination transaction layer will accept the packet when the node is not busy during the next occurrence of retry phase B.

Table 5−10. ACK Code Meanings (Continued)

ERRORBIT_ACK CODE	MEANING	DESCRIPTION
0_1011	ACK_CODE_BUSY_TARDY	The node could not accept the packet because the link and higher layers are in a suspended state. The destination node will restore full functionality to the link and transaction layers and may accept the packet on a retransmission in a subsequent fairness interval.
0_1100	ACK_CONFLICT_ERROR	A resource conflict prevented the packet from being accepted.
0_1101	ACK_CODE_DATA_ERROR	The node could not accept the block packet because the data field failed the CRC check or because the length of the data block payload did not match the length contained in the data_length field. This code is not returned for any packet that does not have a data block payload.
0_1110	ACK_TYPE_ERROR	A field in the request packet header was set to a n unsupported or incorrect value, or an invalid transaction was attempted (e.g., a write to a read-only address).
0_1111	ACK_ADDRESS_ERROR	The node could not accept the packet because the destination_offset field in the request was set to an address not accessible in the destination node.
1_0000	EVT_MISSING_ACK	This is caused when a subaction gap was detected before an ACK arrived.
1_0001	EVT_TCODE_ERR	This is caused when a bad tCode is associated with this packet. If buffer flush is enabled in TXDP CFR, then the associated TX buffer is flushed.
1_0010	EVT_PKT_FORMAT_ERROR	This is caused by the ceLynx hardware when the transmit packet has an incorrect format.
1_0011	EVT_UNKNOWN	This is caused when an error condition has occurred that cannot be represented by any other event codes defined herein.
1_0100	EVT_BUSY_ACK_RETRY_ EXHAUSTED	Not supported

TXDPSTAT bits 15:8 give information on the packet identifier. For asynchronous packets, this is the tlabel and retry code for the transmitted asynchronous packet. For asynchronous stream packets, this is the isochronous tag and channel number. In general, bits 15:8 in TXDPSTAT correspond to bits 15:8 of the first quadlet of a transmitted packet.

The count value indicates how many acknowledges are present in the buffer. The ACKCNT field starts at zero and increments (to a max value of six), with each acknowledge that is loaded into this buffer. A read from an empty buffer returns all zeroes. The buffer can hold up to 6 quadlets. Once the buffer is full, or more than six asynchronous transmits have occurred without a single read from the buffer, no more writes occur to the stack. In this case, it is presumed the host is not concerned with tracking the ACKs returned.



† Full bit name is ACK_ERR.

Figure 5−8. Acknowledge Buffer Format

Table 5−11. Acknowledge Buffer Bit Descriptions for Asynchronous Packets

BIT NAME	DESCRIPTION
ACK_ERR	Acknowledge error
ACKCODE	Acknowledge code (See Table 5−10)
NODEID	1. destination_ID 2. Not valid for asynchronous streaming
PACKETID	1. tlabel and retry code for async 2. Tag and channel for asynchronous streaming
TCODE	tCode
ACKCNT	Number of ACKs available

The returned acknowledge is always appended with a bit that indicates the validity of the acknowledge that was received. This is the ACK_ERR bit shown in Figure 5−8. For the case where no acknowledge was returned or the ACK could not be verified, the ERR bit is set to a 1 and the 4-bit acknowledge field should be interpreted as indicated in Table 5−10. Note that the count field still increments in this case just as if an acknowledge had been received correctly.

Busy retries (ACK codes 4, 5, and 6) should only be loaded into the buffer if the automatic busy retry limit has timed out. Otherwise the buffer could overflow with busy retries while waiting for a node to respond. If an ACK code other than a busy retry is received during the automatic retry, then this ACK is loaded into the buffer as normal.

5.4 Asynchronous Streams

ceLynx can be configured to send asynchronous streams. These are isochronous packets sent during the asynchronous period. It is described in the 1394.a standard.

An asynchronous stream packet has a transaction code of 0xA. It is subject to the same arbitration requirements. Asynchronous stream packets can be routed to the appropriate buffer based on data length or header 0 (isochronous header) information.

5.4.1 Asynchronous Stream Transmit

Asynchronous streams should only be transmitted from the host port using header insertion mode.

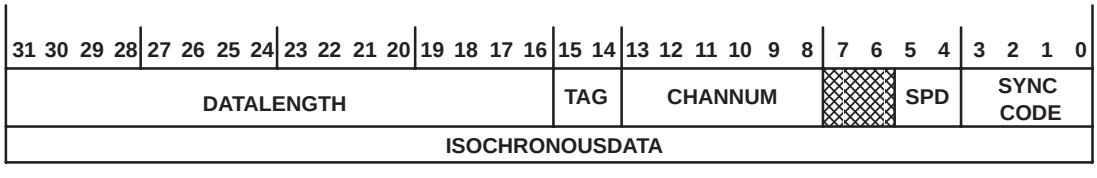


Figure 5−9. Asynchronous Stream Transmit Format

Table 5−12. Asynchronous Stream Transmit Functions

FIELD NAME	DESCRIPTION
DATALENGTH	The DATALENGTH field indicates the number of bytes in the current packet.
TAG	The TAG field indicates the format of data carried by the isochronous packet (00 = unformatted, 01 – 11 are reserved).
CHANNUM	The CHANNUM field carries the channel number with which the current data is associated.
SPD	The speed code of the current packet: 00=100 mbits/s, 01=200 mbits/s, 10=400 mbits/s
SYNC CODE	The SYNC CODE field carries the transaction layer-specific synchronization bits.
ISOCHRONOUSDATA	The ISOCHRONOUSDATA field contains the data to be sent with the current packet. The first byte of data must appear in byte 0 of the first quadlet of this field. If the last quadlet does not contain four bytes of data, the unused bytes should be padded with zeros.

5.4.2 Asynchronous Stream Receive

Asynchronous stream packets are received at buffers with streamtype defined as asynchronous stream.

The packet control token gives information about the received packet. For asynchronous stream packets, this quadlet is included with the data in the data buffer according to the RXDPB(N)CFG0.INSERTPKTTOKEN bit. The packet control token format for asynchronous stream packets is shown in Figure 5−5.

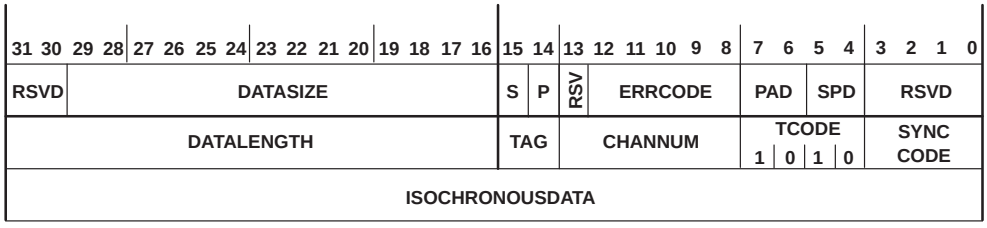


Figure 5−10. Asynchronous Stream Receive Format

Table 5−13. Asynchronous Stream Receive Functions

FIELD NAME	DESCRIPTION
RSVD	Reserved
DATASIZE	Packet control token - Size of the packet in quadlets
S	Packet control token - This bit is set to 1 whenever the packet control token is attached to a self-ID packet.
P	Packet control token - This bit is set to 1 whenever the packet control token is attached to a PHY packet.
RSVD	Reserved
ERRCODE	Packet control token - This 5-bit field holds the error code. 0_0001 corresponds to complete. 0_1101 corresponds to a data error.
PAD	Packet control token - Number of padding bytes added.
SPD	Packet control token - The spd field indicates the speed at which the current packet was sent. 00 = 100 Mbits/s, 01 = 200 Mbits/s, 10 = 400 Mbits/s, and 11 is undefined for this implementation.
RSVD	Reserved
DATALENGTH	The dataLength field indicates the number of bytes in the current packet.
TAG	The TAG field indicates the format of data carried by isochronous packet (00 = unformatted, 01 − 11 are reserved).
CHANNUM	The CHANNUM field contains the channel number with which this data is associated.
TCODE	The TCODE field carries the transaction code for the current packet (TCODE = 0xA).
SYNC CODE	The SYNC CODE field carries the transaction layer-specific synchronization bits.
ISOCHRONOUSDATA	The packet data

5.5 Isochronous Data

ceLynx can be configured to transmit and receive several different types of isochronous data. These include MPEG2 data, DirecTV data, and DV data.

The ceLynx can be configured to insert all isochronous transmit headers automatically, including headers for MPEG2 and DV. In this case, only the raw isochronous data should be supplied to the HSDI or MCIF. The header insertion is controlled in the TXDP(N)CFG registers for the associated data buffer. The microcontroller can program the header values in the TXDP(N)H0−TXDP(N)H4 registers for the associated data buffer. For example, for MPEG2 data, the ceLynx can automatically insert the 1394 isochronous

headers, CIP0, CIP1, and time stamps. The microcontroller should program the header registers according to the formats discussed in Section 5.5.1.

5.5.1 MPEG2 DVB Data

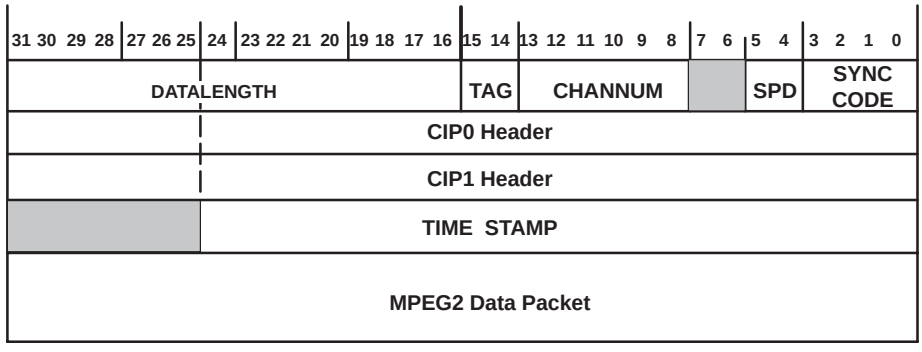


Figure 5−11. MPEG2 Transmit Format

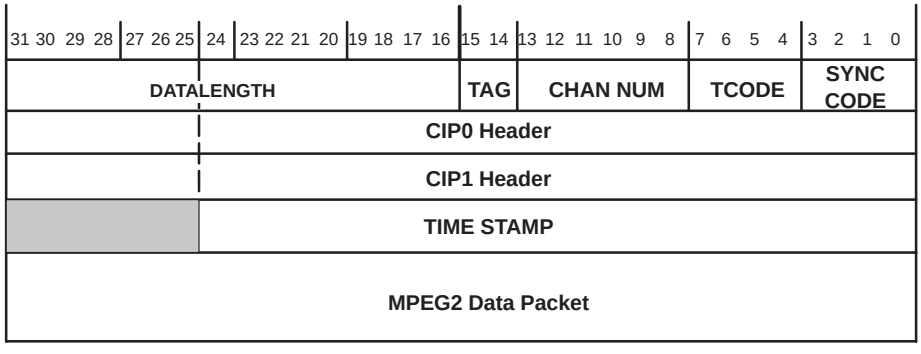


Figure 5−12. MPEG2 Receive Format

Table 5−14. Isochronous−Transmit Functions

FIELD NAME	DESCRIPTION
DATALENGTH	The DATALENGTH field indicates the number of bytes in the current packet.
TAG	The TAG field indicates the format of data carried by the isochronous packet (01 = formatted according to IEC61883)
CHANNUM	The CHANNUM field carries the channel number with which the current data is associated.
TCODE	The transaction code for the current packet (TCODE=Ah).
SPD	Speed code for transmit. 00 = S100, 01 = S200, 10 = S400
SYNC CODE	The SYNC CODE field carries the transaction layer-specific synchronization bits.
MPEG2 Data	The MPEG2 Data field contains the data to be sent with the current packet (includes CIP0, CIP1, and TIME STAMP.

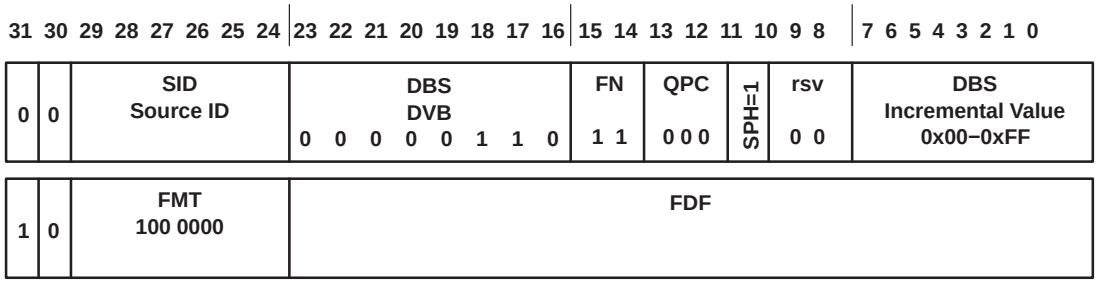


Figure 5−13. Isochronous CIP Headers – MPEG2 Data

5.5.1.1 MPEG2 Transmit

For MPEG2 transmit, ceLynx can be configured to include any of the three 1394 MPEG2 headers. The TXDP(N)CFG.HIM control bit automatically inserts the necessary headers as specified by DB(N)CFG0.STREAMTYPE.

MPEG2 TRANSMIT PACKET HEADERS	REGISTERS USED TO INSERT HEADERS	DEFAULT VALUES FOR MPEG2 TX
ISO HEADER	TXDP(N)H0	0008 4010
CIP0	TXDP(N)H1	0006 C400
CIP1	TXDP(N)H2	A000 0000
TIME STAMP	DB(N)CFG0.TSINSERT	—

The ceLynx has default settings for the MPEG2 transmit CIP headers for buffer 0. The application must set the header registers for MPEG2 transmit for buffers other than buffer 0.

NOTE:

The application must supply quadlet-aligned data in MPEG2 transmit mode. ceLynx does not add padding bits.

The host can access the data buffer through register DB(N)ACC0 for the associated buffer. The host should write the last quadlet of the transmitted packet to the DB(N)ACC1 for the associated buffer.

The ceLynx hardware dynamically updates the CIP headers with the correct values during transmission. In normal operation, there is no need for the user to set the CIP header values using the host processor and the TXDP (N) CFG.VHWEN bit. The TXDP (N) CFG.VHWEN bit should only be used in test or debug situations.

The size of the MPEG2 packet is determined by the MPEG2 class size. The class size is set in TXDP(N)CFG.MXC for the associated buffer. The class sizes correspond to the values in Table 5−15.

Table 5−15. MPEG2 DVB Transmit Bandwidth Classes

CLASS MXC VALUES	MAX TSP B/W (Mbps)	MAX SP B/W (Mbps)	MAX 1394 BW (Mbps)	POSSIBLE MPEG2 – DVB 1394 PACKET SIZE, BYTES (Decimal)
0	1.504	1.536	2.816	20, 44
1	3.008	3.072	4.352	20, 68
2	6.016	6.144	7.424	20, 116
3	12.032	12.288	13.568	20, 212
4	24.064	24.576	25.856	20, 212, 404
5	36.096	36.864	38.144	20, 212, 404, 596
6	48.128	49.152	50.432	20, 212, 404, 596, 788
7	60.160	61.440	62.270	20, 212, 404, 596, 788, 980

TSP BW: Transport stream package bandwidth, based on 188-byte MPEG2 cell
SP BW: Source packet bandwidth. Based on 192-byte MPEG2 cell
1394 BW: Overall BW on 1394 bus. Based on 212-byte MPEG2 packet.

5.5.1.2 MPEG2 Receive

ceLynx can be formatted to strip any of the 1394 isochronous or CIP headers from received packets before data is stored in the data buffer. The ceLynx can be programmed to strip the time stamp off the packet before storing in the data buffer, or to keep the time stamp with the data. The time stamp is stripped when DB(N)CFG0.TSSTRIP is set to 1. This control bit can only be used if the ISO and CIP headers are also removed. The time stamps can also be used to determine when the data is released to the application by using the TSAGE and TSRelease bits. (See *Internal Functions*, Section 4, for more detail.)

Table 5−16. MPEG2 Receive Header Stripping

MPEG2 RECEIVE PACKET HEADERS	REGISTERS SETTINGS USED TO STRIP HEADERS
ISO HEADER	RXDPB(N)CFG0.STRIPHDR0
CIP0	RXDPB(N)CFG0.STRIPHDR1
CIP1	RXDPB(N)CFG0.STRIPHDR2
TIME STAMP	DB(N)CFG0.TSSTRIP

NOTE:

The RXDPB(N)CFG3 and RXDPB(N)CFG4 registers allow ceLynx to filter incoming packets. ceLynx can receive packets based on source ID, data length, or header 0 information. The MASK bits allow the filter to mask off bits of the incoming packet.

The packet control token should not be included with received MPEG2 data.

Either the host or HSDI can access the data buffer. The host can access the data buffer through register DB(N)ACC0 for the associated buffer.

5.5.2 DirecTV Data

ceLynx supports both 130 byte and 140 byte DirecTV data. For DirecTV 140-byte data, ceLynx expects the application to add the 10-byte header before sending the data to ceLynx for transmit. For DirecTV 130-byte data, ceLynx automatically adds the 10-byte header to the 130-byte packet before transmitting over 1394. The 10-byte header can be programmed using internal ceLynx CFRs.

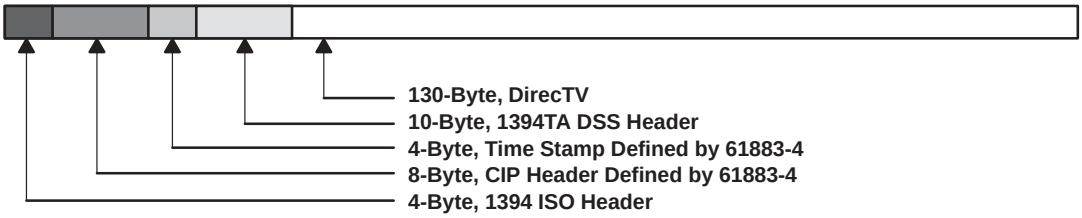


Figure 5−14. 1394 DirecTV Packet

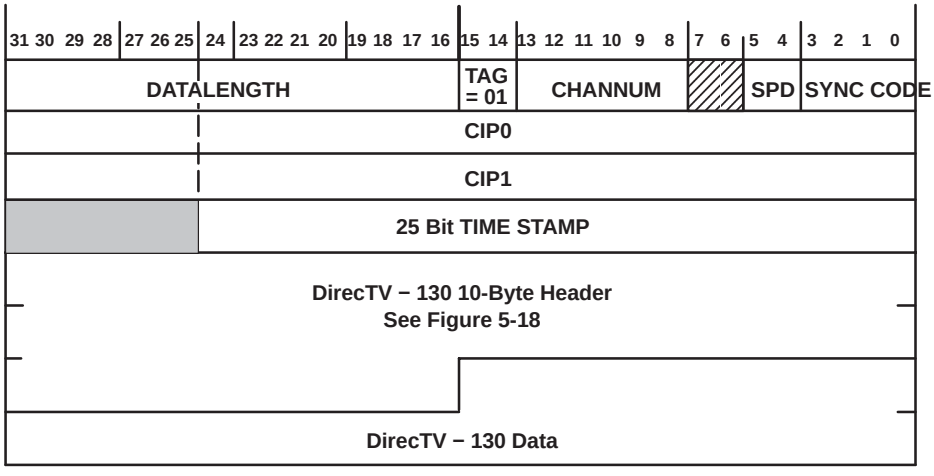


Figure 5−15. DirecTV Transmit Format

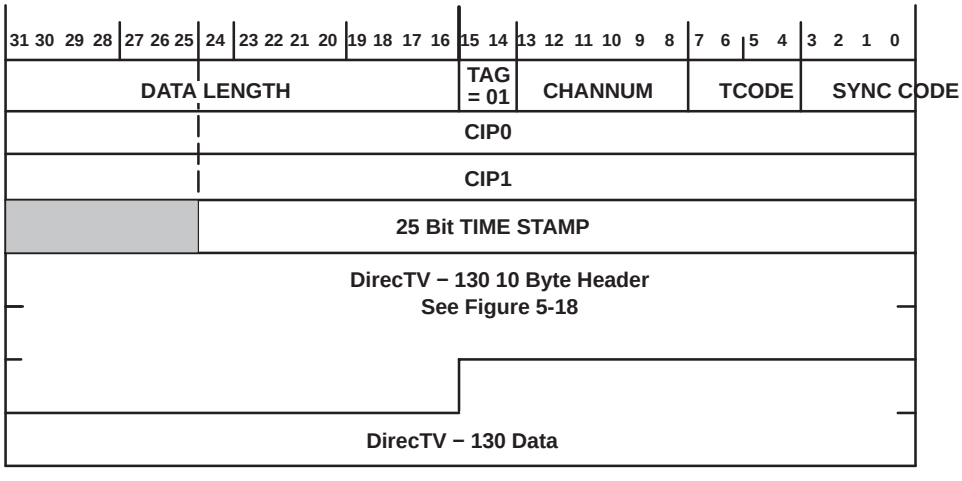


Figure 5−16. DirecTV Receive Format

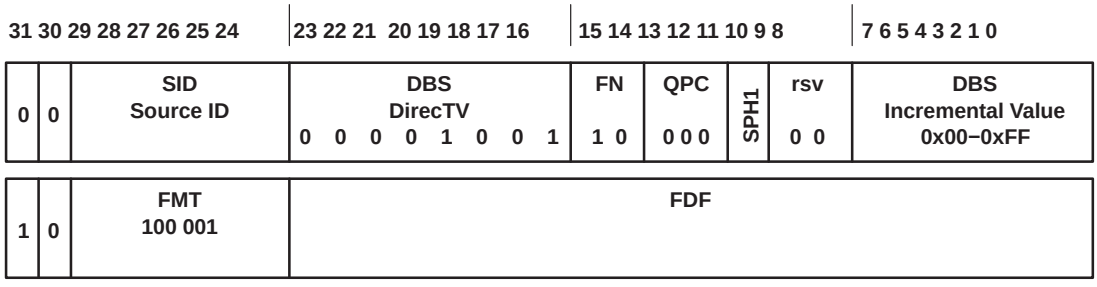


Figure 5−17. Isochronous CIP Headers – DirecTV Data

The 10-byte DirecTV header included for the DirecTV 130-byte packet is defined by the 1394 Trade Association. If enabled, the hardware can insert the system clock count and EF fields. The system clock count is derived internally by the hardware from an external 27-MHz clock is supplied on the GPIO pins. The entire 10-byte header format is shown in Figure 5−18. The first and second words of the header are programmable via a CFR.

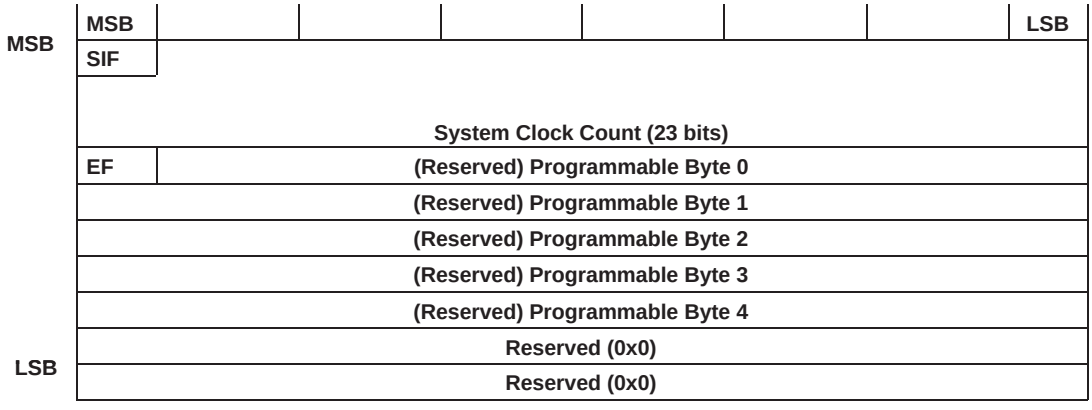


Figure 5−18. DirecTV 130 10-Byte Header

NAME	SIZE BITS	DESCRIPTION
SIF	1	System clock invalid flag, indicates that the system clock count is invalid.
System Clock Count	23	23-bit time stamp from a 23-bit counter driven by an external 27-MHz clock.
EF	1	Error flag, indicates that there is an error in the transport packet.

System Clock Invalid Flag:
The ceLynx automatically adds the system clock count in the hardware. As a result there should be no time when the system clock invalid flag (SIF) bit would be 1 indicating an invalid time stamp. This bit is programmable by software, but hardware does not infer the value of this bit at any time.

System Clock Count:
The system clock count is a 27-MHz clock time stamp. It is 23 bits long and is implemented as a 23-bit counter running on an external 27-MHz clock. The 27-MHz clock is input on a multiplexed GPIO pin.

Error Flag:
The error flag (EF) indicates that ceLynx has detected an error in the packet. This error indication is an input into ceLynx in the 130-byte mode. The signal is valid on the first byte of the packet. For each packet, EF reflects the value of this input signal on the first byte of the packet. This signal is input on a multiplexed GPIO pin.

5.5.2.1 DirecTV Transmit

For DirecTV transmit, ceLynx can be configured to include any of the 1394 DirecTV headers. The TXDP(N)CFG.HIM control bit automatically inserts the necessary headers as specified by DB(N)CFG0.STREAMTYPE.

DirecTV TRANSMIT PACKET HEADERS	REGISTERS USED TO INSERT HEADERS	DEFAULT VALUES FOR DirecTV TX
ISO HEADER	TXDP(N)H0	0008 4010
CIP0	TXDP(N)H1	0009 C400
CIP1	TXDP(N)H2	A000 0000
TIME STAMP	DB(N)CFG0.TSINSERT	—
DirecTV 130_2	TXDP(N)H3	0000 0000

NOTE:
The application must supply quadlet-aligned data in the DirecTV 140-byte transmit mode. No padding bits are added. ceLynx can automatically add the 10-byte DirecTV header to DirecTV 130-byte data. ceLynx does not add the 10-byte DirecTV 130-byte header to packets transmitted through the host port. In this case, the application must supply 140 bytes to ceLynx for transmit.

The host can access the data buffer through registers DB(N)ACC0 and DB(N)ACC1 for the associated buffer. The host should write all transmit quadlets except the last to the DB(N)ACC0 register. The host should write the last transmit quadlet to the DB(N)ACC1 register.

The size of the DirecTV packet is determined by the DirecTV class size. The class size is set in TXDP(N)CFG.MXC for the associated buffer. The class sizes correspond to the values in Table 5−17.

Table 5−17. DirecTV Transmit Bandwidth Classes

CLASS MXC VALUES	MAX DirecTV 140-BYTE CELL B/W (Mbps)	MAX SP B/W (Mbps)	MAX 1394 BW (Mbps)	POSSIBLE MPEG2 – DirecTV 1394 PACKET SIZE, BYTES (Decimal)
0	N/A	N/A	N/A	N/A
1	2.24	2.304	3.584	20, 56
2	4.48	4.608	5.888	20, 92
3	8.96	9.216	10.486	20, 164
4	17.92	18.432	19.712	20, 164, 308
5	26.88	27.648	28.928	20, 164, 308, 452
6	35.84	36.864	38.144	20, 164, 308, 452, 596
7	44.80	46.08	47.360	20, 164, 308, 452, 596, 740

DirecTV 140 BW: Transport stream package bandwidth, based on 140-byte DirecTV cell
SP BW: Source packet bandwidth, based on 144-byte DirecTV cell.
1394 BW: Overall BW on 1394 bus, based on 164-byte DirecTV packet.

5.5.2.2 DirecTV Receive

ceLynx can be formatted to strip any of the 1394 isochronous or CIP headers from received packets before data is stored in the data buffer. ceLynx can be programmed to strip the time stamp off the packet before storing in the data buffer. The time stamp is stripped when DB(N)CFG0.TSSTRIP is set to 1. This control bit can be used only if the ISO and CIP headers are also removed.

Table 5−18. DirecTV Receive Header Stripping

DirecTV RECEIVE PACKET HEADERS	REGISTERS SETTINGS USED TO STRIP HEADERS
ISO HEADER	TXDPB(N)CFG0.STRIPHDR0
CIP0	TXDPB(N)CFG0.STRIPHDR1
CIP1	TXDPB(N)CFG0.STRIPHDR2
TIME STAMP	DB(N)CFG0.TSSTRIP
DirecTV 130_1	10-Byte DirecTV header is automatically stripped when DB(N)CFG0.STREAMTYPE is DirecTV 130-byte packet.

NOTE:

The RXDPB(N)CFG3 and RXDPB(N)CFG4 registers allow ceLynx to filter incoming packets. ceLynx can receive packets based on source ID, data length, or header 0 information. The MASK bits allow the filter to mask off bits of the incoming packet.

The packet control token should not be included with received DirecTV data.

Either the host or HSDI can access the data buffer. The host can access the data buffer through register DB(N)ACC0 for the associated buffer.

5.5.3 DV Data

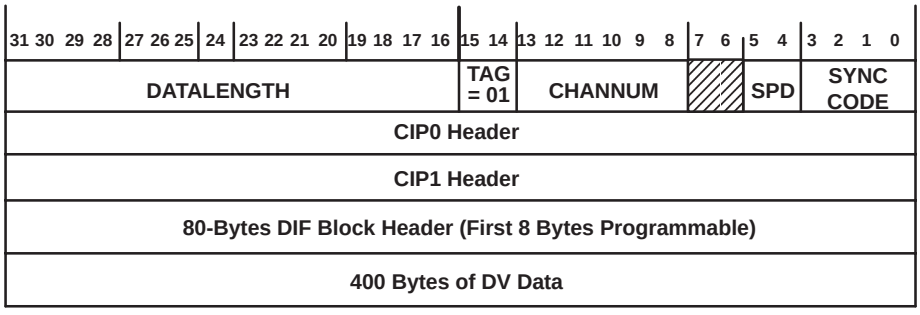


Figure 5−19. DV Transmit Format − DIF Sequence

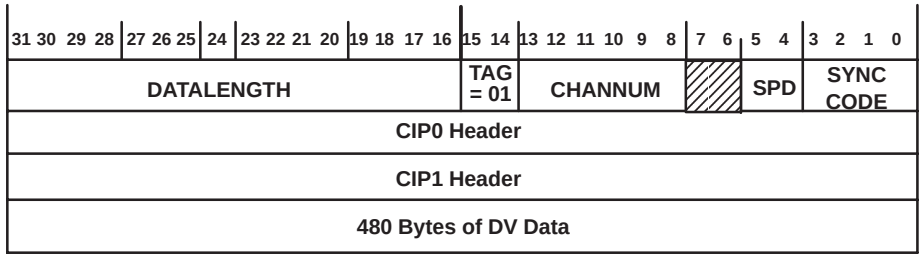


Figure 5−20. DV Transmit Data Packet

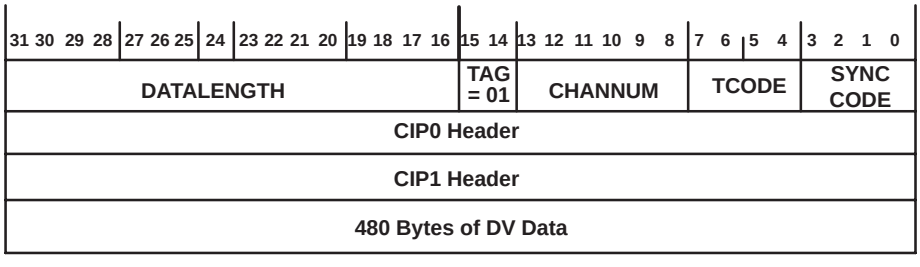


Figure 5−21. DV Receive Format

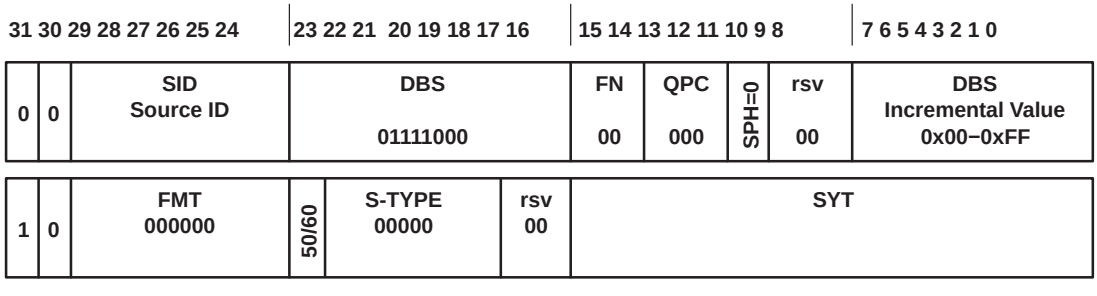


Figure 5−22. Isochronous CIP Headers − DV Data

The application can supply the H0 DIF block header with the DV data, or ceLynx can include the 80-byte H0 DIF block on DV transmit. For NTSC and PAL systems, this occurs every 25th packet. ceLynx allows the host port to program the value of the first eight bytes of the H0 DIF block header. These are available in the TXDP(N)H3 and TXDP(N)H4 headers in DV mode. (See Figure 5−23 for programming information.) By

default, the value of these registers is 0x0000 0000. All other bytes of the inserted H0 DIF block header are 0xFF.

ceLynx automatically increments the ID0 DIF sequence number when the H0 block is automatically inserted. This sequence number is updated with every new sequence. The sequence counter is incremented every 25th packet. It rolls over when it reaches its maximum count, which is 9 (NTSC) and 11 (PAL). The next frame begins with the ID0 counter at zero.

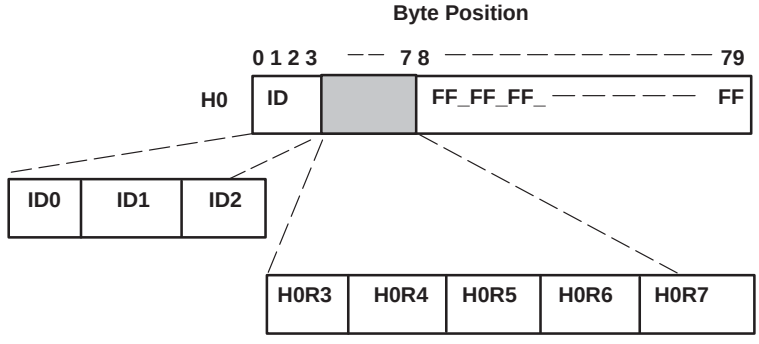


Figure 5−23. H0 DIF Block Header for DV Transmit

When transmitting DV data in the header0 insert mode, ceLynx is not capable of resetting the ID1 DIF sequence number to 0 when the source stops and resumes its data transmission in the middle of the frame. The DIF sequence number starts its counter from the value conserved when the data source stops. As a result, ceLynx inserts the time stamp where the DIF sequence is offset. Use the following steps to correctly transmit DV data in the header0 insert mode.

1. Source turned off within a frame.
2. Wait until the TX buffer signals an empty.
3. Reset the TXDP.
4. Resume data transmission with a new frame.

5.5.3.1 HDDV (61883−3)

ceLynx supports HDDV data in minimal form. ceLynx supports a $H_{0,0}$ and $H_{0,1}$ insertion mode. This mode is a simple derivative of the H_0 insertion mode. The H_0 data is inserted into both the $H_{0,0}$ and $H_{0,1}$ data locations. The customer has the option of disabling this feature.

ceLynx supports the extended data length as defined by 61883-3 for HD-DVCR data. Both PAL and NTSC systems are supported. Time stamping is supported as it is for the standard DV modes.

The burst DV algorithm is not supported for this data type. No hardware smoothing function inserts empty packets. Empty packets are only inserted when a complete packet is not available in the buffer.

ceLynx also supports H0 DIF block insertion for HD-DVCR format. It inserts a 160-byte H0 DIF block. The first eight bytes of the H0 DIF block can be programmed by the host port in internal registers TXDP(N)H3 and TXDP(N)H4. The rest of the 160-byte header are all 0xFF. The ID0 sequence number is also automatically incremented for every new sequence whenever ceLynx automatically inserts the H0 DIF block header.

HDDV has been verified in design simulation only.

5.5.3.2 DV Format (IEC 61883-2) Burst Input

A burst input is defined as an input method that is limited only by the fullness of the transmit buffer. This method is commonly used when the application level hardware or software does not know how fast to input

data into ceLynx. ceLynx is responsible for smoothing the incoming data so that the receive buffer, which has a depth much less than a frame, does not overflow. It is assumed that at the receive node data is read out of the receive buffer at a constant rate. The actual rate is determined by the frame frequency. The frame frequency is determined by a PLL driven by the DV_Frame_Out signal of ceLynx.

Specification 61883-2 defines that either a packet of data (480 bytes for NTSC) or an empty packet must be sent every ISO cycle. To reduce the speed at which data is sent to the receive buffer, empty packets are evenly distributed throughout the frame.

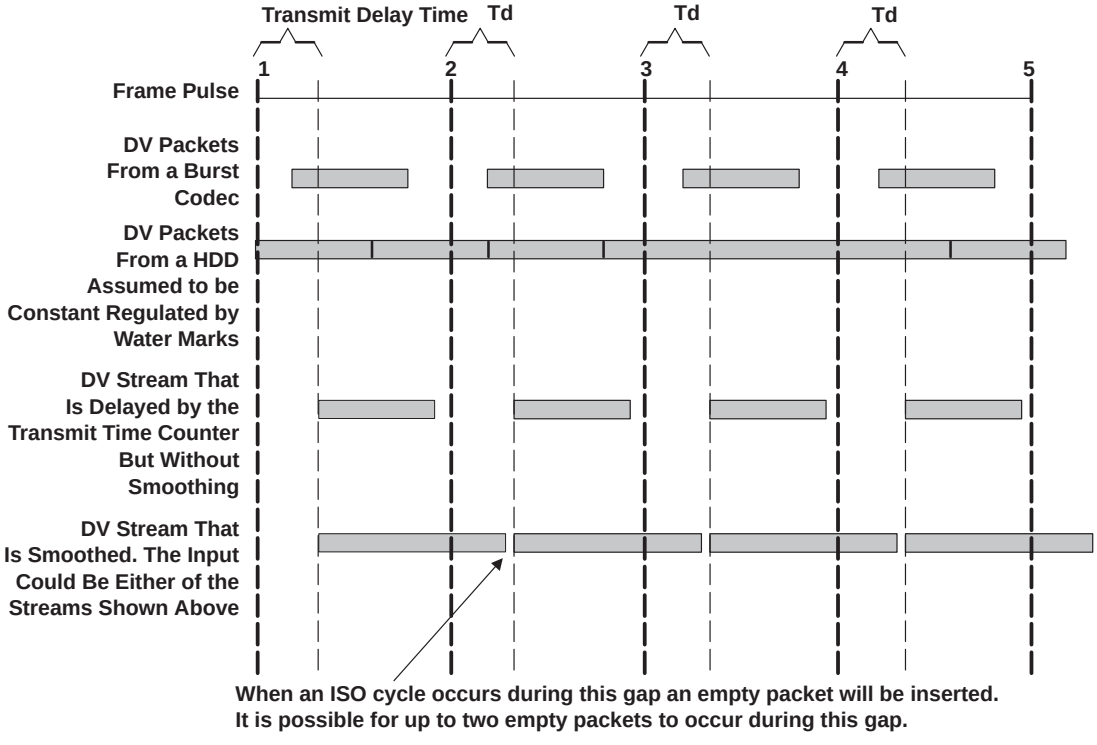


Figure 5−24. DV Smoothing

ceLynx determines the number of empty packets to insert automatically by counting the length of the DV frame. The DV frame is based on a 29.97 Hz clock which has a required accuracy of 1%. The DV frame can be as long as 33.704 ms and as short as 33.036 ms. The number of empty packets inserted into the stream can range from 14.2 to 19.6. Table 5−19 shows the relationship between the frame length and the number of insertion packets automatically insert into the stream. The extra empty packets are inserted during the transmit delay time as previously described.

Table 5−19. Automatic Empty Packets Relative to Frame Length, NTSC Only

MAX FRAME (μs)	MIN FRAME (μs)	AVERAGE NUMBER AUTOMATIC EMPTY PACKETS INSERTED
33700	33650	19
< 33650	33525	18
< 33525	33400	17
< 33400	33275	16

< 33275	33150	15
< 33150	33025	14

Table 5−20. Automatic Empty Packets Relative to Frame Length, PAL Only

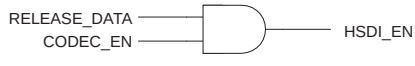
MAX FRAME (μs)	MIN FRAME (μs)	AVERAGE NUMBER AUTOMATIC EMPTY PACKETS INSERTED
40400	40275	22
<40275	40150	21
< 40150	40025	20
< 40025	39900	19
<39900	39775	18
<39775	39650	17
< 39650	39525	16

5.5.3.3 Detecting Start of Frame (Receive Path Only)

In DV mode, ceLynx does not receive any data into the buffer until it has identified the start of frame. The first packet of a frame is the start of frame. The start of frame is determined using the DIF block identification header.

5.5.3.4 Release Data Mode (HSDIxCFG0.ReleaseData)

ceLynx supports a mode where output to the HSDI on receive is controlled by a sequence. The application needs to implement the following sequence along with an external AND gate connected as shown.



RELEASE_DATA = software control bit

CODEC_EN = Enable signal from DV CODEC application

HSDI_EN = HSDI_EN input to ceLynx for HSDI write.

1. No data is being output from the HSDI, the system is at rest, no data is in the RX buffer. RELEASE_DATA = 0.
2. The first packet of a DV stream is received. The cell_AV signal goes active indicating data is available.
3. A packet is received with a valid time stamp. The frame_out goes active.
4. The application acitivates the frame_in and sets RELEASE_DATA = 1.
5. The HSDI_EN signal goes active and toggles with the CODEC_EN signal output.
6. When the buffer becomes empty and the cell_AV signal goes inactive, reset the sequence.

5.5.3.5 Stream Termination Recovery (Receive Mode)

Some systems terminate their DV stream on a nonframe boundary. ceLynx supports termination of a DV channel by interrupting the processor if the DIF sequence has a break or if any number other than 25 DIF blocks is received for a given DIF sequence. When this interrupt occurs the hardware stops receiving data until a start of frame is detected.

5.5.3.6 Receiving DV Headers Only Mode

The user can configure a buffer to receive H0 DV headers from every active DV channel on the 1394 bus.

When a buffer is in this mode, the H0 headers of all DV streams currently on the bus are received by the DV buffer. An H0 packet is defined as a DV packet with the DIF block number equal to 0. When this DIF block is received the following 6 quadlets of data are input into the buffer (packet control token, 1394 header, CIP0, CIP1, and first 8 bytes of H0). The packet control token is the first quadlet input into the buffer. The remaining quadlets are input into the buffer in the order they were received.

ceLynx continues to receive the DV headers in the buffer until the buffer overflows. Once the buffer overflows, no more data will be received by the buffer. If the application needs the latest header information, the software performs a buffer flush and reads the headers from the buffer using the host port.

5.5.3.7 Initial Packet Transmit Delay

The transmit buffer has a programmable amount of data before sending out the first DV packet. This feature is controlled by the VxDV_THMODE and VxDV_THSEL bits in the transmit data path CFRs. X indicates HSDIA or HSDIB. VxDV_THMODE turns on the feature. VxDV_THSEL allows the application to choose the data offset value.

5.5.3.8 Receiving DV Headers for Enabled DV Channel

ceLynx supports a buffer configuration that allows the user to receive DV data in one buffer while receiving the headers and packet token for that same data in another buffer. ceLynx saves the packet token, 1394 header, CIP headers, and the first two quadlets of the H0 header for the single stream that is being received.

Two buffers should be set up for DV receive. The data packet is received in the higher numbered buffer. The headers and packet control token are saved in the lower numbered buffer.

The headers and packet control token are saved to the buffer until it is full. No more data is saved once it is full. The software should flush the buffer to receive the latest header information.

In the header RX buffer, set the RXDP(N)CFG0.INSERTPKTTOKEN bit to 0 for correct operation. The packet control token is still included at the end of received headers. The packet control token takes the same form as isochronous receive.

5.5.3.9 Triggering the HSDI_AV Signal

When receiving DV data the available signal goes active when either the receive buffer has 1 quadlet pending in the buffer.

5.5.4 DV Receive

ceLynx can be formatted to strip any of the 1394 isochronous or CIP headers and time stamp from received packets before data is stored in the data buffer.

Table 5−21. Receive Header Stripping

DV RECEIVE PACKET HEADERS	REGISTER BITS USED TO STRIP HEADERS
ISO HEADER	RXDP(N)CFG0.STRIPHDR0
CIP0	RXDP(N)CFG0.STRIPHDR1
CIP1/TIME STAMP	RXDP(N)CFG0.STRIPHDR2
DVH0_0	Cannot be stripped on receive
DVH0_1	Cannot be stripped on receive

NOTE:
The RXDPB(N)CFG3 and RXDPB(N)CFG4 registers allow ceLynx to filter incoming packets. ceLynx can receive packets based on source ID, data length, or header 0 information. The MASK bits allow the filter to mask off bits of the incoming packet.

The user should not enable the insert packet control token on receive.

Either the host or HSDI can access the data buffer. The host can access the data buffer through the DB(N)ACC0 register for the associated buffer.

5.5.5 DV Transmit

For DV transmit, ceLynx can be configured to include any of the four 1394 DV headers. The TXDP(N)CFG.HIM control bit automatically inserts the necessary headers as specified by DB(N)CFG0.STREAMTYPE. ceLynx automatically inserts the H0 DIF block header if the TXDP(N)CFG.H0IM bit is selected.

Table 5−22. DV TX Headers

DV TRANSMIT PACKET HEADERS	REGISTERS USED TO INSERT HEADERS	DEFAULT VALUES FOR DV TX
ISO HEADER	TXDP(N)H0	0008 40A0
CIP0	TXDP(N)H1	0078 0000
CIP1	TXDP(N)H2	8000 FFFF
DV_H0	TXDP(N)H3	0000 0000
DV_H1	TXDP(N)H4	0000 0000

NOTE:
The application must supply quadlet-aligned data in DV transmit mode. No padding bits is added.

The host can access the data buffer through the DB(N)ACC0 and DB(N)ACC1 registers for the associated buffer. The host should write all transmit quadlets except the last to the DB(N)ACC0 register. The host should write the last transmit quadlet to the DB(N)ACC1 register.

5.6 PHY Configuration Packet

The format of the PHY configuration packet is shown in Figure 5−27 and is described in Table 5−26. The PHY configuration packet transmit contains two quadlets, which are loaded into the selected data buffer. The default data buffer for asynchronous transmit is buffer 4 and is accessed by the microprocessor. The first quadlet is written to the DB(N)ACC0 register for the appropriate data buffer. The last quadlet is written to the DB(N)ACC1 register for the appropriate data buffer. The 0x00E0 in the first quadlet tells ceLynx that this quadlet is the PHY configuration packet. The 0xE is then replaced with 0x0 before the packet is transmitted to the PHY interface.

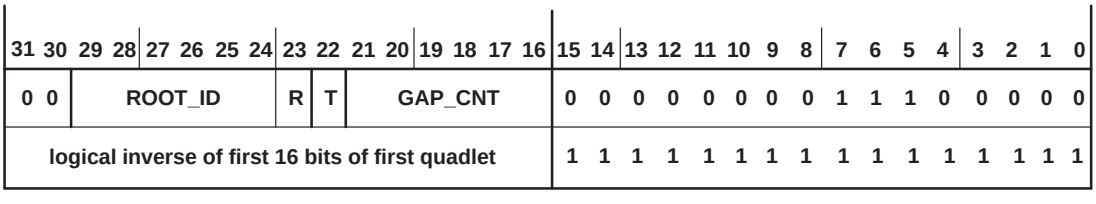


Figure 5−25. PHY Configuration Packet Format

Table 5−23. PHY Configuration Packet Functions

FIELD NAME	DESCRIPTION
00	The 00 field is the PHY configuration packet identifier.
ROOT_ID	The ROOT_ID field is the physical_ID of the node to have its force_root bit set (only meaningful when R is set).
R†	When R is set, the force-root bit of the node identified in root_ID is set and the force_root bit of all other nodes are cleared. When R is cleared, root_ID is ignored.
T†	When T is set, the PHY_Configuration.gap_cnt field of all the nodes is set to the value in the gap_cnt field.
GAP_CNT	The GAP_CNT field contains the new value for PHY_CONFIGURATION.gap_count for all nodes. This value goes into effect immediately upon receipt and remains valid after the next bus reset. After the second reset, GAP_CNT is set to 0x63 unless a new PHY configuration packet is received.

† A PHY configuration packet with R = 0 and T = 0 is reserved and is ignored when received.

5.7 Extended PHY Packets

5.7.1 Remote Access Packet

ceLynx can transmit a remote access packet to read a remote node's PHY registers. Figure 5−28 shows the format for this type of packet.

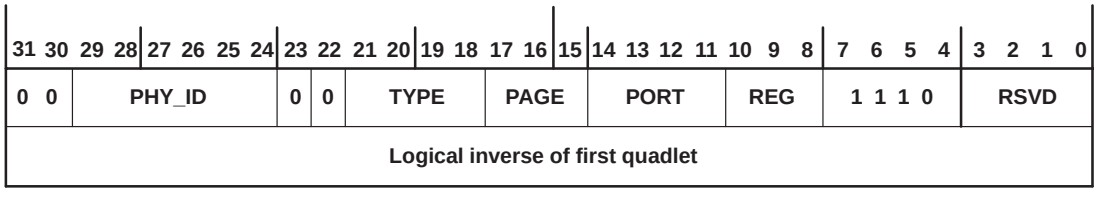


Figure 5−26. Remote Access Packet Format

Table 5−24. Remote Access Packet Functions

FIELD NAME	DESCRIPTION
00	The 00 field is the PHY packet identifier.
PHY_ID	Physical node identifier of the destination of this packet
TYPE	Extended PHY packet type: 1 Register read (base registers) 5 Register read (paged registers)
PAGE	This field corresponds to the *Page_Select* field in the PHY registers. The register read behaves as if the *Page_select* was set to this value.
PORT	This field corresponds to the *Port_select* field in the PHY registers. The register read behaves as if *Port_select* was set to this value.
REG	This field, in combination with page and port, specifies the PHY register. If type indicates a read request of the base PHY registers, the read directly addresses one of the first eight PHY registers. Otherwise, the PHY register address is 1000b + REG.
RSVD	Reserved

5.7.2 Remote Reply Packet

ceLynx can receive a remote reply packet in response to a transmitted remote reply packet.

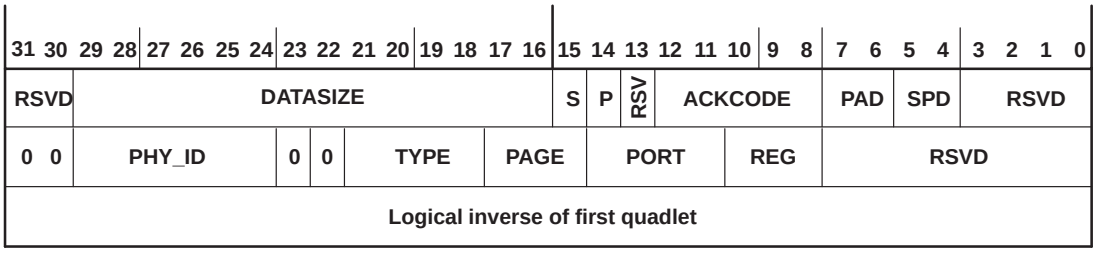


Figure 5−27. Remote Reply Packet − Receive

Table 5−25. Remote Reply Packet Functions

FIELD NAME	DESCRIPTION
RSVD	Reserved
DATASIZE	Packet control token - Size of the packet in quadlets
S	Packet control token - This bit is set to 1 whenever the packet control token is attached to a self-ID packet.
P	Packet control token - This bit is set to 1 whenever the packet control token is attached to a PHY packet.
RSVD	Reserved
ACKCODE	Packet control token - This 5-bit field holds the acknowledge code sent by the receiver for the current packet. See Table 5−10 for ACK codes.
PAD	Packet control token - Number of padding bytes added.
SPD	Packet control token - The SPD field indicates the speed at which the current packet was sent. 00 = 100 Mbps, 01 = 200 Mbps, 10 = 400 Mbps, and 11 is undefined for this implementation.
RSVD	Reserved
00	The 00 field is the PHY packet identifier.
PHY_ID	Physical node identifier of the destination of this packet.
TYPE	Extended PHY packet type: 1 Register read (base registers) 5 Register read (paged registers)
PAGE	This field corresponds to the *Page_Select* field in the PHY registers. The register read behaves as if the *Page_select* was set to this value.
PORT	This field corresponds to the *Port_select* field in the PHY registers. The register read behaves as if *Port_select* was set to this value.
REG	This field, in combination with page and port, specifies the PHY register. If type indicates a read request of the base PHY registers, the read directly addresses one of the first eight PHY registers. Otherwise, the PHY register address is 1000b + REG.
RSVD	Reserved

5.7.3 Remote Command Packet

ceLynx transmits a remote command packet to request the node identified by PHY_ID to perform a specified operation.

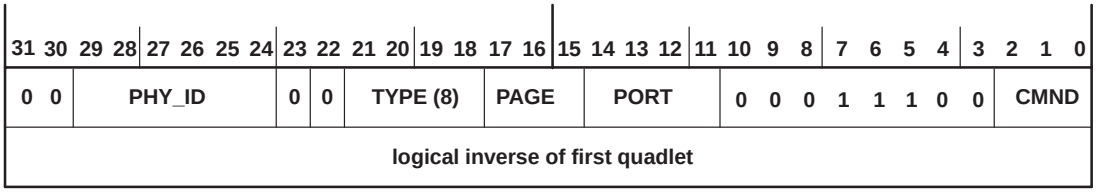


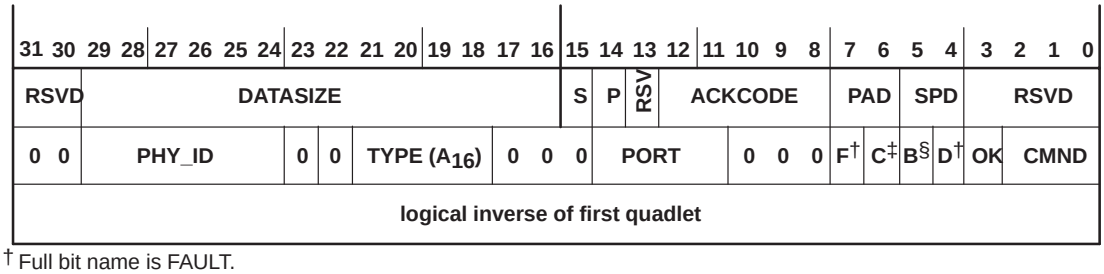
Figure 5−28. Remote Command Packet

Table 5−26. Remote Command Packet Functions

FIELD NAME	DESCRIPTION
00	The 00 field is the PHY packet identifier.
PHY_ID	Physical node identifier of the destination of this packet
TYPE	Extended PHY packet type: (1000b indicates command packet)
PAGE	This field corresponds to the *Page_Select* field in the PHY registers. The register read behaves as if the *Page_select* was set to this value.
PORT	This field selects one of the PHY ports.
CMND	Command: 0 NOP 1 Transmit TX_DISABLE_NOTIFY then disable port 2 Initiate suspend (i.e. become a suspend initiator) 4 Clear the port fault bit to zero 5 Enable port 6 Resume port

5.7.4 Remote Confirmation Packet

ceLynx receives a remote confirmation packet in response to a remote command packet.



† Full bit name is FAULT.
‡ Full bit name is CONNECTED.
§ Full bit name is BIAS.
¶ Full bit name is DISABLED.

Figure 5−29. Remote Confirmation Packet

Table 5−27. Remote Confirmation Packet Functions

FIELD NAME	DESCRIPTION
RSVD	Reserved
DATASIZE	Packet control token - Size of the packet in quadlets
S	Packet control token - This bit is set to 1 whenever the packet control token is attached to a self-ID packet.
P	Packet control token - This bit is set to 1 whenever the packet control token is attached to a PHY packet.
RSVD	Reserved

Table 5−27. Remote Confirmation Packet Functions (Continued)

FIELD NAME	DESCRIPTION
ACKCODE	Packet control token - This 5-bit field holds the acknowledge code sent by the receiver for the current packet. See Table 5−10 for a list of ACK codes.
PAD	Packet control token - Number of padding bytes added
SPD	Packet control token - The spd field indicates the speed at which the current packet was sent. 00 = 100 Mbps, 01 = 200 Mbps, 10 = 400 Mbps, and 11 is undefined for this implementation.
RSVD	Reserved
00	The 00 field is the PHY packet identifier.
PHY_ID	Physical node identifier of the destination of this packet
TYPE	Extended PHY packet type: (1010b indicates confirmation packet)
PORT	This field will specify the PHY port to which this packet pertains.
FAULT	Abbreviated as F in Figure 5−29. This bit is the current value of the fault bit from PHY register 1000b for the addressed port.
CONNECTED	Abbreviated as C in Figure 5−29. This bit is the current value of the connected bit from PHY register 1000b for the addressed port.
BIAS	Abbreviated as B in Figure 5−29. This bit is the current value of the bias bit from PHY register 1000b for the addressed port.
DISABLED	Abbreviated as D in Figure 5−29. This bit is the current value of the disabled bit from PHY register 1000b for the addressed port.
OK	Set to 1 if the command was accepted by the PHY. Set to 0 otherwise.
CMND	The CMND value (from the preceding remote command packet) with which this confirmation packet is associated.

5.7.5 Resume Packet

ceLynx transmits a broadcast resume packet to commence operation on any node that is both connected and suspended. The link logic automatically attaches the logical inverse second quadlet.

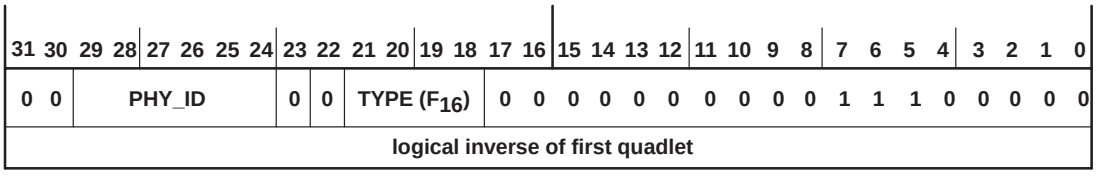


Figure 5−30. Resume Packet

Table 5−28. Resume Packet Functions

FIELD NAME	DESCRIPTION
00	The 00 field is the PHY packet identifier.
PHY_ID	Physical node identifier of the source of this packet
TYPE	Extended PHY packet type (1111b) indicates command packet

5.8 Receive Self-ID Packet

The self-ID packets can be either ignored or received into the data buffer based on the RCVSID bits in the RXDPB(N)CFG1. The user must select which data buffer receives the self-IDs. This can be set in the RXDPB(N)CFG1 register, bit 9. The default setting is self-ID packets routed to data buffer 6 and accessed by the microprocessor port. The RXSIDFULL bit in register 0x300 enables ceLynx to receive both quadlets in the selected data buffer; the self-ID and its inverse. Refer to Table 5−33.

The SIDEND bit in register 0x308 indicates the end of the self-ID period. The LINT.SELFIDERR interrupt in register 0x044 indicates a self-ID error. This error can be decoded in the LCTRL.SIDERCODE bits in register 0x040.

A packet control token is always attached to received self-ID packets. This control token gives information on the receive status. See Figure 5−33 and Table 5−34 for packet control token format.

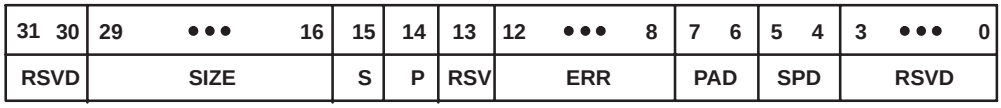


Figure 5−31. Self-ID Packet Control Token Format

Table 5−29. Bit Descriptions for Self-ID Packet Control Token

BIT NAME	DESCRIPTION	
RSVD	Reserved	
Size	Size of the packet in quadlets	
S	This bit is set when the token is attached to a self-ID packet.	
P	This bit is set when the token is attached to a PHY packet.	
RSVD	Reserved	
ERR	When the packet control token is attached to a self-ID packet, this 3-bit field contains the self-ID error code. The error codes are noted in the LCTRL register, bits 6:4.	
	000	No error
	001	Last self-ID received was not all child ports.
	010	Received PHY ID in self-ID was not as expected.
	011	Quadlet not inverted (phase error)
	100	PHY ID sequence error (two or more gaps in Ids)
	101	PHY ID sequence error (large gap in packet)
	110	PHY ID error within packet
	111	Quadlet not the inversion of the prior quadlet
PAD	Number of bytes padded (e.g., data_length = 9, pad = 1)	
SPD	Speed code of the received packet	
RSVD	Reserved	

Table 5−30. Receive Self-ID Setup Using Control Register Bits (RCVSID and RXSIDFULL)

RCVSID	RXSIDFULL	OPERATION
0	X	Self-ID packets are not received by the link.
1	0	Only the data quadlet (first quadlet) of the self-ID packets are received into the selected data buffer.
1	1	Both the data quadlet (first quadlet) and the logical inverse quadlet (second quadlet) of all self-ID packets are received into the selected data buffer.

Figure 5−34 and Figure 5−35 show the format of a received self-ID packet. For completeness, the figures assume the cable PHY on the bus implements the maximum number of ports allowed by the 1394.a specification. Both figures show one received self-ID packet. The contents are described in Table 5−35.

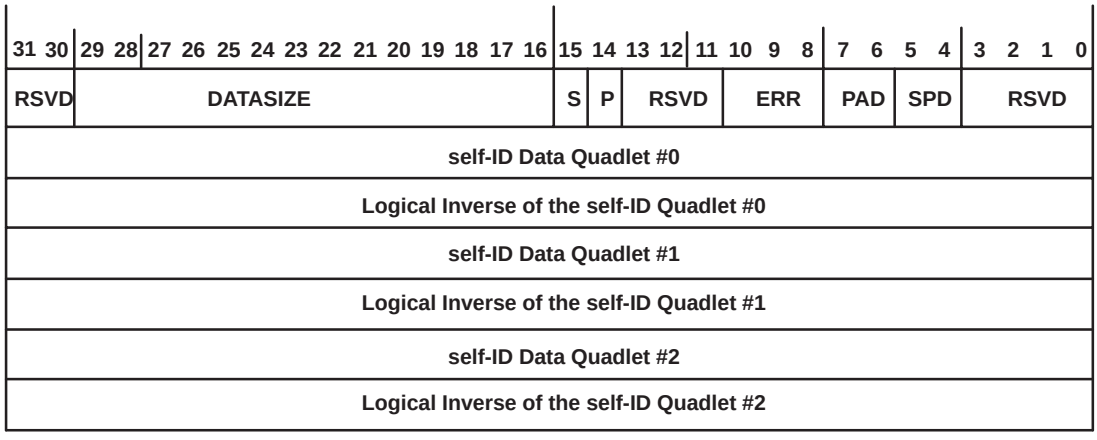


Figure 5−32. Receive Self-ID Packet Format (RCVSID = 1, RXSIDFULL = 1)

Figure 5−35 shows the format of the received self-ID packet when the RXSIDFULL is cleared. In this case, only the first quadlet of each self-ID packet and the packet control token is received in the selected data buffer. Self-ID packets include the packet control token.

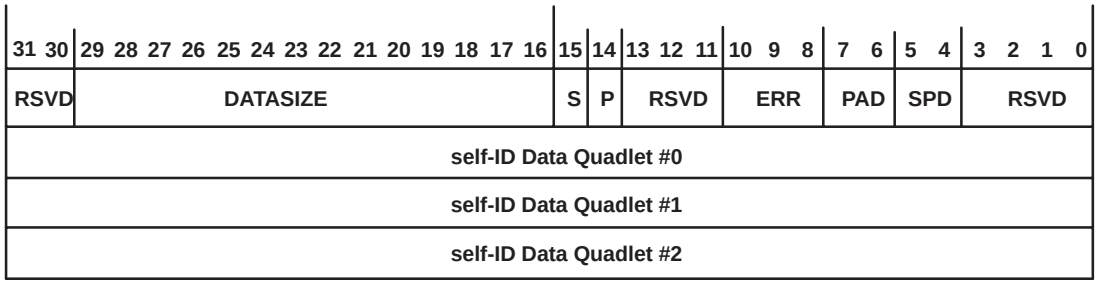


Figure 5−33. Receive Self-ID Packet Format (RCVSID = 1, RXSIDFULL = 0)

Table 5−31. Receive Self-ID Function

FIELD NAME	DESCRIPTION
DATASIZE	Packet control token - Size of the packet in quadlets
S	Packet control token - This bit is set to 1 whenever the packet control token is attached to a self-ID packet.
P	Packet control token - This bit is set to 1 whenever the packet control token is attached to a PHY packet.
ERR	Packet control token - This 3-bit field holds the self-ID error code. See the LCTRL.SIDERCODE register for error codes.
PAD	Packet control token - Number of padding bytes added.
SPD	Packet control token - The spd field indicates the speed at which the current packet was sent. 00 = 100 Mbps 01 = 200 Mbps 10 = 400 Mbps 11 = Undefined for this implementation.
self-ID data quadlet	Contains self-ID information
Logical inverse of the self-ID quadlet	Logical inverse of the self-ID quadlet

The cable PHY sends one to three self-ID packets at the base rate (100 Mbps) during the self-ID phase of arbitration or in response to a ping packet. The number of self-ID packets sent depends on the number of ports.

Example: If there are three 1394.a compliant nodes on the bus, each with a PHY containing three or fewer ports, the selected data buffer is shown below.

Table 5−32. Data Buffer Contents (following a bus reset) With Three Nodes on the Bus

DATA BUFFER #N CONTENTS	DESCRIPTION
0006 8(err)00	Self-ID packet control token
Self-ID 1	Self-ID quadlet for PHY #1
Self-ID 1 (inverse)	Logical inverse quadlet for self-ID of PHY #1
Self-ID 2	Self-ID quadlet for PHY #2
Self-ID 2 (inverse)	Logical inverse quadlet for self-ID of PHY #2
Self-ID 3	Self-ID quadlet for PHY #3
Self-ID 3 (inverse)	Logical inverse quadlet for self-ID of PHY #3

6 Register Map Detail

6.1 Register Description Notes

All shaded areas indicate reserved memory locations. All reset field values are hexadecimal. The meaning of notation in the type field for bit descriptions is as follows:

R – Bit location can be read by software.

R0 – Bit location can be read by software and always returns 0 when read.

R1 – Bit location can be read by software and always returns 1 when read.

W – Bit location can be written by software.

C – Write 1 to clear.

U – Bit location is synchronously updated by hardware.

The values shown in the reset field of bit description are given in hexadecimal values. Two descriptive terms are also used in the reset field as follows:

PIN – Data for the associated register is provided directly by an external pin.

DEP – Data is buffer-dependent, defaults are tabularized in the bit description.

All registers in the CFR maps are shown on quadlet boundaries. Registers are logically grouped for clarity. All doublet addresses are individually accessible.

Figure 6−1 shows the address space of the core modules. This table shows the address ranges used to generate the appropriate module select signals. The entire byte-mapped space occupied by the module CFRs is listed in the table. Quadlet accesses must be quadlet aligned, doublet accesses must be doublet aligned. Misaligned and byte accesses are not supported.

Table 6−1. ceLynx Address Ranges

ADDRESS RANGE (Hexadecimal)	MODULE
000−03F	SYS
040−07F	LLC
080−0BF	HSDIA
0C0−0FF	HSDIB
100−13F	Encrypt
140−23F	HCDB
240−33F	TXDP
340−3FF	RXDP

6.2 Endianness

All registers and multibit fields in this document are diagrammed such that the MSB is leftmost. The terms big endian and little endian do not appear in association with any register or bit field description. All endian related bit descriptions are made in a generic manner and provide examples.

6.2.1 System Information CFR Map

Address	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	SYS CFR Name (Hex Reset Value)
000h	0	1	1	1	0	0	1	1	0	0	0	1	1	0	0	1	1	0	0	1	0	0	1	0	1	0	1	1	0	0	0	0	ID (7319_92x0h)
004h	GPIOINT1SEL				GPIOINT0SEL				HSDIBAVPOL	HSDIBRWPOL	HSDIBENPOL	HSDIBSYNCPOL	HSDIAAVPOL	HSDIARWPOL	HSDIAENPOL	HSDIASYNCPOL	ISOLATION_DIS			CONTENDEROE			MCINTZFLT	MCACKZFLT				MCACKZPOL	MCSTRBZPOL	MCRWPOL	MCCSZPOL	MCS32ZPOL		PINCFG (FFFF_0304h)
008h		GPIO9SEL			GPIO8SEL				GPIO7SEL		GPIO6SEL			GPIO5SEL				GPIO4SEL			GPIO3SEL			GPIO2SEL			GPIO1SEL			GPIO0SEL			GPIOSEL (0000_0000h)
00Ch		GPIOIN9	GPIOOUT9	GPIO9STAT	GPIOIN8	GPIOOUT8	GPIO8STAT	GPIOIN7	GPIOOUT7	GPIO7STAT	GPIOIN6	GPIOOUT6	GPIO6STAT	GPIOIN5	GPIOOUT5	GPIO5STAT		GPIOIN4	GPIOOUT4	GPIO4STAT	GPIOIN3	GPIOOUT3	GPIO3STAT	GPIOIN2	GPIOOUT2	GPIO2STAT	GPIOIN1	GPIOOUT1	GPIO1STAT	GPIOIN0	GPIOOUT0	GPIO0STAT		GPIOCFG (0000_0000h)
010h																						MCACKZDLY							MCENDIAN	MCRWISOE	LOCACCPRTY		MCIFCFG (0000_0104h)
014h	GPIOINTEN1	GPIOINTEN0		MCIFINTEN	RXDPINTEN1	RXDPINTEN0	TXDPINTEN1	TXDPINTEN0	DBINTEN3	DBINTEN2	DBINTEN1	DBINTEN0	HSDIBINTEN	HSDIAINTEN	LLCINTEN1	LLCINTEN0	GPIOINT1	GPIOINT0		MCIFINTR	RXDPINT1	RXDPINT0	TXDPINT1	TXDPINT0	DBINT3	DBINT2	DBINT1	DBINT0	HSDIBINT	HSDIAINT	LLCINT1	LLCINT0		SYSINT (1000_0000h)
018h													SERIALDONEINTEN	SERIALERRINTEN		MCERRINTEN												SERIALDONEINT	SERIALERRINT		MCERRINT		MCIFINT (0008_0000h)
01Ch									SERIALADDR																		RELOAD	DONE	TIMINGER	CKSUMER	NOEEPROM		Serial STAT0 (0000_0000h)
020h																		SERIALDATA																Serial STAT1 (0000_0000h)
024h																		SOFTRESET																SRST (0000_0000h)
028-03Fh																																		RSVD (0000_0000h)

6.2.2 SYS CFR Bit Descriptions

0x000 ID – Chip Identification Number				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:0	ID	R	731992x0	Identification – The value in this register is hardwired to 0x7319 92x0. Future revisions may be indicated by a change in the lower byte. This document covers the following parts/IDs: TSB42AA4 − 0x7319 92C0 TSB42AB4 − 0x7319 92B0

0x004 PINCFG – Pin Configuration				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:28	GPIOINT1SEL	RW	F	GPIO interrupt 1 select – The binary encoded value in this register selects one of the 10 GPIOs as the interrupt source for SYSINT.GPIOINT1. No interrupt source is selected when any value greater than 1001b is written to this field.
27:24	GPIOINT0SEL	RW	F	GPIO interrupt 0 select – The binary encoded value in this register selects one of the 10 GPIOs as the interrupt source for SYSINT.GPIOINT0. No interrupt source is selected when any value greater than 1001b is written to this field.
23	HSDIAAVPOL	RW	1	HSDIA AV polarity – The value written to this location indicates the active level of the associated pin. 1−active high, 0−active low
22	HSDIARWPOL	RW	1	HSDIA RW polarity − The value written to this location indicates the active level of the associated pin. 1−active high, 0−active low
21	HSDIAENPOL	RW	1	HSDIA EN polarity − The value written to this location indicates the active level of the associated pin. 1−active high, 0−active low
20	HSDIASYNCPOL	RW	1	HSDIA SYNC polarity − The value written to this location indicates the active level of the associated pin. 1−active high, 0−active low
19	HSDIBAVPOL	RW	1	HSDIB AV polarity – The value written to this location indicates the active level of the associated pin. 1−active high, 0−active low
18	HSDIBRWPOL	RW	1	HSDIB RW polarity − The value written to this location indicates the active level of the associated pin. 1−active high, 0−active low
17	HSDIBENPOL	RW	1	HSDIB EN polarity − The value written to this location indicates the active level of the associated pin. 1−active high, 0−active low
16	HSDIBSYNCPOL	RW	1	HSDIB SYNC polarity − The value written to this location indicates the active level of the associated pin. 1−active high, 0−active low
15	ISOLATION_DIS	RW	0	Bus holder isolation disable bit – When set to 1, the bus holder isolation for the PHY-link interface is disabled.
14:13	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
12	CONTENDEROE	RW	0	Contender output enable – Determines the direction of the PLI_CNTDR pin on the PHY/link interface. When set to 1, the device drives the PLI_CNTDR pin as an output. When set to 0, the PLI_CNTDR pin is an input to the device.
11:10	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
9	MCINTZFLT	RW	1	Programmable microcontroller interrupt interrupt float − When this bit is set to 1, the microcontroller interface INTZ pin output driver is turned off unless the signal is actively asserted.
8	MCACKZFLT	RW	1	Programmable microcontroller acknowledge float − When this bit is set to 1, the microcontroller interface MCIF_ACKZ pin output driver is turned off when the signal is not actively asserted.

0x004 PINCFG – Pin Configuration (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
7:6	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
5	MCACKZPOL	W	0	Programmable microcontroller acknowledge polarity − The value written to this location indicates the active level of the MCIF_ACKZ pin. 1−active high, 0−active low
4	MCACKZPOL	R	0	Programmable microcontroller acknowledge polarity − The value contained in this location indicates the active level of the MCIF_ACKZ pin. 1−active high, 0−active low
3	MCSTRBZPOL	RW	0	Programmable microcontroller data strobe polarity − The value written to this location indicates the active level of the MCIF_STRBZ pin. 1−active high, 0−active low
2	MCRWPOL	RW	1	Programmable microcontroller read/write polarity − The value written to this location indicates the active level of the MCIF_RWZ pin. When this bit is set to 1: Read − 1 Write − 0 When this bit is set to 0: Read − 0 Write − 1
1	MCCSZPOL	RW	0	Programmable microcontroller chip select polarity − The value written to this location indicates the active level of the MCIF_CSZ pin. 1−active high, 0−active low
0	MCS32ZPOL	RW	0	Programmable microcontroller transfer size polarity − The value written to this location indicates the active level of the MCIF_S32Z pin. 1−active high, 0−active low

0x008 GPIOSEL – GPIO Output Source Select				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
30:28	GPIO9SEL	RW	0	GPIO9 source select – The binary encoded value written to this location selects the function of the associated GPIO. 000 – General-purpose input 001 – HSDIB WTRMRK 0 (see Note 1) 010 – HSDIB WTRMRK 1 (see Note 1) 011 – Video select B DV frame in 100 – Video select B DV frame out 101 – HSDIB SCC clock 110 – HSDIB DirecTV error 111 – General-purpose output
27:25	GPIO8SEL	RW	0	GPIO8 source select – The binary encoded value written to this location selects the function of the associated GPIO. 000 – General-purpose input 001 – HSDIB WTRMRK 0 (see Note 1) 010 – HSDIB WTRMRK 1 (see Note 1) 011 – Video select B DV frame in 100 – Video select B DV frame out 101 – HSDIB SCC clock 110 – HSDIB DirecTV error 111 – General-purpose output

NOTE 1: The watermarks are associated with data buffers routed to the HSDIx. A buffer can be selected for the watermark 0/1 only by applying the buffer address at the HSDIx address lines (HSDIxA[2:0]).

0x008 GPIOSEL – GPIO Output Source Select (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
24:22	GPIO7SEL	RW	0	GPIO7 source select – The binary encoded value written to this location selects the function of the associated GPIO. 000 – General-purpose input 001 – HSDIB WTRMRK 0 (see Note 1) 010 – HSDIB WTRMRK 1 (see Note 1) 011 – Video select B DV frame in 100 – Video select B DV frame out 101 – HSDIB SCC clock 110 – HSDIB DirecTV error 111 – General-purpose output
21:19	GPIO6SEL	RW	0	GPIO6 source select – The binary encoded value written to this location selects the function of the associated GPIO. 000 – General-purpose input 001 – HSDIB WTRMRK 0 (see Note 1) 010 – HSDIB WTRMRK 1 (see Note 1) 011 – Video select B DV frame in 100 – Video select B DV frame out 101 – HSDIB SCC clock 110 – HSDIB DirecTV error 111 – General-purpose output
18:16	GPIO5SEL	RW	0	GPIO5 source select – The binary encoded value written to this location selects the function of the associated GPIO. 000 – General-purpose input 001 – Cycle source input 010 – HSDIB SCC clock 011 – HSDIB DirecTV error 100 – Reserved 101 – Reserved 110 – Reserved 111 – General-purpose output
15	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
14:12	GPIO4SEL	RW	0	GPIO4 source select – The binary encoded value written to this location selects the function of the associated GPIO. 000 – General-purpose input 001 – Cycle source input 010 – HSDIA SCC clock 011 – HSDIA DirecTV error 100 – Reserved 101 – Reserved 110 – Reserved 111 – General-purpose output
11:9	GPIO3SEL	RW	0	GPIO3 source select – The binary encoded value written to this location selects the function of the associated GPIO. 000 – General-purpose input 001 – HSDIA WTRMRK 0 (see Note 1) 010 – HSDIA WTRMRK 1 (see Note 1) 011 – Video select A DV frame in 100 – Video select A DV frame out 101 – HSDIA SCC clock 110 – HSDIA DirecTV error 111 – General-purpose output

NOTE 1: The watermarks are associated with data buffers routed to the HSDIx. A buffer can be selected for the watermark 0/1 only by applying the buffer address at the HSDIx address lines (HSDIxA[2:0]).

0x008 GPIOSEL – GPIO Output Source Select (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
8:6	GPIO2SEL	RW	0	GPIO2 source select – The binary encoded value written to this location selects the function of the associated GPIO. 000 – General-purpose input 001 – HSDIA WTRMRK 0 (see Note 1) 010 – HSDIA WTRMRK 1 (see Note 1) 011 – Video select A DV frame in 100 – Video select A DV frame out 101 – HSDIA SCC clock 110 – HSDIA DirecTV error 111 – General-purpose output
5:3	GPIO1SEL	RW	0	GPIO1 source select – The binary encoded value written to this location selects the function of the associated GPIO. 000 – General-purpose input 001 – HSDIA WTRMRK 0 (see Note 1) 010 – HSDIA WTRMRK 1 (see Note 1) 011 – Video select A DV frame in 100 – Video select A DV frame out 101 – HSDIA SCC clock 110 – HSDIA DirecTV error 111 – General-purpose output
2:0	GPIO0SEL	RW	0	GPIO0 source select – The binary encoded value written to this location selects the function of the associated GPIO. 000 – General-purpose input 001 – HSDIA WTRMRK 0 (see Note 1) 010 – HSDIA WTRMRK 1 (see Note 1) 011 – Video select A DV frame in 100 – Video select A DV frame out 101 – HSDIA SCC clock 110 – HSDIA DirecTV error 111 – General-purpose output

NOTE 1: The watermarks are associated with data buffers routed to the HSDIx. A buffer can be selected for the watermark 0/1 only by applying the buffer address at the HSDIx address lines (HSDIxA[2:0]).

0x00C GPIOCFG – GPIO Configuration				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
30	GPIO9IN	RU	0	GPIO9 input – The current value of the associated GPIO pin is reflected in this register.
29	GPIO9OUT	RW	0	GPIO9 output – When the associated GPIO is configured as a general-purpose output, the value written to this bit location is driven on the associated GPIO terminal.
28	GPIO9STAT	RCU	0	GPIO9 status − This bit is set by hardware when a level shift is detected on the associated GPIO pin. The SYSINT.GPIOINT[N] interrupt is also set, when enabled. Writing a 1 to this location clears the bit, until the next change is detected on the GPIO pin.
27	GPIO8IN	RU	0	GPIO8 input – The current value of the associated GPIO pin is reflected in this register.
26	GPIO8OUT	RW	0	GPIO8 output – When the associated GPIO is configured as a general-purpose output, the value written to this bit location is driven on the associated GPIO terminal.
25	GPIO8STAT	RCU	0	GPIO8 status − This bit is set by hardware when a level shift is detected on the associated GPIO pin. The SYSINT.GPIOINT[N] interrupt is also set, when enabled. Writing a 1 to this location clears the bit, until the next change is detected on the GPIO pin.
24	GPIO7IN	RU	0	GPIO7 input – The current value of the associated GPIO pin is reflected in this register.
23	GPIO7OUT	RW	0	GPIO7 output – When the associated GPIO is configured as a general-purpose output, the value written to this bit location is driven on the associated GPIO terminal.
22	GPIO7STAT	RCU	0	GPIO7 status − This bit is set by hardware when a level shift is detected on the associated GPIO pin. The SYSINT.GPIOINT[N] interrupt is also set, when enabled. Writing a 1 to this location clears the bit, until the next change is detected on the GPIO pin.
21	GPIO6IN	RU	0	GPIO6 input – The current value of the associated GPIO pin is reflected in this register.
20	GPIO6OUT	RW	0	GPIO6 output – When the associated GPIO is configured as a general-purpose output, the value written to this bit location is driven on the associated GPIO terminal.
19	GPIO6STAT	RCU	0	GPIO6 status − This bit is set by hardware when a level shift is detected on the associated GPIO pin. The SYSINT.GPIOINT[N] interrupt is also set, when enabled. Writing a 1 to this location clears the bit, until the next change is detected on the GPIO pin.
18	GPIO5IN	RU	0	GPIO5 input – The current value of the associated GPIO pin is reflected in this register.
17	GPIO5OUT	RW	0	GPIO5 output – When the associated GPIO is configured as a general-purpose output, the value written to this bit location is driven on the associated GPIO terminal.
16	GPIO5STAT	RCU	0	GPIO5 status − This bit is set by hardware when a level shift is detected on the associated GPIO pin. The SYSINT.GPIOINT[N] interrupt is also set, when enabled. Writing a 1 to this location clears the bit, until the next change is detected on the GPIO pin.
15	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.

0x00C GPIOCFG – GPIO Configuration (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
14	GPIO4IN	RU	0	GPIO4 input – The current value of the associated GPIO pin is reflected in this register.
13	GPIO4OUT	RW	0	GPIO4 output – When the associated GPIO is configured as a general-purpose output, the value written to this bit location is driven on the associated GPIO terminal.
12	GPIO4STAT	RCU	0	GPIO4 status − This bit is set by hardware when a level shift is detected on the associated GPIO pin. The SYSINT.GPIOINT[N] interrupt is also set, when enabled. Writing a 1 to this location clears the bit, until the next change is detected on the GPIO pin.
11	GPIO3IN	RU	0	GPIO3 input – The current value of the associated GPIO pin is reflected in this register.
10	GPIO3OUT	RW	0	GPIO3 output – When the associated GPIO is configured as a general-purpose output, the value written to this bit location is driven on the associated GPIO terminal.
9	GPIO3STAT	RCU	0	GPIO3 status − This bit is set by hardware when a level shift is detected on the associated GPIO pin. The SYSINT.GPIOINT[N] interrupt is also set, when enabled. Writing a 1 to this location clears the bit, until the next change is detected on the GPIO pin.
8	GPIO2IN	RU	0	GPIO2 input – The current value of the associated GPIO pin is reflected in this register.
7	GPIO2OUT	RW	0	GPIO2 output – When the associated GPIO is configured as a general-purpose output, the value written to this bit location is driven on the associated GPIO terminal.
6	GPIO2STAT	RCU	0	GPIO2 status − This bit is set by hardware when a level shift is detected on the associated GP10 pin. The SYSINT.GPIOINT[N] interrupt is also set, when enabled. Writing a 1 to this location clears the bit, until the next change is detected on the GPIO pin.
5	GPIO1IN	RU	0	GPIO1 input – The current value of the associated GPIO pin is reflected in this register.
4	GPIO1OUT	RW	0	GPIO1 output – When the associated GPIO is configured as a general-purpose output, the value written to this bit location is driven on the associated GPIO terminal.
3	GPIO1STAT	RCU	0	GPIO1 status − This bit is set by hardware when a level shift is detected on the associated GPIO pin. The SYSINT.GPIOINT[N] interrupt is also set, when enabled. Writing a 1 to this location clears the bit, until the next change is detected on the GPIO pin.
2	GPIO0IN	RU	0	GPIO0 input – The current value of the associated GPIO pin is reflected in this register.
1	GPIO0OUT	RW	0	GPIO0 output – When the associated GPIO is configured as a general-purpose output, the value written to this bit location is driven on the associated GPIO terminal.
0	GPIO0STAT	RCU	0	GPIO0 status − This bit is set by hardware when a level shift is detected on the associated GPIO pin. The SYSINT.GPIOINT[N] interrupt is also set, when enabled. Writing a 1 to this location clears the bit, until the next change is detected on the GP10 pin.

0x010 MCIFCFG – Microcontroller Interface Configuration				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:11	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
10:8	MCACKZDLY	RW	1	Programmable microcontroller acknowledge (ACKZ) output enable delay – The value written to this register determines the amount of delay between the deassertion of the ACKZ signal driver and the disabling of the ACKZ output enable. This delay is needed in designs where the ACKZ line is shared with other clients on the microprocessor bus. In this case the MCIF_ACKZ pin must be briefly deasserted before the output driver is turned off. The delay can be programmed for a value between 0 ns and 10 ns depending on the setting of the bits below (nominal values): MCACKZDLY Delay value 000 0 ns 001 0 ns (default) 010 0 ns 011 2 ns 100 4 ns 101 6 ns 110 8 ns 111 10 ns
7:3	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
2	MCENDIAN	RW	1	Microcontroller endianness − The endianness for data written to and read from the microcontroller interface (MCIF) is selected according to the value written to this location (big endian = 1). Data is interpreted as demonstrated in the following example: Data presented at the MCIF Mcif_addr[1]=1; mcif_addr[1]=0; Mcif_d[15:0] = ABCD mcif_d[15:0] = EF01 Internally stored quadlet; 31 0 MCENDIAN = 0 ABCD EF01 MCENDIAN = 1 EF01 ABCD
1	MCRWISOE	RW	0	Microcontroller RW is output enabled – For microprocessors that require separate read and write strobes this bit may be set to 1. When set to 1, the MCIF_RW pin on the microcontroller interface is used as the data bus output enable during read transactions.
0	LOCACCPRTY	RW	0	Local access priority – Writing a 1 to this location gives internal clients priority over the microprocessor in the event of a simultaneous access to an internal register by the microprocessor and an internal client. By default the microprocessor always wins a tie and there are no wait states inserted.

0x014 SYSINT – System Interrupts and Interrupt Enables				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	GPIOINTEN1	RW	0	GPIO interrupt 1 enable – When this bit is set to 1, an interrupt is generated if hardware sets SYSINT.GPIOINT1. When this bit is set to 0, SYSINT.GPIOINT1 is not an interrupt source.
30	GPIOINTEN0	RW	0	GPIO interrupt 0 enable – When this bit is set to 1, an interrupt is generated if hardware sets SYSINT.GPIOINT0. When this bit is set to 0, SYSINT.GPIOINT0 is not an interrupt source.
29	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
28	MCIFINTEN	RW	1	Microcontroller interface interrupt enable – When this bit is set to 1, an interrupt is generated if hardware sets SYSINT.MCIFINT. When this bit is set to 0, SYSINT.MCIFINT is not an interrupt source.
27	RXDPINTEN1	RW	0	Receive data path interrupt 1 enable − When this bit is set to 1, an interrupt is generated if hardware sets SYSINT.RXDPINT1. When this bit is set to 0, SYSINT.RXDPINT1 is not an interrupt source.
26	RXDPINTEN0	RW	0	Receive data path interrupt 0 enable − When this bit is set to 1, an interrupt is generated if hardware sets SYSINT.RXDPINT0. When this bit is set to 0, SYSINT.RXDPINT0 is not an interrupt source.
25	TXDPINTEN1	RW	0	Transmit data path interrupt 1 enable − When this bit is set to 1, an interrupt is generated if hardware sets SYSINT.TXDPINT1. When this bit is set to 0, SYSINT.TXDPINT1 is not an interrupt source.
24	TXDPINTEN0	RW	0	Transmit data path interrupt 0 enable − When this bit is set to 1, an interrupt is generated if hardware sets SYSINT.TXDPINT0. When this bit is set to 0, SYSINT.TXDPINT0 is not an interrupt source.
23	DBINTEN3	RW	0	DB interrupt 3 enable − When this bit is set to 1, an interrupt is generated if hardware sets SYSINT.DBINT3. When this bit is set to 0, SYSINT.BINT3 is not an interrupt source.
22	DBINTEN2	RW	0	DB interrupt 2 enable − When this bit is set to 1, an interrupt is generated if hardware sets SYSINT.DBINT2. When this bit is set to 0, SYSINT.DBINT2 is not an interrupt source.
21	DBINTEN1	RW	0	DB interrupt 1 enable − When this bit is set to 1, an interrupt is generated if hardware sets SYSINT.DBINT1. When this bit is set to 0, SYSINT.DBINT1 is not an interrupt source.
20	DBINTEN0	RW	0	DB interrupt 0 enable − When this bit is set to 1, an interrupt is generated if hardware sets SYSINT.DBINT0. When this bit is set to 0, SYSINT.DBINT0 is not an interrupt source.
19	HSDIBINTEN	RW	0	HSDIB interrupt enable − When this bit is set to 1, an interrupt is generated if hardware sets SYSINT.HSDIBINT. When this bit is set to 0, SYSINT.HSDIBINT is not an interrupt source.
18	HSDIAINTEN	RW	0	HSDIA interrupt enable − When this bit is set to 1, an interrupt is generated if hardware sets SYSINT.HSDIAINT. When this bit is set to 0, SYSINT.HSDIAINT is not an interrupt source.
17	LLCINTEN1	RW	0	Link interrupt 1 enable − When this bit is set to 1, an interrupt is generated if hardware sets SYSINT.LLCINT1. When this bit is set to 0, SYSINT.LLCINT1 is not an interrupt source.
16	LLCINTEN0	RW	0	Link interrupt 0 enable − When this bit is set to 1, an interrupt is generated if hardware sets SYSINT.LLCINT0. When this bit is set to 0, SYSINT.LLCINT0 is not an interrupt source.

0x014 SYSINT – System Interrupts and Interrupt Enables (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
15	GPIOINT1	RU	0	GPIO interrupt 1 – This bit is set by hardware when any change occurs on the GPIO pin selected by PINCFG.GPIOINT1S. This interrupt is cleared by writing 1 to the associated GPIOCFG.GPIO[N]STAT bit.
14	GPIOINT0	RU	0	GPIO interrupt 0 − This bit is set by hardware when any change occurs on the GPIO pin selected by PINCFG.GPIOINT0S. This interrupt is cleared by writing 1 to the associated GPIOCFG.GPIO[N]STAT bit.
13	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
12	MCIFINTR	RU	0	Microcontroller interface interrupt – This bit is set by hardware to indicate that an assigned interrupt in the MCIFINT register has been triggered. This bit is cleared when the interrupt is cleared in the MCIFINT register.
11	RXDPINT1	RU	0	Receive data path interrupt 1 − This bit is set by hardware to indicate that an assigned interrupt in the upper doublet of the RXDPINT register has been triggered. This bit is cleared when the interrupt is cleared in the RXDPINT register.
10	RXDPINT0	RU	0	Receive data path interrupt 0 − This bit is set by hardware to indicate that an assigned interrupt in the lower doublet of the RXDPINT register has been triggered. This bit is cleared when the interrupt is cleared in the RXDPINT register.
9	TXDPINT1	RU	0	Transmit data path interrupt 1 − This bit is set by hardware to indicate that an assigned interrupt in the upper doublet of the TXDPINT register has been triggered. This bit is cleared when the interrupt is cleared in the TXDPINT register.
8	TXDPINT0	RU	0	Transmit data path interrupt 0 − This bit is set by hardware to indicate that an assigned interrupt in the lower doublet of the TXDPINT register has been triggered. This bit is cleared when the interrupt is cleared in the TXDPINT register.
7	DBINT3	RU	0	DB interrupt 3 − This bit is set by hardware to indicate that an assigned interrupt in the upper doublet of the DBEINT register has been triggered. This bit is cleared when the interrupt is cleared in the DBEINT register.
6	DBINT2	RU	0	DB interrupt 2 − This bit is set by hardware to indicate that an assigned interrupt in the lower doublet of the DBEINT register has been triggered. This bit is cleared when the interrupt is cleared in the DBEINT register.
5	DBINT1	RU	0	DB interrupt 1 − This bit is set by hardware to indicate that an assigned interrupt in the upper doublet of the DBINT register has been triggered. This bit is cleared when the interrupt is cleared in the DBINT register.
4	DBINT0	RU	0	DB interrupt 0 − This bit is set by hardware to indicate that an assigned interrupt in the lower doublet of the DBINT register has been triggered. This bit is cleared when the interrupt is cleared in the DBINT register.
3	HSDIBINT	RU	0	HSDIB interrupt − This bit is set by hardware to indicate that an assigned interrupt in the HSDIBINT register has been triggered. This bit is cleared when the interrupt is cleared in the HSDIBINT register.
2	HSDIAINT	RU	0	HSDIA interrupt − This bit is set by hardware to indicate that an assigned interrupt in the HSDIAINT register has been triggered. This bit is cleared when the interrupt is cleared in the HSDIAINT register.

0x014 SYSINT – System Interrupts and Interrupt Enables (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
1	LLCINT1	RU	0	Link interrupt 1 − This bit is set by hardware to indicate that an assigned interrupt in the upper doublet of the LINT register has been triggered. This bit is cleared when the interrupt is cleared in the LINT register.
0	LLCINT0	RU	0	Link interrupt 0 − This bit is set by hardware to indicate that an assigned interrupt in the lower doublet of the LINT register has been triggered. This bit is cleared when the interrupt is cleared in the LINT register.

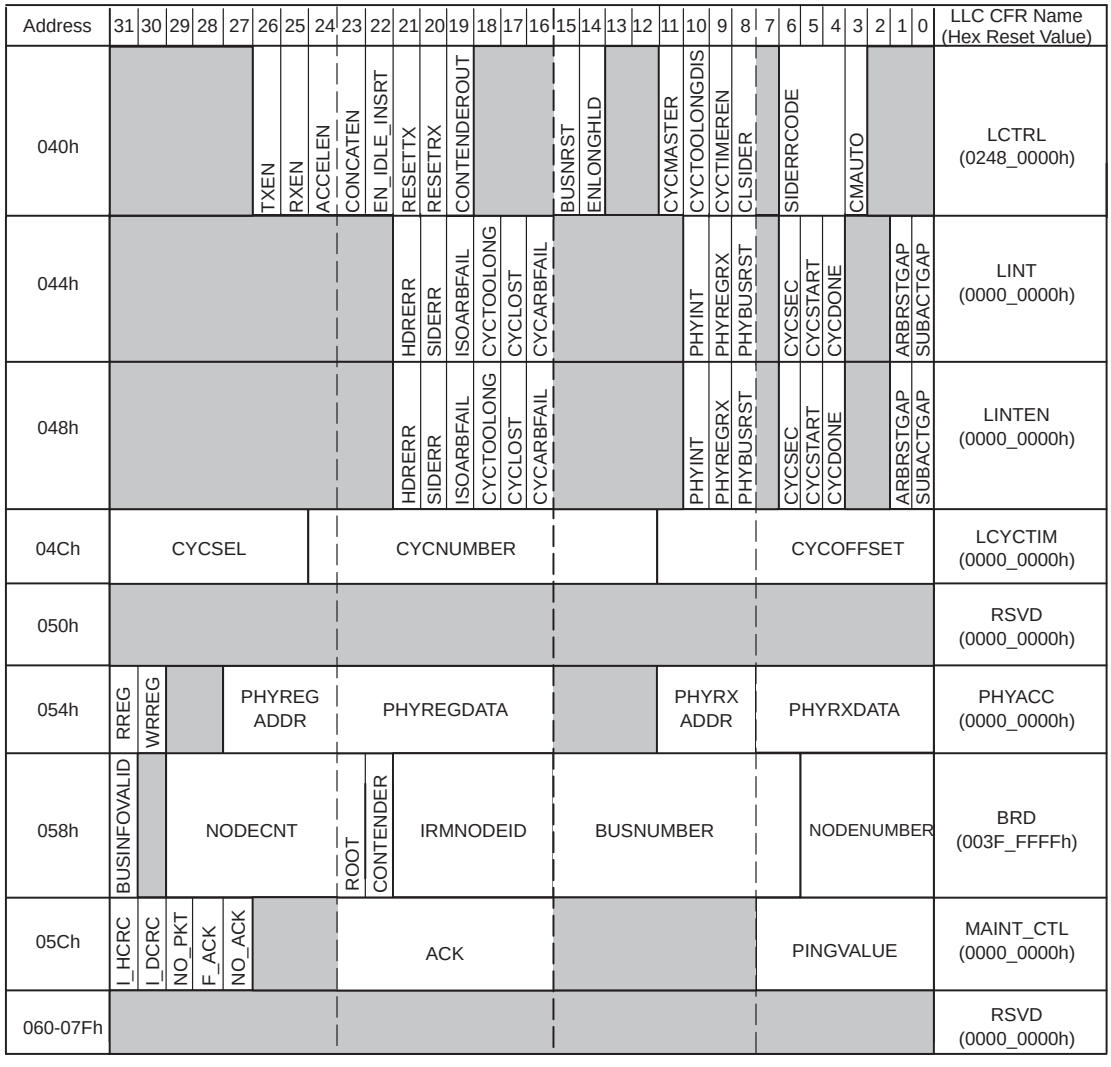
0x018 MCIFINT – Microcontroller Interface Interrupts and Interrupt Enables				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:20	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
19	SERIALDONEINTEN	RW	1	Two-wire serial interface done interrupt enable – When set to 1 MCIFINT.SerialDoneInt is an interrupt source. When set to 0 MCIFINT.SerialDoneInt is not an interrupt source. This interrupt is enabled at reset to allow the microcontroller to determine completion of EEPROM download without accessing the device.
18	SERIALERRINTEN	RW	0	Two-wire serial interface error interrupt enable − When set to 1 MCIFINT.SerialERRINT is an interrupt source. When set to 0 MCIFINT.SerialERRINT is not an interrupt source.
17	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
16	MCERRINTEN	RW	0	Microcontroller error interrupt enable − When set to 1 MCIFINT.MCERRINT is an interrupt source. When set to 0 MCIFINT.MCERRINT is not an interrupt source.
15:4	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
3	SERIALDONEINT	RCU	0	Two-wire serial interface done – This interrupt is generated when EEPROM download is complete or no EEPROM is detected on power up and the associated enable bit is set. Write 1 to clear.
2	SERIALERRINT	RCU	0	Two-wire serial interface error – This interrupt is generated when an error is detected on the two-wire serial interface and the associated enable bit is set. Write 1 to clear.
1	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
0	MCERRINT	RCU	0	Microcontroller error – This interrupt is generated by a micro read/write to a reserved location.

0x01C Serial Stat 0 − Two-Wire Serial Interface Status				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:26	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
25:16	SERIALADDR	RU	0	Two-wire serial interface address – The internal location currently being accessed by the two-wire serial interface is displayed here. This register is provided for diagnostic purposes.
15:5	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
4	RELOAD	RW	0	Reload EEPROM – When this bit is set the SerialStat.Done bit is automatically cleared and the EEPROM values are reloaded via the two-wire serial interface. This bit is self-clearing.
3	DONE	RWU	0	Two-wire serial interface download done – This bit is set by hardware to indicate the completion of the serial EEPROM download. This bit is also set if no EEPROM is detected.
2	TIMINGER	RU	0	Two-wire serial interface timing error – This flag is set by hardware when an expected two-wire serial interface acknowledge is not received.
1	CKSUMER	RU	0	Two-wire serial interface checksum error – This flag is set by hardware when the internally generated checksum does not match the checksum read from the EEPROM.
0	NOEEPROM	RU	PIN	No EEPROM detected – The state of the SCL line is sampled on power up. If the line is sampled LOW, the NOEEPROM bit is set by hardware.

0x020 Serial Stat 1 − Two−Wire Serial Interface Data				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:0	SERIALDATA	RU	0	Two-wire serial interface data – The current quadlet provided by the two-wire serial interface module is provided here. This register is provided for diagnostic purposes.

0x024 SRST – Software Generated Chip Reset				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:0	SOFTRESET	R0W	0	Software reset − A write to the software reset register results in a global synchronous reset. All storage elements in the device, including configuration registers is reset to initial conditions. If an EEPROM is present, the EEPROM download commences following the software reset.

6.3 Link Layer Controller CFR Map



6.3.1 Link CFR Bit Descriptions

0x040 LCTRL – Link Control				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:27	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
26	TXEN	RW	0	Transmit enable – When TXEN is cleared, the transmitter does not arbitrate or send packets. The TXEN bit is cleared by a 1394 bus reset and transmit traffic is interrupted. This bit must be set to 1 for packet transmissions to resume following an IEEE-1394 bus reset.
25	RXEN	RW	1	Receive enable – When RXEN is cleared, the receiver does not receive any packets. This bit is not affected by an IEEE-1394 bus reset.

0x040 LCTRL – Link Control (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
24	ACCELEN	RW	0	Acceleration enable – When this bit is set, fly-by acceleration and accelerated arbitration are enabled. This bit cannot be set while TXEN and RXEN are set. This bit may only be set to 1 when an IEEE-1394.a capable PHY is used.
23	CONCATEN	RW	0	Concatenation enable – When set to 1, the link may concatenate multiple isochronous or asynchronous packets. This bit may only be set to 1 when an IEEE-1394.a capable PHY is used.
22	EN_IDLE_INSRT	RW	1	Enable idle cycle insertion – When this bit is set, the link layer inserts one idle state(00) on the PHY/link interface CTL lines between the PHY transmit state(10) and the link transmit state(11) as indicated in the IEEE-1394.a standard. When this bit is not set, the interface conforms to the signaling specified in the IEEE-1394-1995 specification and an idle state is not inserted.
21	RESETTX	RW	0	Reset transmitter – Writing a 1 to this bit resets all state machines in the link layer that are involved in transmitting a packet. This bit is self-clearing.
20	RESETRX	RW	0	Reset receiver – Writing a 1 to this bit resets all state machines in the link layer that are involved in receiving a packet. This bit is self-clearing.
19	CONTENDEROUT	RW	1	Contender output – The value written to this register is driven on the PLI_CNTDR terminal when the pin is configured as an output in SYSCFR.PINCFG register.
18:16	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
15	BUSNRST	RW	0	BUS number reset enable – When this enable bit is set, the bus number field is reset to 0x3FF when a local bus reset is detected.
14	ENLONGHLD	RW	0	Enable long hold – Writing a 1 to this location causes the IEEE-1394 acknowledge to be delayed to for the maximum allowable time before being sent.
13:12	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
11	CYCMASTER	RWU	0	Cycle master – When this bit is set and the device is attached to the root PHY, the cycle master function is enabled. When the cycle_count field of the cycle timer register increments, the transmitter sends a cycle-start packet. This bit is automatically cleared by hardware when a cycle-too-long event is detected according to the IEEE-1394.a specification. The value in this register cannot be overwritten if CMAUTO is set to 1.
10	CYCTOOLONGDIS	RW	0	Cycle too long disable – When this bit is set, the CYCMASTER bit is not cleared in response to a cycle too long event as defined in the IEEE-1394.a specification.
9	CYCTIMEREN	RW	0	Cycle timer enable – The cycle timer is enabled to count when this bit is set to 1. The cycle timer is disabled when the bit is set to 0.
8	CLSIDER	R0W	0	Clear self-ID error – When CLSIDER is set, the self-ID error code bits are reset to the no error condition.
7	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.

0x040 LCTRL – Link Control (Continued)					
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**	
6:4	SIDERRCODE	RU	0	Self-ID error code − contains the error code of the first self-ID error. The errors are encoded as follows:	
				000	No error
				001	Last self-ID received was not all child ports
				010	Received PHY ID in self-ID was not as expected
				011	Quadlet not inverted (phase error)
				100	PHY ID sequence error (two or more gaps in IDs)
				101	PHY ID sequence error (large gap in IDs)
				110	PHY ID error within packet
				111	Quadlet not the inversion of the prior quadlet
3	CMAUTO	RW	0	Cycle master automatic set – When CMAUTO is set high, the device automatically enables CYCMASTER when this node becomes the root following a bus reset.	
2:0	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.	

0x044 LINT – Link Interrupts				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:22	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
21	HDRERR	RCU	0	Header error – This bit is set when the receiver detects a CRC error in the header of a packet that may have been addressed to this node. An interrupt is generated when the corresponding enable bit in LINTEN is set. Write 1 to clear.
20	SIDERR	RCU	0	Self-ID error – This bit is set to 1 to indicate that a self ID packet with errors has been received. An interrupt is generated when the corresponding enable bit in LINTEN is set. Write 1 to clear.
19	ISOARBFAIL	RCU	0	Isochronous arbitration failed – When set to 1, the isochronous transmit request to send an isochronous packet failed to win bus arbitration. An interrupt is generated when the corresponding enable bit in LINTEN is set. Write 1 to clear.
18	CYCTOOLONG	RCU	0	Cycle too long – This bit is set by hardware when a cycle has exceeded the maximum allowable time. The hardware simultaneously clears the LCTRL.CYCMASTER bit when setting this bit. An interrupt is generated when the corresponding enable bit in LINTEN is set. Write 1 to clear.
17	CYCLOST	RCU	0	Cycle lost – When set to 1, the cycle timer has rolled over twice without the reception of a cycle start packet. This occurs only when this node is not cycle master. An interrupt is generated when the corresponding enable bit in LINTEN is set. Write 1 to clear.
16	CYCARBFAIL	RCU	0	Cycle arbitration failed – When this bit is set to 1, cycle arbitration has failed. An interrupt is generated when the corresponding enable bit in LINTEN is set. Write 1 to clear.
15:11	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
10	PHYINT	RCU	0	PHY interrupt – When this bit is set to 1, the PHY has signaled an interrupt through the PHY interface. An interrupt is generated when the corresponding enable bit in LINTEN is set. Write 1 to clear.
9	PHYREGRX	RCU	0	PHY register received – When set to 1, a register value has been transferred to the PHY access register from the PHY interface. An interrupt is generated when the corresponding enable bit in LINTEN is set. Write 1 to clear.

0x044 LINT – Link Interrupts (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
8	PHYBUSRST	RCU	0	PHY bus reset – When this bit is set to 1, the PHY has entered the 1394 bus reset state. An interrupt is generated when the corresponding enable bit in LINTEN is set. Write 1 to clear.
7	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
6	CYCSEC	RCU	0	Cycle seconds – When set to 1, the cycle seconds field in the cycle timer register has incremented. An interrupt is generated when the corresponding enable bit in LINTEN is set. Write 1 to clear.
5	CYCSTART	RCU	0	Cycle start – When set to 1, the link transmitter has sent or the link receiver has received a cycle start packet. An interrupt is generated when the corresponding enable bit in LINTEN is set. Write 1 to clear.
4	CYCDONE	RCU	0	Cycle done – When set to 1, a subaction gap has been detected on the bus after the transmission or reception of a cycle start packet. An interrupt is generated when the corresponding enable bit in LINTEN is set. Write 1 to clear.
3:2	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
1	ARBRSTGAP	RCU	0	Arbitration reset gap – This bit is set to 1 when an arbitration reset gap has been detected. An interrupt is generated when the corresponding enable bit in LINTEN is set. Write 1 to clear.
0	SUBACTGAP	RCU	0	Subaction gap – This bit is set to 1 when a subaction gap has been detected. An interrupt is generated when the corresponding enable bit in LINTEN is set. Write 1 to clear.

0x048 LINTEN – Link Interrupt Enables				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:22	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
21	HDRERR	RW	0	Header error interrupt enable– When this bit is set to 1, the SYSINT.LLCINT1 bit is set to 1 when the corresponding bit in the LINT register is set by hardware. When set to 0, the corresponding bit in the LINT register has no effect on the SYSINT.LLCINT1 bit.
20	SIDERR	RW	0	Self ID error interrupt enable – When this bit is set to 1, the SYSINT.LLCINT1 bit is set to 1 when the corresponding bit in the LINT register is set by hardware. When set to 0, the corresponding bit in the LINT register has no effect on the SYSINT.LLCINT1 bit.
19	ISOARBFL	RW	0	Isochronous arbitration failed interrupt enable – When this bit is set to 1, the SYSINT.LLCINT1 bit is set to 1 when the corresponding bit in the LINT register is set by hardware. When set to 0, the corresponding bit in the LINT register has no effect on the SYSINT.LLCINT1 bit.
18	CYCTOOL-ONG	RW	0	Cycle too long interrupt enable − When this bit is set to 1, the SYSINT.LLCINT1 bit is set to 1 when the corresponding bit in the LINT register is set by hardware. When set to 0, the corresponding bit in the LINT register has no effect on the SYSINT.LLCINT1 bit.
17	CYCLOST	RW	0	Cycle lost interrupt enable – When this bit is set to 1, the SYSINT.LLCINT1 bit is set to 1 when the corresponding bit in the LINT register is set by hardware. When set to 0, the corresponding bit in the LINT register has no effect on the SYSINT.LLCINT1 bit.
16	CYCARBFAIL	RW	0	Cycle arbitration failed interrupt enable – When this bit is set to 1, the SYSINT.LLCINT1 bit is set to 1 when the corresponding bit in the LINT register is set by hardware. When set to 0, the corresponding bit in the LINT register has no effect on the SYSINT.LLCINT1 bit.
15:11	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.

0x048 LINTEN – Link Interrupt Enables (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
10	PHYINT	RW	0	PHY interrupt enable – When this bit is set to 1, the SYSINT.LLCINT0 bit is set to 1 when the corresponding bit in the LINT register is set by hardware. When set to 0, the corresponding bit in the LINT register has no effect on the SYSINT.LLCINT0 bit.
9	PHYREGRX	RW	0	PHY register received interrupt enable –When this bit is set to 1, the SYSINT.LLCINT0 bit is set to 1 when the corresponding bit in the LINT register is set by hardware. When set to 0, the corresponding bit in the LINT register has no effect on the SYSINT.LLCINT0 bit.
8	PHYBUSRST	RW	0	PHY bus reset interrupt enable – When this bit is set to 1, the SYSINT.LLCINT0 bit is set to 1 when the corresponding bit in the LINT register is set by hardware. When set to 0, the corresponding bit in the LINT register has no effect on the SYSINT.LLCINT0 bit.
7	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
6	CYCSEC	RW	0	Cycle seconds interrupt enable – When this bit is set to 1, the SYSINT.LLCINT0 bit is set to 1 when the corresponding bit in the LINT register is set by hardware. When set to 0, the corresponding bit in the LINT register has no effect on the SYSINT.LLCINT0 bit.
5	CYCSTART	RW	0	Cycle start interrupt enable – When this bit is set to 1, the SYSINT.LLCINT0 bit is set to 1 when the corresponding bit in the LINT register is set by hardware. When set to 0, the corresponding bit in the LINT register has no effect on the SYSINT.LLCINT0 bit.
4	CYCDONE	RW	0	Cycle done interrupt enable – When this bit is set to 1, the SYSINT.LLCINT0 bit is set to 1 when the corresponding bit in the LINT register is set by hardware. When set to 0, the corresponding bit in the LINT register has no effect on the SYSINT.LLCINT0 bit.
3:2	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
1	ARBRSTGAP	RW	0	Arbitration reset gap interrupt enable – When this bit is set to 1, the SYSINT.LLCINT0 bit is set to 1 when the corresponding bit in the LINT register is set by hardware. When set to 0, the corresponding bit in the LINT register has no effect on the SYSINT.LLCINT0 bit.
0	SUBACTGAP	RW	0	Sub action gap interrupt enable – When this bit is set to 1, the SYSINT.LLCINT0 bit is set to 1 when the corresponding bit in the LINT register is set by hardware. When set to 0, the corresponding bit in the LINT register has no effect on the SYSINT.LLCINT0 bit.

0x04C LCYCTIM – Link Cycle Timer				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:25	CYCSEC	RWU	0	Cycle seconds – 1-Hz cycle timer counter. This counter increments whenever the LCYCTIM.CYCNUMBER field rolls over from 7999 to 0.
24:12	CYCNUMBER	RWU	0	Cycle number – 8-kHz cycle timer. This counter increments whenever LCYCTIM.CYCOFFSET rolls over from 3071 to 0.
11:0	CYCOFFSET	RWU	0	Cycle offset – This field counts from 0 to 3071 and rolls over once every 125 µs.

0x054 PHYACC – PHYAccess				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	RREG	RW	0	Read PHY register – When set, the device sends a read register request with the address equal to the PHYACC.PHYRGAD field to the PHY. This bit is cleared when the request is sent.
30	WRREG	RW	0	Write PHY register – When set, the device sends a write register request with the address equal to the PHYACC PHYRGAD field and data equal to the PHYACC.PHYRGDATA field to the PHY. This bit is cleared when the request is sent.
29:28	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
27:24	PHYREGADDR	RW	0	PHY register address – This is the address used for PHY register read and write operations.
23:16	PHYREGDATA	RW	0	PHY register data – This value provides the data to be written to the PHY in PHY-register write requests.
15:12	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
11:8	PHYRXADDR	RWU	0	PHY address received – The address of the PHY register most recently received.
7:0	PHYRXDATA	RWU	0	PHY receive data – The data from the PHY register indicated by PHYACC.PHYRXAD.

0x058 BRD – Bus Reset Data				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	BUSINFOVALID	RU	0	Bus information valid − Indicates that the node ID, IRM node ID, node count, and root information are valid when set.
30	RSVD	R	0	Reserved – A write to this location has no effect. A read returns 0.
29:24	NODECNT	RU	0	Node count – Contains the number of nodes detected in the system.
23	ROOT	RU	0	Node is root − Root is set when the current node is the root node. This bit is read-only.
22	CONTENDER	U	PIN	Contender – Contains the status of the PLI_CNTDR pin.
21:16	IRMNODEID	RU	3F	IRM node ID – This is the isochronous resource manager node identification. If there is no IRM node present on the bus, these bits are equal to 0x3F.
15:6	BUSNUMBER	RU	3FF	Bus number – This is the 10-bit IEEE-1212 bus number. These bits are set to 0x3FF when RBUSNUM is set and there is a bus reset.
5:0	NODENUMBER	RU	3F	Node number – This is the 6-bit IEEE-1212 node number. These bits are set to 0x3F at power-on reset or when a bus reset status response is received by the link.

0x05C MAINT_CTL – Maintenance Control				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	I_HCRC	RWU	0	Inject header CRC error – When this bit is set, a CRC error is generated in the header of the next transmitted packet. After the next packet is transmitted, this bit is cleared by hardware.
30	I_DCRC	RWU	0	Inject DATA CRC error – When this bit is set, a CRC error is generated in the payload of the next transmitted packet. After the next packet is transmitted, this bit is cleared by hardware.
29	NO_PKT	RWU	0	No packet – Setting this bit to 1 causes the next primary packet to be discarded without being sent. After the next packet is transmitted, this bit is cleared by hardware.
28	F_ACK	RWU	0	Force ACK – If this bit is set, the value of the 8-bit ACK field is used for the next ACK generated by this device. After the next packet is transmitted, this bit is cleared by hardware.
27	NO_ACK	RWU	0	No ACK – When this bit is set by hardware, ACK is not transmitted by the device. After the next packet is transmitted, this bit is cleared by hardware.
26:24	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
23:16	ACK	RW	0	ACK – This field contains the 8-bit acknowledge packet to be transmitted when the F_ACK bit is set.
15:8	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
7:0	PINGVALUE	RU	0	Ping timer value – This value reflects the time it takes a node to respond to a ping packet. The granularity of this timer is 40 ns.

6.4 High-Speed Data Interface A CFR Map

Address	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	HSDI CFR Name (Hex Reset Value)
080h	HSDIARST	HSDIAEN													SIF	SCCEN	RESERVED	SYNCMODE		DirecTV™130_PID	RELEASE DATA	BYTEENDIAN	SERBITENDIAN	SERIALMODE	HSDIA_BUFFERS								HSDIA_CFG0 (0000_0003h)
084h																		RXMULTISTREAM		TXMULTISTREAM					TXDBCTREND								HSDIA_CFG1 (0000_0000h)
088h																								INSRTCMPLT								TXOVERRUN	HSDIA_INT (0000_0000h)
08Ch																								INSRTCMPLT								TXOVERRUN	HSDIA_INTEN (0000_0000h)
090h	PIDA_MASK																																PIDA_MASK (0000_0000h)
094h		PID7BUF				PID6BUF				PID5BUF				PID4BUF				PID3BUF				PID2BUF				PID1BUF				PID0BUF			PIDA_ADDRFLTR0 (0000_0000h)
098h		PID15BUF				PID14BUF				PID13BUF				PID12BUF				PID11BUF				PID10BUF				PID9BUF				PID8BUF			PIDA_ADDRFLTR1 (0000_0000h)
09Ch	PIDA_FLTRACC																																PIDA_FLTRACC (0000_0000h)
0A0h																	RDPTR				WRPTR					WRBUF			PIDFLTR_RST		PIDFLTR_EN		PIDA_CSR (0000_0000h)
0A4h	INSBUFA_ACC																																INSBUFA_ACC (xxxx_xxxxh)
0A8h		WRPTR_RST	WRPTR							RDPTR_RST	RDPTR										INSRT_BUF			AUTOFILL	PKTINSRT_EN	PKTSIZE							INSBUFA_CSR0 (0000_0000h)
0ACh																	OFPT																	INSBUFA_CSR1 (0000_0000h)
0B0-0BFh																	RESERVED																	RSVD (0000_0000h)

6.4.1 HSDI A Bit Descriptions

0x080 HSDIA_CFG0 – HSDIA Configuration 0				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	HSDIARST	R0W	0	HSDIA reset – Writing a 1 to this location causes all state machines in the high speed data interface to synchronously reset. This bit is automatically cleared by hardware.
30	HSDIAEN	RW	0	HSDIA enable − When set to 0, the HSDI ignores all interface signaling.
29:18	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
17	SIF	RW	0	DirecTV 130 SIF – The value written to this field is inserted as the SIF (time stamp invalid flag) field in all DirecTV 130 cells written into the HSDI. Packets inserted by the packet insert hardware have a SIF field of 1 regardless of the setting of this bit.
16	SCCEN	RW	0	DirecTV system clock counter enable – When this bit is set to 1, the 23-bit system clock counter runs as a free running linear counter. When this bit is set to 0, the system clock counter is set to all 0s. Enabling this feature requires that one GPIO pin be configured as the DirecTV system clock input.
15	RSVD	RW	0	Reserved − This bit is reserved for internal tests. It should be set to 0 (default) for correct operation.
14:13	SYNCMODE	RW	0	00 = Sync mode A 01 = Sync mode B 10 = Sync Mode C 11 = Reserved
12	DSS130_PID	RW	0	DirecTV 130 used with PID filtering – This bit must be set to 1 if DirecTV 130 streams are used in conjunction with the PID filter on this interface. If DSS130 streams are used with the PID filter, only DirecTV 130 streams are supported for this interface. Other stream types can be mixed as desired when using the PID filter.

0x080 HSDIA_CFG0 – HSDIA Configuration 0 (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
11	RELEASE_DATA	RW	0	Release data mode − When this bit is enabled (set to 1), ceLynx cannot output DV Data to the HSDI, until the following sequence is performed: 1. HSDI_AV active 2. DV frame out (a GPIO pin) goes active indicating the frame time stamp has expired. 3. The application activates the DV-frame-in signal (a GPIO pin). 4. The HSDI_EN signal is activated. The sequence is reset when the buffer is emptied.
10	BYTEENDIAN	RW	0	Byte endian mode – This bit indicates which byte of each 4-byte data quadlet is presented first at the HSDI. Irrespective of direction, the byte-wise data presented at the HSDI composes a quadlet of data as follows: D[7:0] First byte = AB Second byte = CD Third byte = EF Fourth byte = 01 BYTEENDIAN = 0 Resulting quadlet = ABCDEF01 BYTEENDIAN = 1 Resulting quadlet = 01EFCDAB
9	SERBITENDIAN	RW	0	Serial bit endianess – This bit determines the order in which bits are received when the HSDI is configured for serial mode. This bit has no effect when the HSDI data port is configured for 8-bit mode. For example, if the following sequence is presented at the HSDI in serial mode: D[0] First Last 0−1−0−1−0−1−0−1 SERBITENDIAN = 0 Resulting byte = 0x55 SERBITENDIAN = 1 Resulting byte = 0xAA
8	SERIALMODE	RW	0	HSDIA serial mode − When set to 1, the HSDIA is in serial mode, using HSDIA_D0 as the serial data pin.
7:0	HSDIA_BUFFERS	RW	3	HSDIA buffer mapping – The bits in this register correspond to the buffer addresses mapped to this interface. For example, a 1 in bit location 0 indicates that buffer 0 is mapped to this HSDI, a 0 in the same location indicates that buffer 0 is not mapped to this HSDI. By default, buffers 0 and 1 are mapped to HSDIA.

0x084 HSDIA_CFG1 – HSDIA Configuration 1				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:15	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
14	RXMULTISTREAM	RW	0	Receive multiple streams – Setting this bit to 1 causes the HSDI to present data at the interface from the buffer selected by the 3-bit HSDIA address bus. When set to 0 the HSDI retrieves data from the receive buffer indicated by HSDI_BUFFERS.
13	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
12	TXMULTISTREAM	RW	0	Transmit multiple streams – Setting this bit to 1 causes the HSDI to present data at the interface from the buffer selected by the 3-bit HSDIA address bus. When set to 0, the HSDI places the data into the buffer indicated by HSDI_BUFFERS
11:0	TXDBCNTREND	RW	0	Transmit data block counter end – The binary encoded value written to this register determines the size of the data blocks presented at the HSDI when sync mode A or B is used. Values written to this register have no effect when syncmode C is used. This is programmed in terms of hex bytes.

0x088 HSDIA_INT – HSDIA Interrupts				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:9	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
8	INSRTCMPLT	RCU	0	Packet insertion complete – This interrupt indicates that a packet has been inserted into the transport stream by the packet insertion hardware. The packet insert hardware has been automatically disabled when this bit is set and must be re-enabled by software before packets can be inserted into the transport stream.
7:1	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
0	TXOVERRUN	RCU	0	Transmit overrun – This interrupt indicates that the HSDI input buffer has been overrun by the application and data has been lost.

0x08C HSDIA_INTEN – HSDIA Interrupt Enables				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:9	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
8	INSRTCMPLT	RW	0	Packet insertion complete interrupt enable – When this bit is set to 1, the SYSINT.HSDIAINT bit is set to 1 when the corresponding bit in the HSDIA_INT register is set by hardware. When set to 0, the corresponding bit in the HSDIA_INT register has no effect on the SYSINT.HSDIAINT bit.
7:1	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
0	TXOVERRUN	RW	0	Transmit overrun interrupt enable – When this bit is set to 1, the SYSINT.HSDIAINT bit is set to 1 when the corresponding bit in the HSDIA_INT register is set by hardware. When set to 0, the corresponding bit in the HSDIA_INT register has no effect on the SYSINT.HSDIAINT bit.

0x090 PIDA_MASK – HSDIA PID Filter Mask				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:0	PIDA_MASK	RW	0	PID filter mask value – Bit locations set to 1 indicate bits that are used for PID matching operations. For example, if all locations in this register are set to 1, all 32 bits are used for PID compare. If all bits are set to 0, no bits are used for PID compare and all PIDs are transmitted.

0x094 PIDA_ADDRFLTR0 – HSDIA PID Filter Address Mapping				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
30:28	PID7BUF	RW	0	PID location 7 buffer map – When the PID filter is enabled and PID filter location 7 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
27	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
26:24	PID6BUF	RW	0	PID location 6 buffer map – When the PID filter is enabled and PID filter location 6 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
23	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
22:20	PID5BUF	RW	0	PID location 5 buffer map – When the PID filter is enabled and PID filter location 5 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
19	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
18:16	PID4BUF	RW	0	PID location 4 buffer map – When the PID filter is enabled and PID filter location 4 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
15	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
14:12	PID3BUF	RW	0	PID location 3 buffer map – When the PID filter is enabled and PID filter location 3 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
11	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
10:8	PID2BUF	RW	0	PID location 2 buffer map – When the PID filter is enabled and PID filter location 2 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
7	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
6:4	PID1BUF	RW	0	PID location 1 buffer map – When the PID filter is enabled and PID filter location 1 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
3	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
2:0	PID0BUF	RW	0	PID location 0 buffer map – When the PID filter is enabled and PID filter location 0 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.

0x098 PIDA_ADDRFLTR1 – HSDIA PID Filter Address Mapping				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
30:28	PID15BUF	RW	0	PID location 15 buffer map – When the PID filter is enabled and PID filter location 15 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
27	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
26:24	PID14BUF	RW	0	PID location 14 buffer map – When the PID filter is enabled and PID filter location 14 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
23	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
22:20	PID13BUF	RW	0	PID location 13 buffer map – When the PID filter is enabled and PID filter location 13 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
19	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
18:16	PID12BUF	RW	0	PID location 12 buffer map – When the PID filter is enabled and PID filter location 12 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
15	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
14:12	PID11BUF	RW	0	PID location 11 buffer map – When the PID filter is enabled and PID filter location 11 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
11	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
10:8	PID10BUF	RW	0	PID location 10 buffer map – When the PID filter is enabled and PID filter location 10 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
7	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
6:4	PID9BUF	RW	0	PID location 9 buffer map – When the PID filter is enabled and PID filter location 9 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
3	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
2:0	PID8BUF	RW	0	PID location 8 buffer map – When the PID filter is enabled and PID filter location 8 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.

0x09C PIDA_FLTRACC – PID A FILTER Access				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:0	PIDA_FLTRACC	RW	0	PID filter access register – When the PID filter is not enabled, a write to this register results in an update to the PID filter location displayed in PIDA_CSR.WRPTR. When the PID filter is enabled, writes to this register have no effect. A read from this register returns the data from the PID filter location indicated by PIDA_CSR.RDPTR.

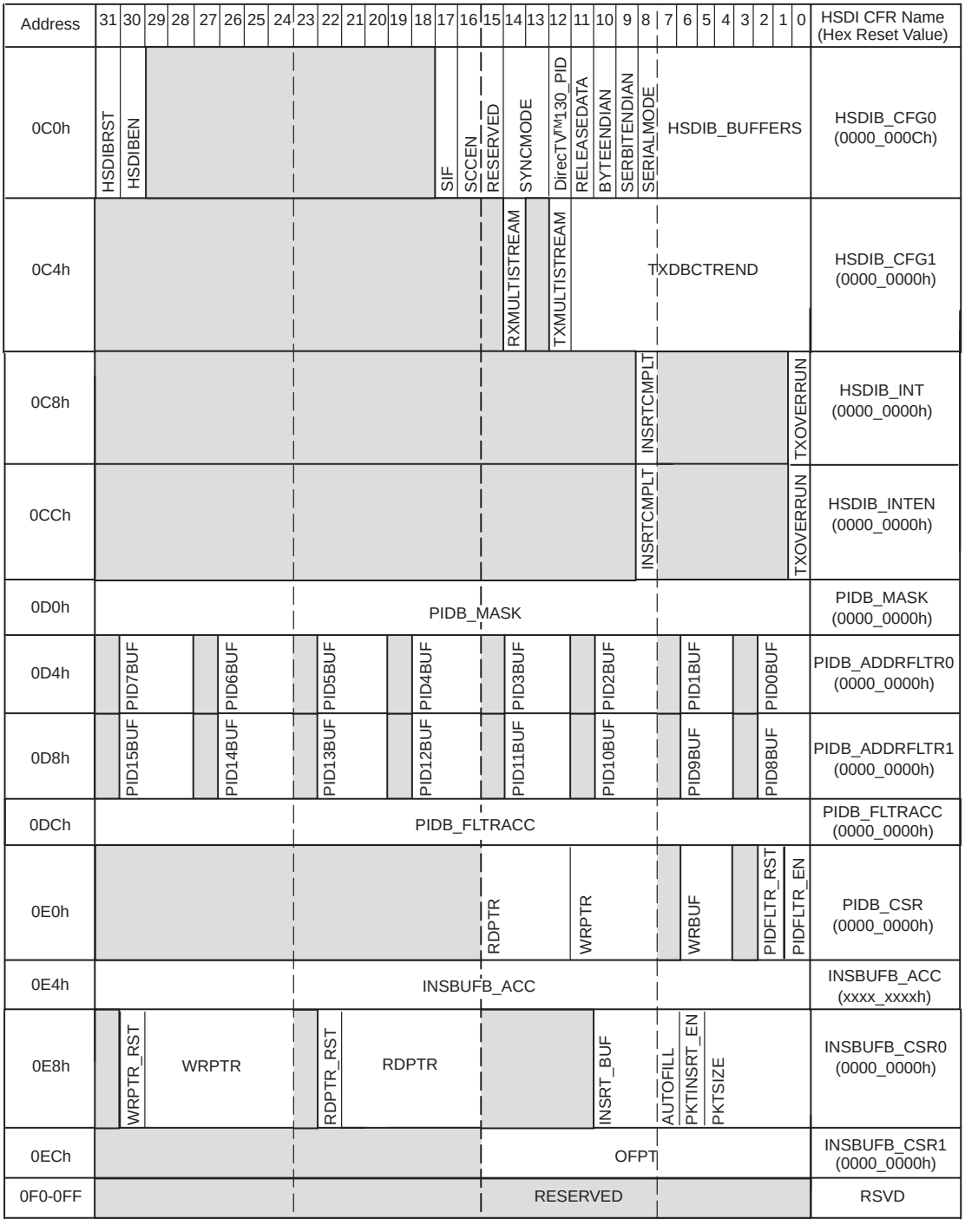
0x0A0 PIDA_CSR – PID A Filter Configuration and Status				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:16	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
15:12	RDPTR	RU	0	PID filter read pointer – The value displayed in this register indicates the register currently accessible for read access via the microcontroller interface. When the PID filter is not enabled, a read access to the PIDA_FLTRACC register causes the read pointer to increment by 1. Enabling the PID filter resets the RDPTR to 0. The read pointer is not affected by reads while the PID filter is enabled.
11:8	WRPTR	RU	0	PID filter write pointer – The value displayed in this register indicates the PID filter location that is accessed by the next microcontroller write. When the PID filter is not enabled, a write to The PIDA_FLTRACC register causes the write pointer to increment by 1.
7	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
6:4	WRBUF	RU	0	PIDA write buffer − Transport streams that are selected by the PID filter are routed to one of the eight data buffers as mapped in this register.
3:2	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
1	PIDFLTR_RST	R0	0	PID filter reset – When this bit is set to 1, all of the PID filter comparison values are set to 0. The read and write pointers are also set to 0.
0	PIDFLTR_EN	RW	0	PID filter enable – Writing a 1 to this location enables the PID filter feature. When enabled, only transport streams with PID fields that match the values programmed into the PID filter are written to the transmit buffer. When disabled, the PID filter has no effect on transport streams.

0x0A4 INSBUFA_ACC – Packet Insertion Buffer A Access				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:0	INSBUFA_ACC	RW	X	Insertion buffer A access – This register provides the access port to the insertion packet storage RAM. When packet insertion is not enabled, the microcontroller can write the insertion packet into the insertion RAM by accessing this register. Writes to this register result in an update to the memory location indicated by INSBUFA_CSR0.WRPTR. Writes to this location, prior to enabling the packet insertion feature, cause the write pointer to increment by 1. When the insertion feature is enabled, access to this register has no effect. The RAM is not initialized at reset.

0x0A8 INSBUFA_CSR0 – Insertion Buffer A Configuration and Status 0				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
30	WRPTR_RST	R0WU	0	Insertion buffer write pointer reset – When the packet insertion feature is disabled, writing a 1 to this location causes the insertion buffer write pointer to be set to 0. When the packet insertion feature is enabled, access to this bit has no effect. This bit is self-clearing.
29:24	WRPTR	RU	0	Insertion buffer write pointer – This read only value indicates the next location that is updated by a write access to INSBUFA_ACC. When the packet insertion feature is disabled, writes to INSBUFA_ACC cause this field to increment.
23	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
22	RDPTR_RST	R0WU	0	Insertion buffer read pointer reset – When the packet insertion feature is disabled, writing a 1 to this location causes the insertion buffer read pointer to be set to 0. When the packet insertion feature is enabled, access to this bit has no effect. This bit is self-clearing.
21:16	RDPTR	RU	0	Insertion buffer read pointer – This read-only value indicates the next location that is returned by a read access to INSBUFA_ACC. When the packet insertion feature is enabled, this field reflects the current insertion buffer location being accessed by hardware.
15:11	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
10:8	INSRT_BUF	RW	0	Insertion buffer mapping – When the packet insertion feature is used, this field must be written by software to indicate which of the eight highly configurable data buffers to place the insertion packet in.
7	AUTOFILL	R0W	0	Auto fill – Writing a 1 in this location causes all locations in the insertion buffer starting from the address indicated by INSBUFA_CSR0.WRPTR to be filled with 0xFFFF FFFF.
6	PKTINSRT_EN	RWU	0	Packet insertion enable – Writing a 1 to this location enables the packet insertion feature. All packet insertion related configurations must be complete prior to setting this bit. This bit is cleared by hardware in the event of a successful packet insertion event. Setting this bit causes the insertion buffer read/write pointers to reset to 0.
5:0	PKTSIZE	RW	0	Packet size – Software must update this field with the size of the inserted packet in quadlets.

0x0AC INSBUFA_CSR1 – Insertion Buffer A Configuration and Status 1				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:16	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
15:0	OFPT	RW	0	Offset packet time – If enabled, the link inserts a packet into the IEEE-1394 isochronous stream if a gap exists in the transport stream equal to or greater than the value of OFPT. The format is identical to the IEEE-1394 cycle timer: bits 15:12 cycle count bits 11:0 cycle offset For a transport stream with HSDIx_CLK of 3 MHz, a gap length to insert 188 bytes is computed as follows: 188 bytes/3 MHz = 62.5 µs cycle count = (0 × 125 µs) = 0h cycle offset = (62.5 µs/25 ns) = 9CAh OFPT = 0000_09CAh

6.5 High-Speed Data Interface B CFR Map



6.5.1 HSDI B Bit Descriptions

0x0C0 HSDIB_CFG0 – HSDIB Configuration 0				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	HSDIBRST	R0WU	0	HSDIB reset – Writing a 1 to this location causes all state machines in the high-speed data interface to synchronously reset. This bit is automatically cleared by hardware.
30	HSDIBEN	RW	0	HSDIB enable − When set to 0, the HSDI ignores all interface signaling.
29:18	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
17	SIF	RW	0	DirecTV 130 SIF – The value written to this field is inserted as the SIF (time-stamp-invalid flag) field in all DirecTV 130 cells written into the HSDI. Packets inserted by the packet insert hardware have an SIF field of 1 regardless of the setting of this bit.
16	SCCEN	RW	0	DirecTV system clock counter enable – When this bit is set to 1, the 23-bit system clock counter runs as a free-running linear counter. When this bit is set to 0, the system clock counter is set to all 0s. Enabling this feature requires that one GPIO pin is configured as the DirecTV system clock input.
15	RSVD	RW	0	Reserved − This bit is reserved for internal tests. It should be set to 0 (default) for correct operation.
14:13	SYNCMODE	RW	0	00 = Sync mode A 01 = Sync mode B 10 = Reserved 11 = Sync mode C
12	DSS130_PID	RW	0	DirecTV 130 used with PID filtering – This bit must be set to 1 if DirecTV 130 streams are used in conjunction with the PID filter on this interface. If DirecTV 130 streams are used with the PID filter, only DirecTV 130 streams are supported for this interface. Other stream types can be mixed as desired when using the PID filter.
11	RELEASE_DATA	RW	0	Release data mode − When this bit is enabled (set to 1), ceLynx cannot output DV data to the HDSI until the following sequence is performed: 1. HSDI_AV signal active 2. DV frame-out signal (GPIO pins) goes active indicating the frame time stamp has expired. 3. The application activates the DV frame-in signal (a GPIO pin). 4. The HSDI_EN signal is activated. The sequence is reset when the buffer is emptied.
10	BYTEENDIAN	RW	0	Byte endian mode – This bit indicates which byte of each 4-byte data quadlet is presented first at the HSDI. Irrespective of direction, the byte-wise data presented at the HSDI composes a quadlet of data as follows: D[7:0] First byte = AB Second byte = CD Third byte = EF Fourth byte = 01 BYTEENDIAN = 0 Resulting quadlet = 0xABCD EF01 BYTEENDIAN = 1 Resulting quadlet = 0x01EF CDAB

0x0C0 HSDIB_CFG0 – HSDIB Configuration 0 (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
9	SERBITENDIAN	RW	0	Serial bit endianess – This bit determines the order in which bits are received when the HSDI is configured for serial mode. This bit has no effect when the HSDI data port is configured for 8-bit mode. For example, if the following sequence is presented at the HSDI in serial mode: D[0] First Last 0−1−0−1−0−1−0−1 SERBITENDIAN = 0 Resulting byte = 0x55 SERBITENDIAN = 1 Resulting byte = 0xAA
8	SERIALMODE	RW	0	HSDIB serial mode − When set to 1, the HSDIB is in serial mode, using HSDIB_D0 as the serial data pin.
7:0	HSDIB_BUFFERS	RW	C	HSDIB buffer mapping – The bits in this register correspond to the buffer addresses mapped to this interface. For example a 1 in bit location 0 indicates that buffer 0 is mapped to this HSDI, a 0 in the same location indicates that buffer 0 is not mapped to this HSDI. By default, buffers 2 and 3 are mapped to HSDI-B.

0x0C4 HSDIB_CFG1 – HSDIB Configuration 1				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:15	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
14	RXMULTISTREAM	RW	0	Receive multiple streams – Setting this bit to 1 causes the HSDI to present data at the interface from the buffer selected by the 3-bit HSDIB address bus. When set to 0, the HSDI retrieves data from the receive buffer indicated by HSDI_BUFFERS.
13	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
12	TXMULTISTREAM	RW	0	Transmit multiple streams – Setting this bit to 1 causes the HSDI to present data at the interface from the buffer selected by the 3-bit HSDIB address bus. When set to 0, the HSDI places the data into the buffer indicated by HSDI_BUFFERS.
11:0	TXDBCNTREND	RW	0	Transmit data block counter end – The binary encoded value written to this register determines the size of the data blocks presented at the HSDI when sync mode A or B is used. Values written to this register have no effect when syncmode C is used. This is programmed in terms of hex bytes.

0x0C8 HSDIB_INT – HSDIB Interrupts				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:9	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
8	INSRTCMPLT	RCU	0	Packet insertion complete – This interrupt indicates that a packet has been inserted into the transport stream by the packet insertion hardware. The packet insert hardware has been automatically disabled when this bit is set and must be re-enabled by software before packets can be inserted into the transport stream.
7:1	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
0	TXOVERRUN	RCU	0	Transmit overrun – This interrupt indicates that the HSDI input buffer has been overrun by the application and data has been lost.

0x0CC HSDIB_INTEN – HSDIB Interrupt Enables				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:9	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
8	INSRTCMPLT	RW	0	Packet insertion complete interrupt enable – When this bit is set to 1, the SYSINT.HSDIBINT bit is set to 1 when the corresponding bit in the HSDIB_INT register is set by hardware. When set to 0, the corresponding bit in the HSDIB_INT register has no effect on the SYSINT.HSDIBINT bit.
7:1	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
0	TXOVERRUN	RW	0	Transmit overrun interrupt enable – When this bit is set to 1, the SYSINT.HSDIBINT bit ise set to 1 when the corresponding bit in the HSDIB_INT register is set by hardware. When set to 0, the corresponding bit in the HSDIB_INT register has no effect on the SYSINT.HSDIBINT bit.

0x0D0 PIDB_MASK – HSDIB PID Filter Mask				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:0	PIDB_MASK	RW	0	PID filter mask value – Bit locations set to 1 indicate bits that are used for PID matching operations. For example, if all locations in this register are set to 1, all bits are used for PID compare. If all bits are set to 0, no bits are used for PID compare and all PIDs are transmitted.

0x0D4 PIDB_ADDRFLTR0 – HSDIB PID Filter Address Mapping				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
30:28	PID7BUF	RW	0	PID location 7 buffer map – When the PID filter is enabled and PID filter location 7 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
27	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
26:24	PID6BUF	RW	0	PID location 6 buffer map – When the PID filter is enabled and PID filter location 6 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
23	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
22:20	PID5BUF	RW	0	PID location 5 buffer map – When the PID filter is enabled and PID filter location 5 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
19	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
18:16	PID4BUF	RW	0	PID location 4 buffer map – When the PID filter is enabled and PID filter location 4 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
15	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
14:12	PID3BUF	RW	0	PID location 3 buffer map – When the PID filter is enabled and PID filter location 3 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
11	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
10:8	PID2BUF	RW	0	PID location 2 buffer map – When the PID filter is enabled and PID filter location 2 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
7	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
6:4	PID1BUF	RW	0	PID location 1 buffer map – When the PID filter is enabled and PID filter location 1 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
3	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
2:0	PID0BUF	RW	0	PID location 0 buffer map – When the PID filter is enabled and PID filter location 0 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.

0x0D8 PIDB_ADDRFLTR1 – HSDIB PID Filter Address Mapping				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
30:28	PID15BUF	RW	0	PID location 15 buffer map – When the PID filter is enabled and PID filter location 15 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
27	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
26:24	PID14BUF	RW	0	PID location 14 buffer map – When the PID filter is enabled and PID filter location 14 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
23	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
22:20	PID13BUF	RW	0	PID location 13 buffer map – When the PID filter is enabled and PID filter location 13 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
19	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
18:16	PID12BUF	RW	0	PID location 12 buffer map – When the PID filter is enabled and PID filter location 12 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
15	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
14:12	PID11BUF	RW	0	PID location 11 buffer map – When the PID filter is enabled and PID filter location 11 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
11	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
10:8	PID10BUF	RW	0	PID Location 10 Buffer map – When the PID filter is enabled and PID filter location 10 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
7	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
6:4	PID9BUF	RW	0	PID Location 9 Buffer map – When the PID filter is enabled and PID filter location 9 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.
3	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
2:0	PID8BUF	RW	0	PID Location 8 Buffer map – When the PID filter is enabled and PID filter location 8 matches the PID of the incoming data stream, the data is routed into one of eight buffers selected by the binary encoded value written to this location.

0x0DC PIDB_FLTRACC – PID B Filter Access				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:0	PIDB_FLTACC	RW	0	PID filter access register – When the PID filter is not enabled, a write to this register results in an update of the PID filter location displayed in PIDB_CSR.WRPTR. When the PID filter is enabled, writes to this register have no effect. A read from this register returns the data from the PID filter location indicated by PIDB_CSR.RDPTR.

0x0E0 PIDB_CSR – PID B Filter Configuration and Status				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:16	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
15:12	RDPTR	RU	0	PID filter read pointer – The value displayed in this register indicates the register currently accessible for read access via the microcontroller interface. When the PID filter is not enabled, a read access to the PIDB_FLTRACC register causes the read pointer to increment by 1. Enabling the PID filter resets the RDPTR to 0. The read pointer is not effected by reads while the PID filter is enabled.
11:8	WRPTR	RU	0	PID filter write pointer – The value displayed in this register indicates the PID filter location that is accessed by the next microcontroller write. When the PID filter is not enabled, a write to the PIDB_FLTRACC register causes the write pointer to increment by 1. When the PID filter is enabled, the write pointer is reset to 0.
7	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
6:4	WRBUF	RU	0	PIDB write buffer − Transport streams that are selected by the PID filter are routed to one of the eight data buffers as mapped in this register.
3:2	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
1	PIDFLTR_RST	R0	0	PID filter reset – When this bit is set to 1, all of the PID filter comparison values are set to 0. The read and write pointers are also set to 0.
0	PIDFLTR_EN	RW	0	PID filter enable – Writing a 1 to this location enables the PID filter feature. When enabled only transport streams with PID fields that match the values programmed into the PID filter is written to the transmit buffer.

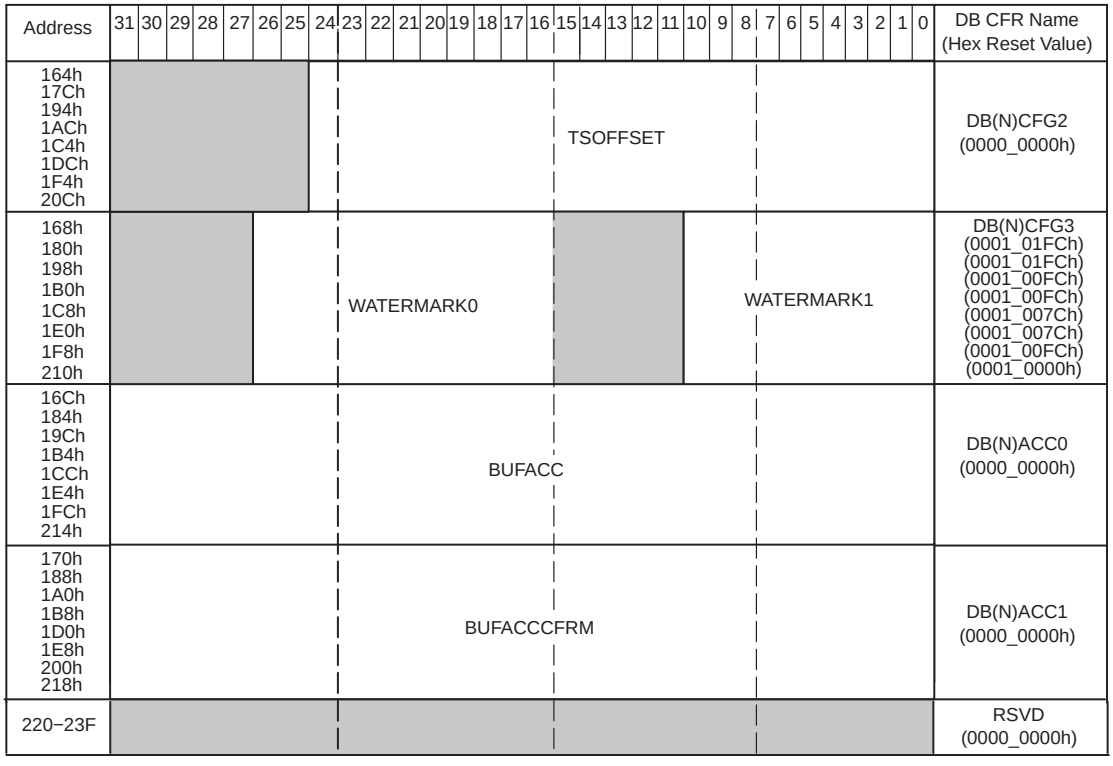
0x0E4 INSBUFB_ACC – Packet Insertion Buffer B Access				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:0	INSBUFB_ACC	RW	X	Insertion buffer B access – This register provides the access port to the insertion packet storage RAM. When packet insertion is not enabled, the microcontroller can write the insertion packet into the insertion RAM by accessing this register. Writes to this register result in an update to the memory location indicated by INSBUFB_CSR0.WRPTR. Writes to this location, prior to enabling the packet insertion feature, cause the write pointer to increment by 1. When the insertion feature is enabled, access to this register has no effect. The RAM is not initialized at reset.

0x0E8 INSBUFB_CSR0 – Insertion Buffer B Configuration and Status 0				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
30	WRPTR_RST	R0WU	0	Insertion buffer write pointer reset – When the packet insertion feature is disabled, writing a 1 to this location causes the insertion buffer write pointer to be set to 0. When the packet insertion feature is enabled, access to this bit has no effect. This bit is self-clearing.
29:24	WRPTR	RU	0	Insertion buffer write pointer – This read-only value indicates the next location that is updated by a write access to INSBUFB_ACC. When the packet insertion feature is disabled, writes to INSBUFB_ACC cause this field to increment.
23	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
22	RDPTR_RST	R0WU	0	Insertion buffer read pointer reset – When the packet insertion feature is disabled, writing a 1 to this location causes the insertion buffer read pointer to be set to 0. When the packet insertion feature is enabled, access to this bit has no effect. This bit is self-clearing.
21:16	RDPTR	RU	0	Insertion buffer read pointer – This read-only value indicates the next location that is returned by a read access to INSBUFB_ACC. When the packet insertion feature is enabled, this field reflects the current insertion buffer location being accessed by hardware.
15:11	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
10:8	INSRT_BUF	RW	0	Insertion buffer mapping – When the packet insertion feature is used, this field must be written by software to indicate which of the eight highly configurable data buffers to place the insertion packet in.
7	AUTOFILL	R0W	0	Auto fill – Writing a 1 in this location causes all locations in the insertion buffer starting from the address indicated by INSBUFB_CSR0.WRPTR to be filled with 0xFFFF FFFF.
6	PKTINSRT_EN	RWU	0	Packet insertion enable – Writing a 1 to this location enables the packet insertion feature. All packet insertion related configurations must be complete prior to setting this bit. This bit is cleared by hardware in the event of a successful packet insertion event. Setting this bit causes the insertion buffer read/write pointers to reset to 0.
5:0	PKTSIZE	RW	0	Packet size – Software must update this field with the size of the inserted packet in quadlets.

0x0EC INSBUFB_CSR1 – Insertion Buffer B Configuration and Status 1				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:16	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
15:0	OFPT	RW	0	Offset packet time – If enabled, the link inserts a packet into the 1394 isochronous stream if a gap exists in the transport stream equal to or greater than the value of OFPT. The format is identical to the 1394 cycle timer: bits 15:12 cycle count bits 11:0 cycle offset For a transport stream with HSDIx_CLK of 3 MHz, a gap length to insert 188 bytes is computed as follows: 188 bytes/3MHz = 62.5 μs cycle count = (0 × 125 μs) = 0h cycle offset = (62.5 μs/25 ns) = 9CAh OFPT = 0000_9CAh

6.6 Data Buffer CFR Map

Address	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DB CFR Name (Hex Reset Value)
140h			BUF7FLSH	BUF7PKTFLSH			BUF6FLSH	BUF6PKTFLSH			BUF5FLSH	BUF5PKTFLSH			BUF4FLSH	BUF4PKTFLSH			BUF3FLSH	BUF3PKTFLSH			BUF2FLSH	BUF2PKTFLSH			BUF1FLSH	BUF1PKTFLSH			BUF0FLSH	BUF0PKTFLSH	DBCTL (0000_0000h)
144h				BUF3WM1	BUF3WM0	BUF3LCELLAV	BUF3FULL	BUF3EMPTY				BUF2WM1	BUF2WM0	BUF2LCELLAV	BUF2FULL	BUF2EMPTY				BUF1WM1	BUF1WM0	BUF1LCELLAV	BUF1FULL	BUF1EMPTY			BUF0WM1	BUF0WM0	BUF0LCELLAV	BUF0FULL	BUF0EMPTY	DBSTAT0 (0909_0909h)
148h				BUF7WM1	BUF7WM0	BUF7LCELLAV	BUF7FULL	BUF7EMPTY				BUF6WM1	BUF6WM0	BUF6LCELLAV	BUF6FULL	BUF6EMPTY				BUF5WM1	BUF5WM0	BUF5LCELLAV	BUF5FULL	BUF5EMPTY			BUF4WM1	BUF4WM0	BUF4LCELLAV	BUF4FULL	BUF4EMPTY	DBSTAT1 (0909_0909h)
14Ch	BUF3CELLCFRM	BUF3TSREL	BUF3AGED	BUF3WM1	BUF3WM0		BUF3FULL	BUF3EMPTY	BUF2CELLCFRM	BUF2TSREL	BUF2AGED	BUF2WM1	BUF2WM0		BUF2FULL	BUF2EMPTY	BUF1CELLCFRM	BUF1TSREL	BUF1AGED	BUF1WM1	BUF1WM0		BUF1FULL	BUF1EMPTY	BUF0CELLCFRM	BUF0TSREL	BUF0AGED	BUF0WM1	BUF0WM0		BUF0FULL	BUF0EMPTY	DBINT0 (0000_0000h)
150h	BUF3CELLCFRM	BUF3TSREL	BUF3AGED	BUF3WM1	BUF3WM0		BUF3FULL	BUF3EMPTY	BUF2CELLCFRM	BUF2TSREL	BUF2AGED	BUF2WM1	BUF2WM0		BUF2FULL	BUF2EMPTY	BUF1CELLCFRM	BUF1TSREL	BUF1AGED	BUF1WM1	BUF1WM0		BUF1FULL	BUF1EMPTY	BUF0CELLCFRM	BUF0TSREL	BUF0AGED	BUF0WM1	BUF0WM0		BUF0FULL	BUF0EMPTY	DBINT0EN (0000_0000h)
154h	BUF7CELLCFRM	BUF7TSREL	BUF7AGED	BUF7WM1	BUF7WM0		BUF7FULL	BUF7EMPTY	BUF6CELLCFRM	BUF6TSREL	BUF6AGED	BUF6WM1	BUF6WM0		BUF6FULL	BUF6EMPTY	BUF5CELLCFRM	BUF5TSREL	BUF5AGED	BUF5WM1	BUF5WM0		BUF5FULL	BUF5EMPTY	BUF4CELLCFRM	BUF4TSREL	BUF4AGED	BUF4WM1	BUF4WM0		BUF4FULL	BUF4EMPTY	DBINT1 (0000_0000h)
158h	BUF7CELLCFRM	BUF7TSREL	BUF7AGED	BUF7WM1	BUF7WM0		BUF7FULL	BUF7EMPTY	BUF6CELLCFRM	BUF6TSREL	BUF6AGED	BUF6WM1	BUF6WM0		BUF6FULL	BUF6EMPTY	BUF5CELLCFRM	BUF5TSREL	BUF5AGED	BUF5WM1	BUF5WM0		BUF5FULL	BUF5EMPTY	BUF4CELLCFRM	BUF4TSREL	BUF4AGED	BUF4WM1	BUF4WM0		BUF4FULL	BUF4EMPTY	DBIN1TEN (0000_0000h)
15Ch 174h 18Ch 1A4h 1BCh 1D4h 1ECh 204h		PADSIZE		CELL LENGTH					WM1CTL	WM0CTL	VIDEOSEL	STREAMTYPE					TSRELEASE	TSAGE		TSINSERT		TSSTRIP	BUFEN	BUFFERDIR									DB(N)CFG0 (0030_9651h) (0030_9684h) (0000_8201h) (0000_8200h) (0000_8101h) (0000_8100h) (0000_8102h) (0000_8000h)
160h 178h 190h 1A8h 1C0h 1D8h 1F0h 208h				STARTADDR																					ENDADDR								DB(N)CFG1 (0000_01FFh) (0200_03FFh) (0400_04FFh) (0500_05FFh) (0600_067Fh) (0680_06FFh) (0700_07FFh) (07FF_07FFh)



6.6.1 Data Buffer Bit Descriptions

0x140 DBCTL – Data Buffer Control				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
30	RSVD	R0W	0	Reserved. Do not write to this bit.
29	BUF7FLSH	R0W	0	Buffer 7 flush – Writing a 1 to this location causes all contents to be flushed from the associated buffer. All pointers and related state machines are synchronously reset when this bit is set.
28	BUF7PKTFLSH	R0W	0	Buffer 7 packet flush – Writing a 1 to this location causes the packet at the top of the current buffer to be flushed. A packet flush should not be performed on an empty buffer.
27	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
26	RSVD	R0W	0	Reserved. Do not write to this bit.
25	BUF6FLSH	R0W	0	Buffer 6 flush – Writing a 1 to this location causes all contents to be flushed from the associated buffer. All pointers and related state machines are synchronously reset when this bit is set.
24	BUF6PKTFLSH	R0W	0	Buffer 6 packet flush – Writing a 1 to this location causes the packet at the top of the current buffer to be flushed. A packet flush should not be performed on an empty buffer.
23	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
22	RSVD	R0W	0	Reserved. Do not write to this bit.
21	BUF5FLSH	R0W	0	Buffer 5 flush – Writing a 1 to this location causes all contents to be flushed from the associated buffer. All pointers and related state machines are synchronously reset when this bit is set.

0x140 DBCTL – Data Buffer Control (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
20	BUF5PKTFLSH	R0W	0	Buffer 5 packet flush – Writing a 1 to this location causes the packet at the top of the current buffer to be flushed. A packet flush should not be performed on an empty buffer.
19	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
18	RSVD	R0W	0	Reserved. Do not write to this bit.
17	BUF4FLSH	R0W	0	Buffer 4 flush – Writing a 1 to this location causes all contents to be flushed from the associated buffer. All pointers and related state machines are synchronously reset when this bit is set.
16	BUF4PKTFLSH	R0W	0	Buffer 4 packet flush – Writing a 1 to this location causes the packet at the top of the current buffer to be flushed. A packet flush should not be performed on an empty buffer.
15	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
14	RSVD	R0W	0	Reserved. Do not write to this bit.
13	BUF3FLSH	R0W	0	Buffer 3 flush – Writing a 1 to this location causes all contents to be flushed from the associated buffer. All pointers and related state machines are synchronously reset when this bit is set.
12	BUF3PKTFLSH	R0W	0	Buffer 3 packet flush – Writing a 1 to this location causes the packet at the top of the current buffer to be flushed. A packet flush should not be performed on an empty buffer.
11	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
10	RSVD	R0W	0	Reserved. Do not write to this bit.
9	BUF2FLSH	R0W	0	Buffer 2 flush – Writing a 1 to this location causes all contents to be flushed from the associated buffer. All pointers and related state machines are synchronously reset when this bit is set.
8	BUF2PKTFLSH	R0W	0	Buffer 2 packet flush – Writing a 1 to this location causes the packet at the top of the current buffer to be flushed. A packet flush should not be performed on an empty buffer.
7	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
6	RSVD	R0W	0	Reserved. Do not write to this bit.
5	BUF1FLSH	R0W	0	Buffer 1 flush – Writing a 1 to this location causes all contents to be flushed from the associated buffer. All pointers and related state machines are synchronously reset when this bit is set.
4	BUF1PKTFLSH	R0W	0	Buffer 1 packet flush – Writing a 1 to this location causes the packet at the top of the current buffer to be flushed. A packet flush should not be performed on an empty buffer.
3	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
2	RSVD	R0W	0	Reserved. Do not write to this bit.
1	BUF0FLSH	R0W	0	Buffer 0 flush – Writing a 1 to this location causes all contents to be flushed from the associated buffer. All pointers and related state machines are synchronously reset when this bit is set.
0	BUF0PKTFLSH	R0W	0	Buffer 0 packet flush – Writing a 1 to this location causes the packet at the top of the current buffer to be flushed. A packet flush should not be performed on an empty buffer.

0x144 DBSTAT0 – Data Buffer Status 0				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:29	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
28	BUF3WM1	RU	0	Buffer 3 watermark 1 − This bit is set by hardware to indicate that the number of quadlets in the associated buffer has risen above or fallen below the value in DB3CFG3.WATERMARK1, depending on the setting of DB3CFG0.WM1CTL.
27	BUF3WM0	RU	1	Buffer 3 watermark 0 − This bit is set by hardware to indicate that the number of quadlets in the associated buffer has risen above or fallen below the value in DB3CFG3.WATERMARK0, depending on the setting of DB3CFG0.WM0CTL.
26	BUF3LCELLAV	RU	0	Buffer 3 logical cell available – When set to 1, a complete logical cell has been confirmed into a transmit or receive buffer.
25	BUF3FULL	RU	0	Buffer 3 full – When set to 1, indicates that there is no space available in the current buffer. Software cannot write to this buffer when this bit is set.
24	BUF3EMPTY	RU	1	Buffer 3 empty – When set to 1, indicates that there is no data in the current buffer. Software cannot read from this buffer when this bit is set.
23:21	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
20	BUF2WM1	RU	0	Buffer 2 watermark 1 − This bit is set by hardware to indicate that the number of quadlets in the associated buffer has risen above or fallen below the value in DB2CFG3.WATERMARK1, depending on the setting of DB2CFG0.WM1CTL.
19	BUF2WM0	RU	1	Buffer 2 watermark 0 − This bit is set by hardware to indicate that the number of quadlets in the associated buffer has risen above or fallen below the value in DB2CFG3.WATERMARK0, depending on the setting of DB2CFG0.WM0CTL.
18	BUF2LCELLAV	RU	0	Buffer 2 logical cell available – When set to 1, a logical cell has been received and confirmed into a receive buffer.
17	BUF2FULL	RU	0	Buffer 2 full – When set to 1, indicates that there is no space available in the current buffer. Software cannot write to this buffer when this bit is set.
16	BUF2EMPTY	RU	1	Buffer 2 empty – When set to 1, indicates that there is no data in the current buffer. Software cannot read from this buffer when this bit is set.
15:13	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
12	BUF1WM1	RU	0	Buffer 1 watermark 1 − This bit is set by hardware to indicate that the number of quadlets in the associated buffer has risen above or fallen below the value in DB1CFG3.WATERMARK1, depending on the setting of DB1CFG0.WM1CTL.
11	BUF1WM0	RU	1	Buffer 1 watermark 0 − This bit is set by hardware to indicate that the number of quadlets in the associated buffer has risen above or fallen below the value in DB1CFG3.WATERMARK0, depending on the setting of DB1CFG0.WM0CTL.
10	BUF1LCELLAV	RU	0	Buffer 1 logical cell available – When set to 1, a logical cell has been received and confirmed into a receive buffer.
9	BUF1FULL	RU	0	Buffer 1 full – When set to 1, indicates that there is no space available in the current buffer. Software cannot write to this buffer when this bit is set.
8	BUF1EMPTY	RU	1	Buffer 1 empty – When set to 1, indicates that there is no data in the current buffer. Software cannot read from this buffer when this bit is set.

0x144 DBSTAT0 – Data Buffer Status 0 (continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
7:5	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
4	BUF0WM1	RU	0	Buffer 0 watermark 1 − This bit is set by hardware to indicate that the number of quadlets in the associated buffer has risen above or fallen below the value in DB0CFG3.WATERMARK1, depending on the setting of DB0CFG0.WM1CTL.
3	BUF0WM0	RU	1	Buffer 0 watermark 0 − This bit is set by hardware to indicate that the number of quadlets in the associated buffer has risen above or fallen below the value in DB0CFG3.WATERMARK0, depending on the setting of DB0CFG0.WM0CTL.
2	BUF0LCELLAV	RU	0	Buffer 0 logical cell available – When set to 1, a logical cell has been received and confirmed into a receive buffer.
1	BUF0FULL	RU	0	Buffer 0 full – When set to 1, indicates that there is no space available in the current buffer. Software cannot write to this buffer when this bit is set.
0	BUF0EMPTY	RU	1	Buffer 0 empty – When set to 1, indicates that there is no data in the current buffer. Software cannot read from this buffer when this bit is set.

0x148 DBSTAT1 – Data Buffer Status 1				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:29	RSVD	R0	0	Reserved − A write to this location has no effect. A read returns 0s.
28	BUF7WM1	RU	0	Buffer 7 watermark 1 − This bit is set by hardware to indicate that the number of quadlets in the associated buffer has risen above or fallen below the value in DB7CFG3.WATERMARK1, depending on the setting of DB7CFG0.WM1CTL.
27	BUF7WM0	RU	1	Buffer 7 watermark 0 − This bit is set by hardware to indicate that the number of quadlets in the associated buffer has risen above or fallen below the value in DB7CFG3.WATERMARK0, depending on the setting of DB7CFG0.WM0CTL.
26	BUF7LCELLAV	RU	0	Buffer 7 logical cell available – When set to 1, a logical cell has been received and confirmed into a receive buffer.
25	BUF7FULL	RU	0	Buffer 7 full – When set to 1, indicates that there is no space available in the current buffer. Software cannot write to this buffer when this bit is set to 1.

0x148 DBSTAT1 – Data Buffer Status 1 (continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
24	BUF7EMPTY	RU	1	Buffer 7 empty – When set to 1, indicates that there is no data in the current buffer. Software cannot read from this buffer when this bit is set to 1.
23:21	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
20	BUF6WM1	RU	0	Buffer 6 watermark 1 − This bit is set by hardware to indicate that the number of quadlets in the associated buffer has risen above or fallen below the value in DB6CFG3.WATERMARK1, depending on the setting of DB6CFG0.WM1CTL.
19	BUF6WM0	RU	1	Buffer 6 watermark 0 − This bit is set by hardware to indicate that the number of quadlets in the associated buffer has risen above or fallen below the value in DB6CFG3.WATERMARK0, depending on the setting of DB6CFG0.WM0CTL.
18	BUF6LCELLAV	RU	0	Buffer 6 logical cell available – When set to 1, a logical cell has been received and confirmed into a receive buffer.
17	BUF6FULL	RU	0	Buffer 6 full – When set to 1, indicates that there is no space available in the current buffer. Software cannot write to this buffer when this bit is set to 1.
16	BUF6EMPTY	RU	1	Buffer 6 empty – When set to 1, indicates that there is no data in the current buffer. Software cannot read from this buffer when this bit is set to 1.
15:13	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
12	BUF5WM1	RU	0	Buffer 5 watermark 1 − This bit is set by hardware to indicate that the number of quadlets in the associated buffer has risen above or fallen below the value in DB5CFG3.WATERMARK1, depending on the setting of DB5CFG0.WM1CTL.
11	BUF5WM0	RU	1	Buffer 5 watermark 0 − This bit is set by hardware to indicate that the number of quadlets in the associated buffer has risen above or fallen below the value in DB5CFG3.WATERMARK0, depending on the setting of DB5CFG0.WM0CTL.
10	BUF5LCELLAV	RU	0	Buffer 5 logical cell available – When set to 1, a logical cell has been received and confirmed into a receive buffer.
9	BUF5FULL	RU	0	Buffer 5 full – When set to 1, indicates that there is no space available in the current buffer. Software cannot write to this buffer when this bit is set to 1.
8	BUF5EMPTY	RU	1	Buffer 5 empty – When set to 1, indicates that there is no data in the current buffer. Software cannot read from this buffer when this bit is set to 1.
7:5	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
4	BUF4WM1	RU	0	Buffer 4 watermark 1 − This bit is set by hardware to indicate that the number of quadlets in the associated buffer has risen above or fallen below the value in DB4CFG3.WATERMARK1, depending on the setting of DB4CFG0.WM1CTL.
3	BUF4WM0	RU	1	Buffer 4 watermark 0 − This bit is set by hardware to indicate that the number of quadlets in the associated buffer has risen above or fallen below the value in DB4CFG3.WATERMARK0, depending on the setting of DB4CFG0.WM0CTL.

0x148 DBSTAT1 – Data Buffer Status 1 (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
2	BUF4LCELLAV	RU	0	Buffer 4 logical cell available – When set to 1, a logical cell has been received and confirmed into a receive buffer.
1	BUF4FULL	RU	0	Buffer 4 full – When set to 1, indicates that there is no space available in the current buffer. Software cannot write to this buffer when this bit is set to 1.
0	BUF4EMPTY	RU	1	Buffer 4 empty – When set to 1, indicates that there is no data in the current buffer. Software cannot read from this buffer when this bit is set to 1.

0x14C DBINT0 – Data Buffer Interrupts 0				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	BUFF3CELLCFRM	RCU	0	Buffer 3 cell confirm – This bit is set by hardware to indicate that a complete logical cell has been confirmed into the associated buffer.
30	BUFF3TSREL	RCU	0	Buffer 3 time stamp release – This bit is set by hardware to indicate that a time-stamped logical cell in the current buffer is ready to be released, irrespective of buffer direction.
29	BUF3AGED	RCU	0	Buffer 3 time stamp expired – This bit is set by hardware to indicate that a time-stamped logical cell in the current buffer has been flushed because its time stamp expired, irrespective of buffer direction.
28	BUF3WM1	RCU	0	Buffer 3 watermark 1 − This bit is set by hardware to indicate that DBSTAT0.BUF3WM1 has changed its status from 0 to 1.
27	BUF3WM0	RCU	0	Buffer 3 watermark 0 − This bit is set by hardware to indicate that DBSTAT0.BUF3WM0 has changed its status from 0 to 1.
26	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
25	BUF3FULL	RCU	0	Buffer 3 full – When set to 1, indicates that there is no space available in the current buffer.
24	BUF3EMPTY	RCU	0	Buffer 3 empty – When set to 1, indicates that there is no data in the current buffer.
23	BUF2CELLCFRM	RCU	0	Buffer 2 cell confirm – This bit is set by hardware to indicate that a complete logical cell has been confirmed into the associated buffer.
22	BUF2TSREL	RCU	0	Buffer 2 time stamp release – This bit is set by hardware to indicate that a time-stamped logical cell in the current buffer is ready to be released, irrespective of buffer direction.
21	BUF2AGED	RCU	0	Buffer 2 time stamp expired – This bit is set by hardware to indicate that a time-stamped logical cell in the current buffer has been flushed because its time stamp expired, irrespective of buffer direction.
20	BUF2WM1	RCU	0	Buffer 2 watermark 1 − This bit is set by hardware to indicate that DBSTAT0.BUF2WM1 has changed its status from 0 to 1.
19	BUF2WM0	RCU	0	Buffer 2 watermark 0 − This bit is set by hardware to indicate that DBSTAT0.BUF3WM0 has changed its status from 0 to 1.
18	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
17	BUF2FULL	RCU	0	Buffer 2 full – When set to 1, indicates that there is no space available in the current buffer.
16	BUF2EMPTY	RCU	1	Buffer 2 empty – When set to 1, indicates that there is no data in the current buffer.

0x14C DBINT0 – Data Buffer Interrupts 0 (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
15	BUF1CELLCFRM	RCU	0	Buffer 1 cell confirm – This bit is set by hardware to indicate that a complete logical cell has been confirmed into the associated buffer.
14	BUF1TSREL	RCU	0	Buffer 1 time stamp release – This bit is set by hardware to indicate that a time-stamped logical cell in the current buffer is ready to be released, irrespective of buffer direction.
13	BUF1AGED	RCU	0	Buffer 1 time stamp expired – This bit is set by hardware to indicate that a time-stamped logical cell in the current buffer has been flushed because its time stamp expired, irrespective of buffer direction.
12	BUF1WM1	RCU	0	Buffer 1 water mark 1 − This bit is set by hardware to indicate that DBSTAT0.BUF1WM1 has changed its status from 0 to 1.
11	BUF1WM0	RCU	0	Buffer 1 water mark 0 − This bit is set by hardware to indicate that DBSTAT0.BUF1WM0 has changed its status from 0 to 1.
10	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
9	BUF1FULL	RCU	0	Buffer 1 full – When set to 1, indicates that there is no space available in the current buffer
8	BUF1EMPTY	RCU	0	Buffer 1 empty – When set to 1, indicates that there is no data in the current buffer.
7	BUF0CELLCFRM	RCU	0	Buffer 0 cell confirm – This bit is set by hardware to indicate that a complete logical cell has been confirmed into the associated buffer.
6	BUF0TSREL	RCU	0	Buffer 0 time stamp release – This bit is set by hardware to indicate that a time-stamped logical cell in the current buffer is ready to be released, irrespective of buffer direction.
5	BUF0AGED	RCU	0	Buffer 0 time stamp expired – This bit is set by hardware to indicate that a time-stamped logical cell in the current buffer has been flushed because its time stamp expired, irrespective of buffer direction.
4	BUF0WM1	RCU	0	Buffer 0 water mark 1 − This bit is set by hardware to indicate that DBSTAT0.BUF0WM1 has changed its status from 0 to 1.
3	BUF0WM0	RCU	0	Buffer 0 water mark 0 − This bit is set by hardware to indicate that DBSTAT0.BUF0WM0 has changed its status from 0 to 1.
2	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
1	BUF0FULL	RCU	0	Buffer 0 full – When set to 1, indicates that there is no space available in the current buffer.
0	BUF0EMPTY	RCU	0	Buffer 0 empty – When set to 1, indicates that there is no data in the current buffer.

0x150 DBINT0EN − Data Buffer Interrupt 0 Enables				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	BUF3CELLCFRM	RW	0	Buffer 3 cell confirm − When this bit is set to 1, the SYSINT.DBINT1 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT1 bit.
30	BUF3TSREL	RW	0	Buffer 3 time stamp release − When this bit is set to 1, the SYSINT.DBINT1 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT1 bit.
29	BUF3AGED	RW	0	Buffer 3 time stamp expired − When this bit is set to 1, the SYSINT.DBINT1 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT1 bit.
28	BUF3WM1	RW	0	Buffer 3 water mark 1 − When this bit is set to 1, the SYSINT.DBINT1 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT1 bit.
27	BUF3WM0	RW	0	Buffer 3 water mark 0 − When this bit is set to 1, the SYSINT.DBINT1 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT1 bit.
26	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
25	BUF3FULL	RW	0	Buffer 3 full − When this bit is set to 1, the SYSINT.DBINT1 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT1 bit.
24	BUF3EMPTY	RW	0	Buffer 3 empty − When this bit is set to 1, the SYSINT.DBINT1 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT1 bit.
23	BUF2CELLCFRM	RW	0	Buffer 2 cell confirm − When this bit is set to 1, the SYSINT.DBINT1 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT1 bit.
22	BUF2TSREL	RW	0	Buffer 2 time stamp release − When this bit is set to 1, the SYSINT.DBINT1 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT1 bit.
21	BUF2AGED	RW	0	Buffer 2 time stamp expired − When this bit is set to 1, the SYSINT.DBINT1 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT1 bit.

0x150 DBINT0EN − Data Buffer Interrupt 0 Enables (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
20	BUF2WM1	RW	0	Buffer 2 water mark 1 − When this bit is set to 1, the SYSINT.DBINT1 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT1 bit.
19	BUF2WM0	RW	0	Buffer 2 water mark 0 − When this bit is set to 1, the SYSINT.DBINT1 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT1 bit.
18	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
17	BUF2FULL	RW	0	Buffer 2 full − When this bit is set to 1, the SYSINT.DBINT1 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT1 bit.
16	BUF2EMPTY	RW	1	Buffer 2 empty − When this bit is set to 1, the SYSINT.DBINT1 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT1 bit.
15	BUF1CELLCFRM	RW	0	Buffer 1 cell confirm − When this bit is set to 1, the SYSINT.DBINT0 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT0 bit.
14	BUF1TSREL	RW	0	Buffer 1 time stamp release − When this bit is set to 1, the SYSINT.DBINT0 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT0 bit.
13	BUF1AGED	RW	0	Buffer 1 time stamp expired − When this bit is set to 1, the SYSINT.DBINT0 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT0 bit.
12	BUF1WM1	RW	0	Buffer 1 water mark 1 − When this bit is set to 1, the SYSINT.DBINT0 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT0 bit.
11	BUF1WM0	RW	0	Buffer 1 water mark 0 − When this bit is set to 1, the SYSINT.DBINT0 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT0 bit.
10	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
9	BUF1FULL	RW	0	Buffer 1 full − When this bit is set to 1, the SYSINT.DBINT0 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT0 bit.

0x150 DBINT0EN − Data Buffer Interrupt 0 Enables (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
8	BUF1EMPTY	RW	0	Buffer 1 empty − When this bit is set to 1, the SYSINT.DBINT0 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT0 bit.
7	BUF0CELLCFRM	RW	0	Buffer 0 cell confirm − When this bit is set to 1, the SYSINT.DBINT0 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT0 bit.
6	BUF0TSREL	RW	0	Buffer 0 time stamp release − When this bit is set to 1, the SYSINT.DBINT0 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT0 bit.
5	BUF0AGED	RW	0	Buffer 0 time stamp expired− When this bit is set to 1, the SYSINT.DBINT0 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT0 bit.
4	BUF0WM1	RW	0	Buffer 0 water mark 1 − When this bit is set to 1, the SYSINT.DBINT0 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT0 bit.
3	BUF0WM0	RW	0	Buffer 0 water mark 0 − When this bit is set to 1, the SYSINT.DBINT0 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT0 bit.
2	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
1	BUF0FULL	RW	0	Buffer 0 full − When this bit is set to 1, the SYSINT.DBINT0 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT0 bit.
0	BUF0EMPTY	RW	0	Buffer 0 empty − When this bit is set to 1, the SYSINT.DBINT0 bit is set to 1 when the corresponding bit in the DBINT0 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT0 bit.

0x154 DBINT1 – Data Buffer Interrupts 1				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	BUF7CELLCFRM	RCU	0	Buffer 7 cell confirm – This bit is set by hardware to indicate that a complete logical cell has been confirmed into the associated buffer.
30	BUF7TSREL	RCU	0	Buffer 7 time stamp release – This bit is set by hardware to indicate that a time-stamped logical cell in the current buffer is ready to be released, irrespective of buffer direction.
29	BUF7AGED	RCU	0	Buffer 7 time stamp expired – This bit is set by hardware to indicate that a time-stamped logical cell in the current buffer has been flushed because its time stamp expired, irrespective of buffer direction.
28	BUF7WM1	RCU	0	Buffer 7 water mark 1 − This bit is set by hardware to indicate that DBSTAT1.BUF7WM1 has changed its status from 0 to 1.

0x154 DBINT1 – Data Buffer Interrupts 1 (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
27	BUF7WM0	RCU	0	Buffer 7 water mark 0 − This bit is set by hardware to indicate that DBSTAT1.BUF7WM0 has changed its status from 0 to 1.
26	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
25	BUF7FULL	RCU	0	Buffer 7 full – When set to 1, indicates that there is no space available in the current buffer.
24	BUF7EMPTY	RCU	0	Buffer 7 empty – When set to 1, indicates that there is no data in the current buffer.
23	BUF6CELLCFRM	RCU	0	Buffer 6 cell confirm – This bit is set by hardware to indicate that a complete logical cell has been confirmed into the associated buffer.
22	BUF6TSREL	RCU	0	Buffer 6 time stamp release – This bit is set by hardware to indicate that a time-stamped logical cell in the current buffer is ready to be released, irrespective of buffer direction.
21	BUF6AGED	RCU	0	Buffer 6 time stamp expired – This bit is set by hardware to indicate that a time-stamped logical cell in the current buffer has been flushed because its time stamp expired, irrespective of buffer direction.
20	BUF6WM1	RCU	0	Buffer 6 water mark 1 − This bit is set by hardware to indicate that DBESTAT1.BUF6WM1 has changed its status from 0 to 1.
19	BUF6WM0	RCU	0	Buffer 6 water mark 0 − This bit is set by hardware to indicate that DBESTAT1.BUF6WM0 has changed its status from 0 to 1.
18	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
17	BUF6FULL	RCU	0	Buffer 6 full – When set to 1, indicates that there is no space available in the current buffer.
16	BUF6EMPTY	RCU	0	Buffer 6 empty – When set to 1, indicates that there is no data in the current buffer.
15	BUF5CELLCFRM	RCU	0	Buffer 5 cell confirm – This bit is set by hardware to indicate that a complete logical cell has been confirmed into the associated buffer.
14	BUF5TSREL	RCU	0	Buffer 5 time stamp release – This bit is set by hardware to indicate that a time-stamped logical cell in the current buffer is ready to be released, irrespective of buffer direction.
13	BUF5AGED	RCU	0	Buffer 5 time stamp expired – This bit is set by hardware to indicate that a time-stamped logical cell in the current buffer has been flushed because its time stamp expired, irrespective of buffer direction.
12	BUF5WM1	RCU	0	Buffer 5 water mark 1 − This bit is set by hardware to indicate that DBESTAT1.BUF5WM1 has changed its status from 0 to 1.
11	BUF5WM0	RCU	0	Buffer 5 water mark 0 − This bit is set by hardware to indicate that DBESTAT1.BUF5WM0 has changed its status from 0 to 1.
10	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
9	BUF5FULL	RCU	0	Buffer 5 full – When set to 1, indicates that there is no space available in the current buffer.
8	BUF5EMPTY	RCU	0	Buffer 5 empty – When set to 1, indicates that there is no data in the current buffer.
7	BUF4CELLCFRM	RCU	0	Buffer 4 cell confirm – This bit is set by hardware to indicate that a complete logical cell has been confirmed into the associated buffer.
6	BUF4TSREL	RCU	0	Buffer 4 time stamp release – This bit is set by hardware to indicate that a time-stamped logical cell in the current buffer is ready to be released, irrespective of buffer direction.

0x154 DBEINT – Data Buffer Interrupts 1 (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
5	BUF4AGED	RCU	0	Buffer 4 time stamp expired – This bit is set by hardware to indicate that a time-stamped logical cell in the current buffer has been flushed because its time stamp expired, irrespective of buffer direction.
4	BUF4WM1	RCU	0	Buffer 4 water mark 1 − This bit is set by hardware to indicate that DBSTAT1.BUF4WM1 has changed its status from 0 to 1.
3	BUF4WM0	RCU	0	Buffer 4 water mark 0 − This bit is set by hardware to indicate that DBSTAT1.BUF4WM0 has changed its status from 0 to 1.
2	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
1	BUF4FULL	RCU	0	Buffer 4 full – When set to 1, indicates that there is no space available in the current buffer.
0	BUF4EMPTY	RCU	0	Buffer 4 empty – When set to 1, indicates that there is no data in the current buffer.

0x158 DBINT1EN – Data Buffer Interrupt 1 Enables				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	BUF7CELLCFRM	RW	0	Buffer 7 cell confirm − When this bit is set to 1, the SYSINT.DBINT3 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT3 bit.
30	BUF7TSREL	RW	0	Buffer 7 time stamp release − When this bit is set to 1, the SYSINT.DBINT3 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT3 bit.
29	BUF7AGED	RW	0	Buffer 7 time stamp expired − When this bit is set to 1, the SYSINT.DBINT3 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT3 bit.
28	BUF7WM1	RW	0	Buffer 7 water mark 1 − When this bit is set to 1, the SYSINT.DBINT3 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT3 bit.
27	BUF7WM0	RW	0	Buffer 7 water mark 0 − When this bit is set to 1, the SYSINT.DBINT3 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT3 bit.
26	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
25	BUF7FULL	RW	0	Buffer 7 full − When this bit is set to 1, the SYSINT.DBINT3 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT3 bit.
24	BUF7EMPTY	RW	0	Buffer 7 empty − When this bit is set to 1, the SYSINT.DBINT3 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT3 bit.

0x158 DBEINTEN – Data Buffer Interrupt 1 Enables (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
23	BUF6CELLCFRM	RW	0	Buffer 6 cell confirm − When this bit is set to 1, the SYSINT.DBINT3 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT3 bit.
22	BUF6TSREL	RW	0	Buffer 6 time stamp release − When this bit is set to 1, the SYSINT.DBINT3 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT3 bit.
21	BUF6AGED	RW	0	Buffer 6 time stamp expired− When this bit is set to 1, the SYSINT.DBINT3 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBInt1 register has no effect on the SYSINT.DBINT3 bit.
20	BUF6WM1	RW	0	Buffer 6 water mark 1 − When this bit is set to 1, the SYSINT.DBINT3 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT3 bit.
19	BUF6WM0	RW	0	Buffer 6 water mark 0 − When this bit is set to 1, the SYSINT.DBINT3 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT3 bit.
18	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
17	BUF6FULL	RW	0	Buffer 6 full − When this bit is set to 1, the SYSINT.DBINT3 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT3 bit.
16	BUF6EMPTY	RW	0	Buffer 6 empty − When this bit is set to 1, the SYSINT.DBINT3 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT3 bit.
15	BUF5CELLCFRM	RW	0	Buffer 5 cell confirm − When this bit is set to 1, the SYSINT.DBINT2 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT2 bit.
14	BUF5TSREL	RW	0	Buffer 5 time stamp release − When this bit is set to 1, the SYSINT.DBINT2 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT2 bit.
13	BUF5AGED	RW	0	Buffer 5 time stamp expired− When this bit is set to 1, the SYSINT.DBINT2 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT2 bit.

0x158 DBEINTEN – Data Buffer Interrupt 1 Enables (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
12	BUF5WM1	RW	0	Buffer 5 water mark 1 − When this bit is set to 1, the SYSINT.DBINT2 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT2 bit.
11	BUF5WM0	RW	0	Buffer 5 water mark 0 − When this bit is set to 1, the SYSINT.DBINT2 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT2 bit.
10	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
9	BUF5FULL	RW	0	Buffer 5 full − When this bit is set to 1, the SYSINT.DBINT2 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT2 bit.
8	BUF5EMPTY	RW	0	Buffer 5 empty − When this bit is set to 1, the SYSINT.DBINT2 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT2 bit.
7	BUF4CELLCFRM	RW	0	Buffer 4 cell confirm − When this bit is set to 1, the SYSINT.DBINT2 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT2 bit.
6	BUF4TSREL	RW	0	Buffer 4 time stamp release − When this bit is set to 1, the SYSINT.DBINT2 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT2 bit.
5	BUF4AGED	RW	0	Buffer 4 time stamp expired − When this bit is set to 1, the SYSINT.DBINT2 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT2 bit.
4	BUF4WM1	RW	0	Buffer 4 water mark 1 − When this bit is set to 1, the SYSINT.DBINT2 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT2 bit.
3	BUF4WM0	RW	0	Buffer 4 water mark 0 − When this bit is set to 1, the SYSINT.DBINT2 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT0 register has no effect on the SYSINT.DBINT2 bit.
2	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
1	BUF4FULL	RW	0	Buffer 4 full − When this bit is set to 1, the SYSINT.DBINT2 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT2 bit.
0	BUF4EMPTY	RW	0	Buffer 4 empty − When this bit is set to 1, the SYSINT.DBINT2 bit is set to 1 when the corresponding bit in the DBINT1 register is set by hardware. When set to 0, the corresponding bit in the DBINT1 register has no effect on the SYSINT.DBINT2 bit.

0x15C 0x174 0x18C 0x1A4 0x1BC 0x1D4 0x1EC 0x204				
DB(N)CFG0 – Data Buffer #N Configuration Register 0				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:30	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
29:28	PADSIZE	RW	0	Padding size − The number of bytes in the last quadlet of a packet that does not contain valid data. This is only used if the data does not end on a quadlet boundary.
27:16	CELL LENGTH	RW	DEP	Cell length – The value written to this field indicates the number of quadlets to be flushed when a packet flush command is issued to the associated buffer. The default values for these registers are buffer-dependent as shown in the following: Buffer 0 – 30 Buffer 1 – 30 Buffer 2 – 00 Buffer 3 – 00 Buffer 4 – 00 Buffer 5 – 00 Buffer 6 – 00 Buffer 7 – 00 (not configured)
15	WM1CTL	RW	1	WTRMRK 1 control – The setting of this bit determines the functionality of the DBSTAT.BUF(N)WM1 bit. When set to 1, the DBSTAT.BUF(N)WM1 bit is asserted when the number of quadlets in the associated buffer is greater than or equal to the value in the associated DB(N)CFG3.WATERMARK1 field. When set to 0, the DBSTAT.BUF(N)WM1 bit is asserted when the number of quadlets in the associated buffer is less than or equal to the value in the associated DB(N)CFG3.WATERMARK1 field. If configured for water mark monitoring, the associated GPIO signal acts the same as the DBSTAT.BUF(N)WM1 bit.
14	WM0CTL	RW	0	WTRMRK 0 control – The setting of this bit determines the functionality of the DBSTAT.BUF(N)WM0 bit. When set to 1, the DBSTAT.BUF(N)WM0 bit is asserted when the number of quadlets in the associated buffer is greater than or equal to the value in the associated DB(N)CFG3.WATERMARK0 field. When set to 0, the DBSTAT.BUF(N)WM1 bit is asserted when the number of quadlets in the associated buffer is less than or equal to the value in the associated DB(N)CFG3.WATERMARK0 field. If configured for water mark monitoring, the associated GPIO signal acts the same as the DBSTAT.BUF(N)WM0 bit.
13:12	VIDEOSEL	RW	DEP	Video select – Routes the indicated video stream hardware to the associated buffer according to the following settings: 00 – No video stream routed to the associated buffer 01 – Video stream A routed to the associated buffer 10 – Video stream B routed to the associated buffer 11 – No video stream routed to the associated buffer Individual buffers default to the following selections: Buffer 0 – 01 Buffer 1 – 01 Buffer 2 – 00 Buffer 3 – 00 Buffer 4 – 00 Buffer 5 – 00 Buffer 6 – 00 Buffer 7 – 00 (not configured)

0x15C 0x174 0x18C 0x1A4 0x1BC 0x1D4 0x1EC 0x204 (Continued)				
DB(N)CFG0 – Data Buffer #N Configuration Register 0				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
11:8	STREAMTYPE	RW	DEP	Stream type – The binary encoded value in this field selects the stream type for the associated buffer as follows: 0000 – Unconfigured 0001 – Asynchronous data 0011 – Asynchronous stream 0100 – DirecTV 130 0101 – DirecTV 140 0110 – DVB 0111 – DV, PAL, standard definition 1000 – DV, PAL, high definition 1001 – DV, NTSC, standard definition 1010 – DV, NTSC, high definition 0010 and 1011 – 1111 Reserved Individual buffers default to the following configurations: Buffer 0 – 0110 (DVB) Buffer 1 – 0110 (DVB) Buffer 2 – 0010 (Reserved) Buffer 3 – 0010 (Reserved) Buffer 4 – 0001 (ASYNC) Buffer 5 – 0001 (ASYNC) Buffer 6 – 0001 (ASYNC) Buffer 7 – 0000 (not configured)
7	TSRELEASE	RW	DEP	Time stamp release – Setting this bit to 1 enables time stamp release for the associated buffer. When enabled, an MPEG2 cell is held in the buffer until its time stamp has matured.
6	TSAGE	RW	DEP	Time stamp age – Setting this bit to 1 causes logical cells with expired time stamps to be flushed from the associated buffer.
5	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
4	TSINSERT	RW	DEP	Time stamp insert – Setting this bit to 1 causes the current 1394 cycle timer value to be inserted as the time stamp for the current logical cell, irrespective of buffer direction.
3	RSVD	RW	0	Reserved. Do not write to this bit.
2	TSSTRIP	RW	DEP	Time stamp strip – Setting this bit to 1 causes the first quadlet of each cell confirmed into the associated buffer to be treated as a time stamp and stripped from the payload data. This field defaults to 1 for DB1CFG0. All others default to 0. This bit should only be used for MPEG2 data.
1	BUFEN	RW	DEP	Buffer enable – Writing a 1 to this location enables the associated buffer. This defaults to 1 for DB6CFG0. All others default to 0.

0x15C 0x174 0x18C 0x1A4 0x1BC 0x1D4 0x1EC 0x204 (Continued)				
DB(N)CFG0 – Data Buffer #N Configuration Register 0				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
0	BUFFERDIR	RW	DEP	Buffer direction – This bit selects the direction for the current buffer as follows: 0 – Receive 1 – Transmit Individual buffers default to the following directions: Buffer 0 – 1 Buffer 1 – 0 Buffer 2 – 1 Buffer 3 – 0 Buffer 4 – 1 Buffer 5 – 0 Buffer 6 – 0 Buffer 7 – 0 (not configured)

0x160 0x178 0x190 0x1A8 0x1C0 0x1D8 0x1F0 0x208				
DB(N)CFG1 – Data Buffer #N Configuration Register 1				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:27	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
26:16	STARTADDR	RW	DEP	Start address – The value in this register indicates the quadlet start address for the associated data buffer. The default values for the eight DB(N)CFG1.STARTADDR registers are as follows; Buffer start address — Initial size of buffer (bytes) Buffer 0 – 000 — 2k Buffer 1 – 200 — 2k Buffer 2 – 400 — 1k Buffer 3 – 500 — 1k Buffer 4 – 600 — 512 Buffer 5 – 680 — 512 Buffer 6 – 700 — 1k Buffer 7 – 7FF (not configured) — 0
15:11	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
10:0	ENDADDR	RW	DEP	End address – The value in this register indicates the quadlet end address for the associated data buffer. The default values for the eight DB(N)CFG1.ENDADDR registers are as follows: Buffer 0 – 1FF Buffer 1 – 3FF Buffer 2 – 4FF Buffer 3 – 5FF Buffer 4 – 67F Buffer 5 – 6FF Buffer 6 – 7FF Buffer 7 – 7FF (not configured)

0x164 0x17C 0x194 0x1AC 0x1C4 0x1DC 0x1F4 0x20C				
DB(N)CFG2 – Data Buffer #N Configuration Register 2				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:25	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
24:0	TSOFFSET	RW	0	Time stamp offset – The value contained in this register is added to the time stamp of the logical cell.

0x168 0x180 0x198 0x1B0 0x1C8 0x1E0 0x1F8 0x210				
DB(N)CFG3 – Data Buffer #N Configuration Register 3				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:27	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
26:16	WATERMARK0	RW	1	Water mark 0 − Contains the number of quadlets used during water mark 0 compare. Programmable in number of hex quadlets. The value is offset from the DB(N)CFG1.STARTADDR and must be contained within the associated buffer limits. Setting this value to 0 disables the feature. The default value of 1 provides an indication whenever any data exists in the associated buffer, given water mark 0 is set up as a low water mark [DB(N)CFG.WMOCTL = 0].
15:11	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
10:0	WATERMARK1	RW	DEP	Water mark 1 − Contains the number of quadlets used during water mark 1 compare. Programmable in number of hex quadlets. The value is offset from the DB(N)CFG1.STARTADDR and must be contained within the associated buffer limits. Given water mark 1 is set up as a high water mark [DB(N)CFG0.WM1CTL = 1], the default values for the buffers provide and indication when there are four empty quadlet locations left within the associated buffer as follows: Buffer 0 – 1FC Buffer 1 – 1FC Buffer 2 – 0FC Buffer 3 – 0FC Buffer 4 – 07C Buffer 5 – 07C Buffer 6 – 0FC Buffer 7 – 000 (not configured)

0x16C 0x184 0x19C 0x1B4 0x1CC 0x1E4 0x1FC 0x214				
DB(N)ACC0 – Data Buffer #N Access 0				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:0	BUFACC	RW	0	Buffer access – Reads and writes to this location result in pop and push operations for the associated buffer. For writes, the last quadlet for the packet must be written to DB(N)ACC1.BUFACCCFRM.

0x170 0x188 0x1A0 0x1B8 0x1D0 0x1E8 0x200 0x218				
DB(N)ACC1 – Data Buffer #N Access 1				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:0	BUFACCCFRM	RW	0	Buffer access confirm – Writing to this location confirms a logical cell into the current buffer for transmission.

6.7 Transmit Data Path CFR Map

Address	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	TXDP CFR Name (Hex Reset Value)
240h	TXDPRST					VBDV_THMODE	VBDV_THSEL			VADV_THMODE	VADV_THSEL			RSTONFPB	RSTONFPA	ACKFLSH	ATXRETRYINT								ATXRETRYMAX								TXDPCTL (0000_00FFh)
244h			VIDSEL_ERR	ACKC_ERR	ACKCODE					NODEID				PKTID							TCODE								ACKCNT				TXDPSTAT (0000_0000h)
248h					ERRASYTX	ACKLOST	ACKRCVD	ERRISOTX	ERRBFLSH0	ERRBFLSH1	ERRBFLSH2	ERRBFLSH3	ERRDBC0	ERRDBC1	ERRDBC2	ERRDBC3	ERRTH0_0	ERRTH0_1	ERRTH0_2	ERRTH0_3	ERRBFLSH4	ERRBFLSH5	ERRBFLSH6	ERRBFLSH7	ERRDBC4	ERRDBC5	ERRDBC6	ERRDBC7	ERRTH0_4	ERRTH0_5	EERTH0_6	EERTH0_7	TXDPINT (0000_0000h)
24Ch					ERRASYTX	ACKLOST	ACKRCVD	ERRISOTX	ERRBFLSH0	ERRBFLSH1	ERRBFLSH2	ERRBFLSH3	ERRDBC0	ERRDBC1	ERRDBC2	ERRDBC3	ERRTH0_0	ERRTH0_1	ERRTH0_2	ERRTH0_3	ERRBFLSH4	ERRBFLSH5	ERRBFLSH6	ERRBFLSH7	ERRDBC4	ERRDBC5	ERRDBC6	ERRDBC7	ERRTH0_4	ERRTH0_5	EERTH0_6	EERTH0_7	TXDPINTEN (0000_0000h)
250h 268h 280h 298h 2B0h 2C8h 2E0h 2F8h																					SPH_NEWCELL	INTSSP	VHFWEN	BFLUSHEN	FAIRARB_OFF	HIM	H0IM	EPINSRT	DVTXSUB	MPEG2TXCLASS			TXDP(N)CFG (0000_0043h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h)
254h 26Ch 284h 29Ch 2B4h 2CCh 2E4h 2FCh	ASYNC0/VIDEO (Fields vary depending upon configuration)																																TXDP(N)H0 (0000_4010h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h)
258h 270h 288h 2A0h 2B8h 2D0h 2E8h 300h	ASYNC1/VIDEO (Fields vary depending upon configuration)																																TXDP(N)H1 (0006_C400h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h)
25Ch 274h 28Ch 2A4h 2BCh 2D4h 2ECh 304h	ASYNC2/DirecTV 130/DirecTV 140 DVP/PALSD/PALHD/NTSCHD (Fields vary depending upon configuration)																																TXDP(N)H2 (0000_0000h)

Address	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	RXDP CFR Name (Hex Reset Value)
260h 278h 290h 2A8h 2C0h 2D8h 2F0h 308h	ASYNC3/DVH0/DirecTV 130 (Fields vary depending upon configuration)																																TXDP(N)H3 (0000_0000h)
264h 27Ch 294h 2ACh 2C4h 2DCh 2F4h 30Ch	DVH1																																TXDP(N)H4 (0000_0000h)
310h	VA_DV_BURST		VA_DV_EPGAG					VA_DV_EPNUM				VA_DV_DELAY																					TXDPDVABRST (0000_0000h)
314h	VB_DV_BURST		VB_DV_EPGAP					VB_DV_EPNUM				VB_DV_DELAY																					TXDPDVBBRST (0000_0000h)
318h-33Fh	RESERVED																																RSVD (0000_0000h)

0x240 TXDPCTL – Transmit Data Path Control				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	TXDPRST	R0W	0	Transmit data path reset – Writing a 1 to this bit sets all transmit data path state machines and storage elements to initial conditions. CFR bits are not affected by writes to this location. This bit is self clearing.
30:27	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
26	VBDV_THMODE	RW	0	Video B DV threshold mode – Set to 1, the first DV source packet of every frame is transmitted only after the related data buffer has accumulated 480 + N bytes of data. Set to 0, the first DV source packet following power-on reset or TXDP software reset is transmitted only after the related data buffer has filled to 480 + N bytes of data Where, N is the value found in the TXDPCTL.VBDV_THSEL bit field. These settings are also valid for the DV-HD data, where the accumulated data is 960 + N bytes of data.
25:24	VBDV_THSEL	RW	0	Video B DV threshold select – The binary encoded value in this register indicates the number of bytes in addition to a complete source packet that must be present in the buffer before a DV source packet is transmitted. 00 – 0 bytes (SD) 0 bytes (HD) 01 – 128 bytes (SD) 256 bytes (HD) 10 – 256 bytes (SD) 512 bytes (HD) 11 – 384 bytes (SD) 768 bytes (HD)
23	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.

0x240 TXDPCTL – Transmit Data Path Control (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
22	VADV_THMODE	RW	0	Video A DV threshold mode – Set to 1, the first DV source packet of every frame is transmitted only after the related data buffer has accumulated 480 + N bytes of data. Set to 0, the first DV source packet following power-on reset or TXDP software reset is transmitted only after the related data buffer has filled to 480 + N bytes of data. Where, N is the value found in the TXDPCTL.VADV_THSEL bit field. These settings are also valid for the DV-HD data, where the accumulated data is 960 + N bytes of data.
21:20	VADV_THSEL	RW	0	Video A DV threshold select – The binary encoded value in this register indicates the number of bytes in addition to a complete source packet that must be present in the buffer before a DV source packet is transmitted. 00 – 0 bytes (SD) 0 bytes (HD) 01 – 128 bytes (SD) 256 bytes (HD) 10 – 256 bytes (SD) 512 bytes (HD) 11 – 384 bytes (SD) 768 bytes (HD)
19	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
18	RSTONFPB	RW	0	Reset on frame pulse B – When this bit is set to 1, empty packet insertion logic for video stream B is reset each time a new frame pulse is received.
17	RSTONFPA	RW	0	Reset on frame pulse A – When this bit is set to 1, empty packet insertion logic for video stream A is reset each time a new frame pulse is received.
16	ACKFLSH	R0W	0	ACK code flush – Writing a 1 to this location causes the ACK FIFO to be flushed. This bit is self clearing.
15:8	ATXRETRYINT	RW	0	Asynchronous transmit retry interval – The binary encoded value stored in this register indicates the number of isochronous cycles between asynchronous transmit retrys.
7:0	ATXRETRYMAX	RW	FF	Asynchronous transmit retry max – The binary encoded value stored in this register indicates the maximum number of retries to attempt for asynchronous transmission.

0x244 TXDPSTAT – Transmit Data Path Status				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:30	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
29	VIDSEL_ERR	RU	0	Video select error – This bit is set by hardware if a buffer is selected for video A and video B at the same time or more than two total video paths are selected.
28	ACKC_ERR	RU	0	Acknowledge code error – When this bit is set to 1, an acknowledge code was returned with an error. This indicates that the asynchronous packet has experienced a transmit failure.
27:24	ACKCODE	RU	0	Acknowledge code – the value in this field represents the 1394 ACK code generated by the receiving node. ACK complete is always returned by the link layer controller internally for asynchronous streaming and broadcast packets. A list of ACK codes is included in Table 5−10.
23:22	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
21:16	NODEID	RU	0	Destination node ID – Not valid for asynchronous streaming data.
15:8	PKTID	RU	0	Packet identifier – This field encodes the packet identification information for the current transmit packet. This field represents bits 8 through 20 of the first quadlet of the transmitted 1394 packet, respectively.
7:4	TCODE	R0	0	IEEE-1394 TCODE – This field represents the TCODE of the transmitted packet.
3	RSVD	R0	0	Reserved − A write to this location has no effect. A read returns 0.
2:0	ACKCNT	R	0	ACK count – This binary encoded value represents the number of ACKS currently available within the ACK FIFO.

0x248 TXDPINT – Transmit Data Path Interrupts				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:28	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
27	ERRASYTX	RCU	0	Asynchronous transmit error – This bit is set by hardware when the number of retries (defined in the TxDPCTL.ATRETRYMAX field) has expired, an error acknowledge code was returned, or an illegal tCode was written into the asynchronous header register.
26	ACKLOST	RCU	0	Acknowledge lost – This bit is set by hardware when the ACK buffer has an overrun condition.
25	ACKRCVD	RCU	0	Acknowledge received – When this bit is set to 1 by hardware, an ACK has been written to the ACK FIFO by the TXDP. When this bit is set and the TXDPINTEN.ACKRCVD bit is set, an interrupt is generated.
24	ERRISOTX	RCU	0	Isochronous transmit error – When this bit is set to 1 by hardware, the TXDP has detected an error in an attempted isochronous transmission. The error was caused by an illegal tCode or by the fact that the data length of the actual packet does not equal the data length field in the isochronous header.
23	ERRBFLSH0	RCU	0	Buffer 0 flushed due to an error – When this bit is set to 1 by hardware, the TXDP has flushed the transmit buffer due to an error. This only occurs when TXDP(N)CFG.BUFFLSHEN is set to 1.

0x248 TXDPINT – Transmit Data Path Interrupts (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
22	ERRBFLSH1	RCU	0	Buffer 1 flushed due to an error − When this bit is set to 1 by hardware, the TXDP has flushed the transmit buffer due to an error. This only occurs when TXDP(N)CFG.BUFFLSHEN is set to 1.
21	ERRBFLSH2	RCU	0	Buffer 2 flushed due to an error− When this bit is set to 1 by hardware, the TXDP has flushed the transmit buffer due to an error. This only occurs when TXDP(N)CFG.BUFFLSHEN is set to 1.
20	ERRBFLSH3	RCU	0	Buffer 3 flushed due to an error − When this bit is set to 1 by hardware, the TXDP has flushed the transmit buffer due to an error. This only occurs when TXDP(N)CFG.BUFFLSHEN is set to 1.
19	ERRDBC0	RCU	0	Buffer 0 DBC error − When this bit is set to 1 by hardware, the TXDP has detected a data block continuity error in an MPEG/DV packet.
18	ERRDBC1	RCU	0	Buffer 1 DBC error − When this bit is set to 1 by hardware, the TXDP has detected a data block continuity error in an MPEG/DV packet.
17	ERRDBC2	RCU	0	Buffer 2 DBC error − When this bit is set to 1 by hardware, the TXDP has detected a data block continuity error in an MPEG/DV packet.
16	ERRDBC3	RCU	0	Buffer 3 DBC error − When this bit is set to 1 by hardware, the TXDP has detected a data block continuity error in an MPEG/DV packet.
15	ERRTH0_0	RCU	0	Buffer 0 transmit header error − When this bit is set to 1 by hardware, the TXDP has detected an error in the transmit packet header.
14	ERRTH0_1	RCU	0	Buffer 1 transmit header error − When this bit is set to 1 by hardware, the TXDP has detected an error in the transmit packet header.
13	ERRTH0_2	RCU	0	Buffer 2 transmit header error − When this bit is set to 1 by hardware, the TXDP has detected an error in the transmit packet header.
12	ERRTH0_3	RCU	0	Buffer 3 transmit header error − When this bit is set to 1 by hardware, the TXDP has detected an error in the transmit packet header.
11	ERRBFLSH4	RCU	0	Buffer 4 flushed due to an error − When this bit is set to 1 by hardware, the TXDP has flushed the transmit buffer due to an error. This only occurs when TXDP(N)CFG.BUFFLSHEN is set to 1.
10	ERRBFLSH5	RCU	0	Buffer 5 flushed due to an error − When this bit is set to 1 by hardware, the TXDP has flushed the transmit buffer due to an error. This only occurs when TXDP(N)CFG.BUFFLSHEN is set to 1.
9	ERRBFLSH6	RCU	0	Buffer 6 flushed due to an error − When this bit is set to 1 by hardware, the TXDP has flushed the transmit buffer due to an error. This only occurs when TXDP(N)CFG.BUFFLSHEN is set to 1.
8	ERRBFLSH7	RCU	0	Buffer 7 flushed due to an error − When this bit is set to 1 by hardware, the TXDP has flushed the transmit buffer due to an error. This only occurs when TXDP(N)CFG.BUFFLSHEN is set to 1.
7	ERRDBC4	RCU	0	Buffer 4 DBC error − When this bit is set to 1 by hardware, the TXDP has detected a data block continuity error in an MPEG/DV packet.
6	ERRDBC5	RCU	0	Buffer 5 DBC error − When this bit is set to 1 by hardware, the TXDP has detected a data block continuity error in an MPEG/DV packet.

0x248 TXDPINT – Transmit Data Path Interrupts (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
5	ERRDBC6	RCU	0	Buffer 6 DBC error − When this bit is set to 1 by hardware, the TXDP has detected a data block continuity error in an MPEG/DV packet.
4	ERRDBC7	RCU	0	Buffer 7 DBC error − When this bit is set to 1 by hardware, the TXDP has detected a data block continuity error in an MPEG/DV packet.
3	ERRTH0_4	RCU	0	Buffer 4 transmit header error − When this bit is set to 1 by hardware, the TXDP has detected an error in the transmit packet header.
2	ERRTH0_5	RCU	0	Buffer 5 transmit header error − When this bit is set to 1 by hardware, the TXDP has detected an error in the transmit packet header.
1	ERRTH0_6	RCU	0	Buffer 6 transmit header error − When this bit is set to 1 by hardware, the TXDP has detected an error in the transmit packet header.
0	ERRTH0_7	RCU	0	Buffer 7 transmit header error − When this bit is set to 1 by hardware, the TXDP has detected an error in the transmit packet header.

0x24C TXDPINTEN – Transmit Data Path Interrupt Enable				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:28	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
27	ERRASYTX	RW	0	Asynchronous transmit error interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT1 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT1 bit.
26	ACKLOST	RW	0	Acknowledge lost interrupt enable – When this bit is set to 1, the SYSINT.TXDPINT1 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT1 bit.
25	ACKRCVD	RW	0	ACKRCVD interrupt enable – When this bit is set to 1, the SYSINT.TXDPINT1 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT1 bit.
24	ERRISOTX	RW	0	ERRISOTX interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT1 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT1 bit.
23	ERRBFLSH0	RW	0	ERRBFLSH0 interrupt enable – When this bit is set to 1, the SYSINT.TXDPINT1 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT1 bit.
22	ERRBFLSH1	RW	0	ERRBFLSH1 interrupt enable – When this bit is set to 1, the SYSINT.TXDPINT1 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT1 bit.
21	ERRBFLSH2	RW	0	ERRBFLSH2 interrupt enable – When this bit is set to 1, the SYSINT.TXDPINT1 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT1 bit.
20	ERRBFLSH3	RW	0	ERRBFLSH3 interrupt enable – When this bit is set to 1, the SYSINT.TXDPINT1 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT1 bit.

0x24C TXDPINTEN – Transmit Data Path interrupt enable (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
19	ERRDBC0	RW	0	ERRDBC0 interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT1 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT1 bit.
18	ERRDBC1	RW	0	ERRDBC1 interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT1 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT1 bit.
17	ERRDBC2	RW	0	ERRDBC2 interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT1 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT1 bit.
16	ERRDBC3	RW	0	ERRDBC3 interrupt enable −When this bit is set to 1, the SYSINT.TXDPINT1 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT1 bit.
15	ERRTH0_0	RW	0	ERRTH0_0 interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT0 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT0 bit.
14	ERRTH0_1	RW	0	ERRTH0_1 interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT0 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT0 bit.
13	ERRTH0_2	RW	0	ERRTH0_2 interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT0 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT0 bit.
12	ERRTH0_3	RW	0	ERRTH0_3 interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT0 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT0 bit.
11	ERRBFLSH4	RW	0	ERRBFLSH4 interrupt enable – When this bit is set to 1, the SYSINT.TXDPINT0 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT0 bit.
10	ERRBFLSH5	RW	0	ERRBFLSH5 interrupt enable – When this bit is set to 1, the SYSINT.TXDPINT0 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT0 bit.
9	ERRBFLSH6	RW	0	ERRBFLSH6 interrupt enable – When this bit is set to 1, the SYSINT.TXDPINT0 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT0 bit.
8	ERRBFLSH7	RW	0	ERRBFLSH7 interrupt enable – When this bit is set to 1, the SYSINT.TXDPINT0 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT0 bit.
7	ERRDBC4	RW	0	ERRDBC4 interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT0 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT0 bit.

0x24C TXDPINTEN – Transmit Data Path interrupt enable (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
6	ERRDBC5	RW	0	ERRDBC5 interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT0 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT0 bit.
5	ERRDBC6	RW	0	ERRDBC6 interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT0 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT0 bit.
4	ERRDBC7	RW	0	ERRDBC7 interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT0 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT0 bit.
3	ERRTH0_4	RW	0	ERRTH0_4 interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT0 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT0 bit.
2	ERRTH0_5	RW	0	ERRTH0_5 interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT0 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT0 bit.
1	ERRTH0_6	RW	0	ERRTH0_6 interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT0 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT0 bit.
0	ERRTH0_7	RW	0	ERRTH0_7 interrupt enable − When this bit is set to 1, the SYSINT.TXDPINT0 bit is set to 1 when the corresponding bit in the TXDPINT register is set by hardware. When set to 0, the corresponding bit in the TXDPINT register has no effect on the SYSINT.TXDPINT0 bit.

0x250 0x268 0x280 0x298 0x2B0 0x2C8 0x2E0 0x2F8				
TXDP(N)CFG – Transmit Data Path Buffer #N Configuration				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:12	RSVD	R0	0	Reserved − A write to this location has no effect. A read returns 0s.
11	SPH_NEWCELL	RW	0	SPH new cell − When this bit is set to 1, the SPH bit is set only if a DirecTV/DVB packet contains a time stamp. When this bit is set to 0, the SPH bit is set to a static value according to bit 10 in the TXDP(N)H1 register, of a video formatted transmit data buffer.
10	INTSSP	RW	0	Insert time stamp only into source packets – Valid in DV mode only. When this bit is set to 1, DV time stamps are not inserted into empty packets.
9	VHFWEN	RW	0	Video header field write enable − When this bit is set to 1, the read-only fields in the video formatted TXDP header registers can be read or written by software.

0x250 0x268 0x280 0x298 0x2B0 0x2C8 0x2E0 0x2F8				
TXDP(N)CFG – Transmit Data Path Buffer #N Configuration				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
8	BFLUSHEN	RW	0	Buffer flush enable – TXDP is enabled to flush the associated buffer when error conditions warrant. These conditions are as follows: ISO format related flush conditions: − Invalid (any other than A) tCode detected in ISO header. − Data length field in ISO header is set to 0. Async/async-streaming format related flush condition: − Invalid (8, C or any undefined) tCode detected in the async header. NOTE: Not only does the last data packet get flushed but also the complete contents of the dedicated Tx buffer.
7	FAIRARB_OFF	RW	0	Fair arbitration off – Disables fair arbitration for the buffer selection. Natural priority of the buffer always takes precedence.
6	HIM	RW	DEP	Header insert mode – When this bit is set to 1, packet type-specific headers are inserted in the transmit packet. The buffer dependent default values are as follows: Buffer# Value 0 1 1−7 0
5	H0IM	RW	0	Header zero insert mode – In a DV mode when this bit is set to 1, DIF block H0 is inserted by hardware.
4	EPINSRT	RW	DEP	Empty packet insert test mode – Should be set to 0 for DV applications.
3	DVTXSUB	RW	0	DV transmit sub mode select. (Valid in DV mode only) 0 – Send a full source packet (480/960 bytes + CIP) 1 – Send only empty packets.
2:0	MPEG2TXCLASS	RW	DEP	MPEG transmit class selection – The binary encoded value in this register programs the MPEG class for the associated buffer. The values in this field only have meaning when DVB or DirecTV is selected in DB(N)CFG0.STREAMTYPE. The MPEG2 classes are discussed in Table 5−15. The DirecTV classes are discussed in Table 5−16. Only DB0CFG0.STREAMTYPE is set to DVB after reset. The defaults for these fields are as follows: Buffer0 – 011 : Configured for MPEG TX class 3 at reset Buffer1 – 000 : No meaning at reset Buffer2 – 000 : No meaning at reset Buffer3 – 000 : No meaning at reset Buffer4 – 000 : No meaning at reset Buffer5 – 000 : No meaning at reset Buffer6 – 000 : No meaning at reset Buffer7 – 000 : No meaning at reset

6.7.1 TXDP Header Register Descriptions

The TXDP header registers have meaning only when the associated transmit path is being used in header insert mode. The header fields for various 1394 and video mode specific formats are provided via these registers. The default values for these registers match the default stream types for the data buffers. If the data buffer stream type is changed from the default configuration, then the TXDP header registers must be programmed to reflect the new stream type. All RW bits in these registers must be configured by software to the appropriate mode specific values. All RU registers can be made writeable by setting the TXDP(N)CFG.VHFWEN bit to 1.

0x254 0x26C 0x284 0x29C 0x2B4 0x2CC 0x2E4 0x2FC				
TXDP(N)H0 – When associated buffer is configured for stream type 1 (Async) DEFAULT CONFIGURATION FOR BUFFER 4				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:18	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
17:16	SPD	RW	0	Speed code – This 2-bit value represents the IEEE-1394 speed code to be provided in the header of the transmitted packet.
15:10	TLABEL	RW	0	Transaction label – This 6-bit value contains the IEEE-1394 transaction label to be provided in the header of the transmitted packet.
9:8	RT	RW	0	Retry code – This two-bit value contains the IEEE-1394 retry code to be provided in the header of the transmitted packet.
7:4	TCODE	RW	0	Transaction code − This 4-bit value contains the IEEE-1394 transaction code to be provided in the header of the transmitted packet.
3:0	PRIORITY	RW	0	Priority – This 4-bit field contains the IEEE-1394 priority value to be provided in the header of the transmitted packet transmitted packet.
TXDP(N)H0 – When associated buffer is configured for stream types: 3 (Async Streams) DEFAULT CONFIGURATION FOR BUFFER 2				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:16	DATALENGTH	RW	0	Data length – This field represents the data_length to be provided in the header of the transmitted packet.
15:14	TAG	RW	0	TAG – This field contains the TAG value to be provided in the header of the transmitted packet.
13:8	CHANNUM	RW	0	Channel number – This field contains the channel number to be provided in the header of the transmitted packet.
7:6	RSVD	R0	0	Reserved − A write to this location has no effect. A read returns 0s.
5:4	SPD	RW	0	Speed code – This field contains the speed code to be used for the transmitted packet.
3:0	SYNC CODE	RW	0	Synchronization code – This field contains the synchronization code to be provided in the header of the transmitted packet.

0x254 0x26C 0x284 0x29C 0x2B4 0x2CC 0x2E4 0x2FC (Continued)				
TXDP(N)H0 – When associated buffer is configured for stream types; 4−10 (VIDEO) DEFAULT CONFIGURATION FOR BUFFER 0				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:16	DATALENGTH	RU	0	Data length – This field represents the data length of the transmitted packet. This read only value is determined by hardware depending on the MPEG class.
15:14	TAG	RW	1	TAG – This field contains the TAG value to be provided in the header of the transmitted packet.
13:8	CHANNUM	RW	0	Channel number – This field contains the channel number to be provided in the header of the transmitted packet.
7:6	RSVD	R0	0	Reserved − A write to this location has no effect. A read returns 0s.
5:4	SPD	RW	1	Speed code – This field contains the speed code to be used for the transmitted packet.
3:0	SYNC CODE	RW	0	Synchronization code – This field contains the synchronization code to be provided in the header of the transmitted packet.

0x258 − 0x270 0x288 0x2A0 0x2B8 0x2D0 0x2E8 0x300				
TXDP(N)H1 – When associated buffer is configured for stream type 1 (ASYNC) DEFAULT CONFIGURATION FOR BUFFER 4				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:16	DESTID	RW	0	Destination ID – This field contains the destination ID to be provided in the header of the transmitted async packet.
15:0	DESTOFFHI	RW	0	Destination offset high – This field contains the upper 16 bits of the destination offset to be provided in the header of the transmitted async packet.
TXDP(N)H1 – When associated buffer is configured for stream type 4−10 (all Video modes) DEFAULT CONFIGURATION FOR BUFFER 0				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:29	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
28:24	SRCID	RU	0	Source node ID – This field contains the source ID to be provided with the transmitted header. This value is updated with each PHY register 0 transfer.
23:16	DBS	RU	DEP	Data block size – This field contains the size of the transmitted data blocks. The value of this field varies according to the stream type of the associated buffer. Stream type — Data block size DVB — 6 DirecTV — 9 SD — 78 (Standard definition digital video) HD — F0 (High definition digital video) The default values for individual buffers is as follows: Buffer# — Value 0 — 6 1−7 — 0

0x258 − 0x270 0x288 0x2A0 0x2B8 0x2D0 0x2E8 0x300 (Continued)				
TXDP(N)H1 – When associated buffer is configured for stream type 4−10 (all Video modes) DEFAULT CONFIGURATION FOR BUFFER 0				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
15:14	FN	RU	DEP	Fraction number – This field indicates the number of 1394 packets required to send one complete video cell. This field represents the FN value provided in the CIP header of the transmitted packet. The encoding of this field is used as follows: 00 – Cell is not divided 01 – Cell is divided into two data blocks 10 – Cell is divided into four data blocks 11 – Cell is divided into eight data blocks The default values for individual buffers is as follows; Buffer# Value 0 3 1−7 0
13:11	QPC	R0	0	Quadlet padding count – This field represents the QPC value provided in the CIP header of the transmitted packet.
10	SPH	RW RU†	DEP	Source packet header – This field represents the SPH value provided in the CIP header of the transmitted packet. The buffer dependent default values are as follows: Buffer# Value 0 1 1−7 0
9:8	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
7:0	DBCC	RU	0	Data block continuity counter – This field represents the countinuity counter value provided in the CIP header of the transmitted packet.

† Read only if SPH_NEWCELL is activated.

0x25C 0x274 0x28C 0x2A4 0x2BC 0x2D4 0x2EC 0x304				
TXDP(N)H2 – When associated buffer is configured for stream type 1 (ASYNC) DEFAULT CONFIGURATION FOR BUFFER 4				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:0	DESTOFFLOW	RW	0	Destination offset low − This field contains the lower 32 bits of the destination offset to be provided in the header of the transmitted packet.
TXDP(N)H2 – When associated buffer is configured for stream types: 4 − 6 (DirecTV 130, DirecTV 140, DVB) DEFAULT CONFIGURATION FOR BUFFER 0				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	RSVD	R1	0	Reserved – A write to this location has no effect. A read returns 1.
30	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
29:24	FMT	RU	DEP	Format type – This field contains the format type value provided with the CIP1 header of the transmitted packet. The default values for individual buffers is as follows; Buffer# Value 0 20 1−7 00
23:0	FDF	RW	0	Format dependent field − This field contains the format dependent value. Bit 23 represents the TSF (time shift flag). Bits 22−0 are all zeros.

0x25C 0x274 0x28C 0x2A4 0x2BC 0x2D4 0x2EC 0x304 (Continued)				
TXDP(N)H2 – When associated buffer is configured for stream types 7−10; (PALSD, PALHD, NTSCSD, NTSCHD) NO BUFFERS DEFAULT TO THIS CONFIGURATION				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	RSVD	R1	0	Reserved – A write to this location has no effect. A read returns 1.
30	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0.
29:24	FMT	RU	0	Format type – This field contains the format type value provided with the CIP1 header of the transmitted packet.
23	50/60	RU	0	This field contains the 50/60 flag provided with the CIP1 header of the transmitted packet.
22:18	STYPE	RU	0	Signal type – This field contains the signal type value provided with the CIP1 header of the transmitted packet.
17:16	RSVD	R0	0	Reserved − A write to this location has no effect. A read returns 0s.
15:0	SYT	RU	0	SYT – This field contains the SYT value provided with the CIP1 header of the transmitted packet.

0x260 0x278 0x290 0x2A8 0x2C0 0x2D8 0x2F0 0x308				
TXDP(N)H3 − When associated buffer is configured for stream type 1 (ASYNC) DEFAULT CONFIGURATION FOR BUFFER 4				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:16	DATALENGTH	RW	0	Data length – The data length value for the 1394 header must be written into this field when header insert mode is used.
15:0	EXTTCODE	RW	0	Extended TCODE – The extended TCODE value for the 1394 header is written to this location for use in header insert mode.
TXDP(N)H3 − When associated buffer is configured for stream type 4 (DirecTV 130) NO BUFFERS DEFAULT TO THIS CONFIGURATION				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:0	DirecTV130_1	RW	0	DirecTV 130 header 1 – DSS130 header fields starting with the reserved byte 1 and continuing through reserved byte 4 may be set by software by accessing this field.
TXDP(N)H3 − When associated buffer is configured for stream type 7−10 (DV) NO BUFFERS DEFAULT TO THIS CONFIGURATION				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:0	DVH0	RW	0	DV header 0 – The DV header 0 field is provided by software in this location.

0x264 0x27C 0x294 0x2AC 0x2C4 0x2DC 0x2F4 0x30C				
TXDP(N)H4 − When associated buffer is configured for stream type 7−10 (DV)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:0	DVH1	RW	0	DV header 1 – The DVH1 field is provided by software in this location.

0X310 TXDPDVABRST − Transmit Data Path A Burst				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:30	VA_DV_BURST	RW	0	Video A DV burst mode − 00: Burst mode disabled 01: frame delay enabled / smooth mode disabled 10: frame delay enabled / manual smooth mode 11: frame delay enabled / auto smooth mode
29:25	VA_DV_EPGAP	RW	0	Video A DV empty packet gap − Defines the number of source packets that is sent, before the next empty packet is inserted. Valid only if VA_DV_BURST=10. Set to 0 − The empty packet gap depends on the value of VA_DV_EPNUM.
24:20	VA_DV_EPNUM	RW	0	Video A DV empty packet number − Defines the number of empty packets which is inserted additionally within a frame. Valid only if VA_DV_BURST=10.
19:0	VA_DV_DELAY	RW	0	Video A DV frame delay − Defines the number of SCLK cycles that occur before the first source packet of a new frame is sent. Valid only if VA_DV_BURST is not set to 0.

0X314 TXDPDVBBRST − Transmit Data Path B Burst				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:30	VB_DV_BURST	RW	0	Video B DV burst mode − 00: Burst mode disabled 01: frame delay enabled / smooth mode disabled 10: frame delay enabled / manual smooth mode 11: frame delay enabled / auto smooth mode
29:25	VB_DV_EPGAP	RW	0	Video B DV empty packet gap − Defines the number of source packets that is sent, before the next empty packet is inserted. Valid only if VB_DV_BURST=10. Set to 0 − The empty packet gap depends on the value of VB_DV_EPNUM.
24:20	VB_DV_EPNUM	RW	0	Video B DV empty packet number − Defines the number of empty packets which are additionally inserted within a frame. Valid only if VB_DV_BURST=10.
19:0	VB_DV_DELAY	RW	0	Video B DV frame delay − Defines the number of SCLK cycles that occur before the first source packet of a new frame is sent. Valid only if VB_DV_BURST is not set to 0.

6.8 Receive Data Path CFR Map

Address	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	RXDP CFR Name (Hex Reset Value)
340h	SOFTRSTB	SOFTRSTA									DVABTTOUT	DVABTSEQER	DVSPLITB	DVSPLITA	DVH0ONLYB	DVH0ONLYA	RSPBUFADDR				ABTDBCERR		DBCRST_B	DBCRST_A	DBCCRST_B	DBCCRST_A	EMPTPKTBEN	EMPTPKTAEN	FLUSHDCRERR		RXSIDFULL	ACKTARDYEN	BSYALLPKTS	RXDPCTL (0030_1020h)
344h																	STATEVODB	STATEVODA	STATEMIB		STATEMIA											VIDSELERR	RXDPSTAT (0000_0000h)
348h	PKTRCVERR7	PKTRCVERR6	PKTRCVERR5	PKTRCVERR4	PKTRCVERR3	PKTRCVERR2	PKTRCVERR1	PKTRCVERR0	PKTRCVD7	PKTRCVD6	PKTRCVD5	PKTRCVD4	PKTRCVD3	PKTRCVD2	PKTRCVD1	PKTRCVD0	EVODCHNGB	EVODCHNGA	EMIERRB	EMIERRA	DVSPLITERRB	DVSPLITERRA	DVSEQERRB	DVSEQERRA		SNTRJCT	DATACRCERR	BUFADDRERR	PKTTYPERR	BSYREQ	CMDRSTRCVD	SIDEND	RXDPINT (0000_0000h)
34Ch	PKTRCVERR7	PKTRCVERR6	PKTRCVERR5	PKTRCVERR4	PKTRCVERR3	PKTRCVERR2	PKTRCVERR1	PKTRCVERR0	PKTRCVD7	PKTRCVD6	PKTRCVD5	PKTRCVD4	PKTRCVD3	PKTRCVD2	PKTRCVD1	PKTRCVD0	EVODCHNGB	EVODCHNGA	EMIERRB	EMIERRA	DVSPLITERRB	DVSPLITERRA	DVSEQERRB	DVSEQERRA		SNTRJCT	DATACRCERR	BUFADDRERR	PKTTYPERR	BSYREQ	CMDRSTRCVD	SIDEND	RXDPINTEN (0000_0000h)
350h 364h 378h 38Ch 3A0h 3B4h 3C8h 3DCh																								INVERTSTRIP		ACKPEND	INSERTPKTTOKEN	STRIPHDR0	STRIPHDR1	STRIPHDR2	STRIPHDR3		RXDP(N)CFG0 (0000_0020h) (0000_0020h) (0000_0020h) (0000_0020h) (0000_0020h) (0000_0020h) (0000_0030h) (0000_0030h) (0000_0020h)
354h 368h 37Ch 390h 3A4h 3B8h 3CCh 3E0h																						RCVPHYPKT	RCVSELFID	BROADCAST	RCVALLADDR	INITIALMEMLO	INITIALMEMHI	PRIVATE	CSR	SERBUS	ROM	INITUNIT		RXDP(N)CFG1 (0000_0080h) (0000_0080h) (0000_0080h) (0000_0080h) (0000_0080h) (0000_0080h) (0000_0780h) (0000_0080h)
358h 36Ch 380h 394h 3A8h 3BCh 3D0h 3E4h	SRCIDFILTER MASK																SRCIDFILTER																RXDP(N)CFG2 (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h)

Address	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	RXDP CFR Name (Hex Reset Value)
35Ch 370h 384h 398h 3ACh 3C0h 3D4h 3E8h	LOWER 16 BIT HEADER0 MASK																LOWER 16 BIT HEADER0 FILTER																RXDP(N)CFG3 (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h)
360h 374h 388h 39Ch 3B0h 3C4h 3D8h 3ECh	DATALENGTH_MASK																DATALENGTH_FILTER																RXDP(N)CFG4 (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h) (0000_0000h)
3F0-3FFh																																	RSVD (0000_0000h)

6.8.1 RXDP Bit Descriptions

0x340 RXDPCTL − Receive Data Path Control				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31	SOFTRSTB	RWU	0	Receive data path B soft reset – When this bit is set to 1, the receive data path state machine and stream B, affecting the hardware, are synchronously reset. This bit is self-clearing.
30	SOFTRSTA	RWU	0	Receive data path A soft reset – When this bit is set to 1, the receive data path state machine and stream A, affecting the hardware, are synchronously reset. This bit is self-clearing.
29:22	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
21	DVABTTOUT	RW	1	Digital video abort on timeout − If this bit is set to 1, the receiver ignores incoming data after timeout until the next frame starts.
20	DVABTSEQER	RW	1	Digital video abort on sequence error − When this bit is set to 1, if a discontinuous DV sequence occurs, all DV packets is ignored until the next start of frame.
19	DVSPLITB	RW	0	Digital video split stream B − When this bit is set to 1, it enables receiving the DV headers for DV stream B into a separate buffer.
18	DVSPLITA	RW	0	Digital video split stream A − When this bit is set to 1, it enables receiving the DV headers for DV stream A into a separate buffer.
17	DVH0ONLYB	RW	0	Digital video HO header only stream B − When this bit is set to 1, it enables the receiving DV headers only mode for stream B.
16	DVH0ONLYA	RW	0	Digital video HO header only stream A − When this bit is set to 1, it enables the receiving DV headers only mode for stream A.
15:13	RSPBUFADDR	RW	000	When REMOTEEN is set to 1, all response packets generated after a quadlet write/read request are written to the buffer specified in this bit field. In order to transmit the response packet, this buffer needs to be configured for asynchronous transmit.
12	ABTDBCER	RW	1	Abort on DBC error – An entire MPEG cell or DV frame has been aborted due to a DBC counter error.
11	DBCRST_B	R0W	0	Data block counter B reset − Writing a 1 to this location causes data block counter B to be synchronously reset. This bit is self-clearing.
10	DBCRST_A	R0W	0	Data block counter A reset − Writing a 1 to this location causes data block counter A to be synchronously reset. This bit is self-clearing.

0x340 RXDPCTL − Receive Data Path Control (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
9	DBCCRST_B	R0W	0	Data block continuity counter reset B − Writing a 1 to this location causes data block continuity counter B to be synchronously reset. This bit is self-clearing.
8	DBCCRST_A	R0W	0	Data block continuity counter reset A − Writing a 1 to this location causes data block continuity counter A to be synchronously reset. This bit is self-clearing.
7	EMPTPKTBEN	RW	0	Empty packet B receive enable – Setting this bit to 1 enables empty packets of video stream B to be received.
6	EMPTPKTAEN	RW	0	Empty packet A receive enable – Setting this bit to 1 enables empty packets of video stream A to be received.
5	FLUSHDCRCERR	RW	1	Abort on data CRC error – When this bit is set by hardware, incoming packets that contain a data CRC error are automatically aborted and flushed from the associated buffer.
4:3	RSVD	RW	0	Reserved – A write to this location has no effect. A read returns 0s.
2	RXSIDFULL	RW	0	Receive full self-ID packets – Setting this bit to 1 enables both self-ID packet quadlets to be written into the buffer.
1	ACKTARDYEN	RW	0	Ack tardy enable – Setting this bit to 1 causes all incoming asynchronous 1394 packets to be acknowledged with an ACK_tardy (B) acknowledge unless RXDPCTL.BSYALLPKTS is set to 1.
0	BSYALLPKTS	RW	0	Busy all packets – Setting this bit to 1 causes all incoming asynchronous 1394 packets to be acknowledged with an ACK_busy_x (4) acknowledge. This bit overrides the function of RXDPCTL.ACKTARDYEN.

0x344 RXDPSTAT – Receive Data Path Status				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:16	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
15:14	STATEMIB	R	0	State encryption mode indicator stream B − Shows the EMI status of the MPEG stream B.
13:12	STATEMIA	R	0	State encryption mode indicator stream A − Shows the EMI status of the MPEG stream A.
11	STATEVODA	R	0	State even/odd bit stream A − This even/odd bit stream is extracted from the header of DVB and DirecTV source packets. It is updated with each packet.
10	STATEVODB	R	0	State even/odd bit stream B − This even/odd bit stream is extracted from the header of DVB and DirecTV source packets. It is updated with each packet.
9:1	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
0	VIDSELERR	RU	0	Video select error – This bit is set by hardware to indicate that two buffers are configured as video type A or B at the same time. This error indication clears itself when the conflict is resolved.

0x348 RXDPINT − Receive Data Path Interrupts				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:24	PKTRCVERR(N)	RCU	0	Packet receive error − There is an indication for each of the eight buffers which is set to 1 whenever a 1394 packet is aborted.
23:16	PKTRCVD(N)	RCU	0	Packet received – There is an indication for each of the eight buffers which is set to 1 whenever a 1394 packet is confirmed into the corresponding buffer.
15	EVODCHNGB	RCU	0	Even/odd bit change stream B − Set to 1 when the even/odd bit for stream B changes.
14	EVODCHNGA	RCU	0	Even/odd bit change stream A − Set to 1 when the even/odd bit for stream A changes.
13	EMIERRB	RCU	0	Encryption mode indicator error stream B − When the detected EMI setting is different from the EMI setting in the cipher, this bit is set to 1 to indicate an EMI error.
12	EMIERRA	RCU	0	Encryption mode indicator error stream A − When the detected EMI setting is different from the EMI setting in the cipher, this bit is set to 1 to indicate an EMI error.
11	DVSPLITERRB	RCU	0	Digital video split error stream B − Set to 1 when an error occurs when receiving DV headers for DV stream B into a separate buffer.
10	DVSPLITERRA	RCU	0	Digital video split error stream A − Set to 1 when an error occurs when receiving DV headers for DV stream A into a separate buffer.
9	DVSEQERRB	RCU	0	Digital video sequence error stream B − Set to 1 when a sequence error is detected in stream B.
8	DVSEQERRA	RCU	0	Digital video sequence error stream A − Set to 1 when a sequence error is detected in stream A.
7	RSVD	RW	0	Reserved – A write to this location has no effect. A read returns 0.
6	SNTRJCT	RCU	0	Sent reject − Set to 1 when a received packet has been acknowledged with the ACK_BUSY_X.
5	DATACRCERR	RCU	0	Data CRC error − This bit is set to 1 by hardware when the data CRC check failed for a receive packet.
4	BUFADDRERR	RCU	0	Buffer address error – Set to 1 when a packet has been received but no valid buffer address could be generated. The packet was aborted.
3	PKTTYPERR	RCU	0	Packet type error – Set to 1 when a 1394 packet with an illegal tCode is received and aborted.
2	BSYREQ	RCU	0	Busy requested – This bit is set to 1 by hardware to indicate that a receive packet was busied off because the receive state machines were not idle when the start of reception was detected.
1	CMDRSTRCVD	RCU	0	Command reset received − When CMDRSTRCVD is set to 1, the link has received a 1394 quadlet write request to the Reset_Start CSR register (target address is FFFF_F000_000Ch)
0	SIDEND	RCU	0	Self-ID end − Set to 1 when the self-ID phase is over and all self-ID packets have been confirmed into the FIFO.

0x34C RXDPINTEN − Receive Data Path Interrupt Enables				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:24	PKTRCVERR(N)	RW	0	Packet receive error – When this bit is set to 1, the SYSINT.RXDPINT1 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT1 bit.
23:16	PKTRCVD(N)	RW	0	Packet received − When this bit is set to 1, the SYSINT.RXDPINT1 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT1 bit.
15	EVODCHNGB	RW	0	Even/odd bit change stream B − When this bit is set to 1, the SYSINT.RXDPINT0 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT0 bit.
14	EVODCHNGA	RW	0	Even/odd bit change stream A − When this bit is set to 1, the SYSINT.RXDPINT0 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT0 bit.
13	EMIERRB	RW	0	Encryption mode indicator error stream B − When this bit is set to 1, the SYSINT.RXDPINT0 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT0 bit.
12	EMIERRA	RW	0	Encryption mode indicator error stream A − When this bit is set to 1, the SYSINT.RXDPINT0 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT0 bit.
11	DVSPLITERRB	RW	0	Digital video split error stream B − When this bit is set to 1, the SYSINT.RXDPINT0 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT0 bit.
10	DVSPLITERRA	RW	0	Digital video split error stream A − When this bit is set to 1, the SYSINT.RXDPINT0 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT0 bit.
9	DVSEQERRB	RW	0	Digital video sequence error stream B − When this bit is set to 1, the SYSINT.RXDPINT0 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT0 bit.
8	DVSEQERRA	RW	0	Digital video sequence error stream A − When this bit is set to 1, the SYSINT.RXDPINT0 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT0 bit.
7	RSVD	RW	0	Reserved – A write to this location has no effect. A read returns 0.

0x34C RXDPINTEN − Receive Data Path Interrupt Enables (Continued)				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
6	SNTRJCT	RW	0	Sent reject interrupt enable – When this bit is set to 1, the SYSINT.RXDPINT0 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT0 bit.
5	DATACRCERR	RW	0	Data CRC error interrupt enable − When this bit is set to 1, the SYSINT.RXDPINT0 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT0 bit.
4	BUFADDRERR	RW	0	Buffer address error – When this bit is set to 1, the SYSINT.RXDPINT0 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT0 bit.
3	PKTTYPERR	RW	0	Packet type error – When this bit is set to 1, the SYSINT.RXDPINT0 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT0 bit.
2	BSYREQ	RW	0	Busy requested − When this bit is set to 1, the SYSINT.RXDPINT0 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT0 bit.
1	CMDRSTRCVD	RW	0	Command reset received − When this bit is set to 1, the SYSINT.RXDPINT0 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT0 bit.
0	SIDEND	RCU	0	Self ID end interrupt enable − When this bit is set to 1, the SYSINT.RXDPINT0 bit is set to 1 when the corresponding bit in the RXDPINT register is set by hardware. When set to 0, the corresponding bit in the RXDPINT register has no effect on the SYSINT.RXDPINT0 bit.

RXDP(N)CFG0 – Receive Data Path Buffer #N Configuration 0				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:9	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
8	INVERTSTRP	RW	0	Invert striping – When this bit is set to 1, only the header quadlets programmed to be stripped in RXBUF(N)CFG0.STRIPHDR(0−3) are written to the receive buffer. Packet control token insertion is not affected by this mode.
7:6	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
5	ACKPEND	RW	1	Ack pending – Writing a 1 to this location causes all 1394 write request packets to be acknowledged with ACK_PENDING (2). When this bit is set to 0 ACK_COMPLETE is generated.
4	INSERTPKTTOKEN	RW	DEP	Insert packet control token – Writing a 1 to this bit causes a packet control token quadlet to be attached to all incoming packets. This enable is ignored for self-ID and other PHY packets. RXDB5CFG0.INSERTPKTTOKEN and RXDB6CFG0.INSERTPKTTOKEN default to 1. This bit defaults to 0 for all other buffers.
3	STRIPHDR0	RW	0	Strip header 0 − Writing a 1 to this bit causes the first quadlet of an incoming 1394 packet to be stripped from the data stream and not written to the receive buffer with the other data.
2	STRIPHDR1	RW	0	Strip header 1 − Writing a 1 to this bit causes the second quadlet of an incoming 1394 packet to be stripped from the data stream and not written to the receive buffer with the other data.
1	STRIPHDR2	RW	0	Strip header 2 − Writing a 1 to this bit causes the third quadlet of an incoming 1394 packet to be stripped from the data stream and not written to the receive buffer with the other data.
0	STRIPHDR3	RW	0	Strip header 3 – Writing a 1 to this bit causes the fourth quadlet of an incoming 1394 packet to be stripped from the data stream and not written to the receive buffer with the other data.

0x354 0x368 0x37C 0x390 0x3A4 0x3B8 0x3CC 0x3E0				
RXDP(N)CFG1 – Receive Data Path Buffer #N Configuration 1				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:11	RSVD	R0	0	Reserved – A write to this location has no effect. A read returns 0s.
10	RCVPHYPKT	RW	DEP	Receive PHY packets enable – Setting this bit to 1 causes PHY packets to be routed to the corresponding buffer. RXDBGCFG1.RCVPHYPKT defaults to 1. This bit defaults to 0 for all other buffers.
9	RCVSELFID	RW	DEP	Receive self-ID – When set to 1, the corresponding buffer receives self-ID packets during the 1394 self-ID phase. RXDBGCFG1.RCVSELFID defaults to 1. This bit defaults to 0 for all other buffers.
8	BROADCAST	RW	DEP	Broadcast − When set to 1, only asynchronous packets with a destination ID of 3FFh is received in the associated buffer. RXDBGCFG1.BROADCAST defaults to 1. This bit defaults to 0 for all other buffers.
7	RCVALLADDR	RW	1	Receive all addresses – When set to 1, the corresponding buffer receives all asynchronous packets regardless of their destination address.
6	INITMEMLO	RW	0	Initial memory low − When INITMEMLO is set to 1, the corresponding buffer only receives asynchronous packets that have destination addresses within the lower half of the initial memory space, specified in IEEE-1394-1995 3.3. This bit is ignored if RcvAllAddr is set or when this buffer is configured for isochronous receive.
5	INITMEMHI	RW	0	Initial memory Hi − When INITMEMHI is set to 1, the corresponding buffer only receives asynchronous packets that have destination addresses within the upper half of the initial memory space, specified in IEEE-1394-1995 3.3. This bit is ignored if RcvAllAddr is set or when this buffer is configured for isochronous receive.
4	PRIVATE	RW	0	Private address offset − When PRIVATE is set to 1, the corresponding buffer only receives asynchronous packets, that have destination addresses within the private memory space, specified in IEEE-1394-1995 3.3. This bit is ignored if RcvAllAddr is set or when this buffer is configured for isochronous receive.
3	CSR	RW	0	Configuration and status register − When CSR is set to 1, the corresponding buffer only receives asynchronous packets that have destination addresses within the CSR architecture space, specified in IEEE-1394-1995 3.3. This bit is ignored, when RcvAllAddr is set or when this buffer is configured for isochronous receive.
2	SERBUS	RW	0	Serial bus − When SERBUS is set to 1, the corresponding buffer only receives asynchronous packets that have destination addresses within the serial bus space, specified in IEEE-1394-1995 3.3. This bit is ignored if RcvAllAddr is set or when this buffer is configured for isochronous receive.

0x354 0x368 0x37C 0x390 0x3A4 0x3B8 0x3CC 0x3E0 (Continued)				
RXDP(N)CFG1 – Receive Data Path Buffer #N Configuration 1				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
1	ROM	RW	0	Configuration ROM − When ROM is set to 1, the corresponding buffer only receives asynchronous packets that have destination addresses within the ROM space, specified in IEEE-1394-1995 3.3. This bit is ignored if RcvAllAddr is set or when this buffer is configured for isochronous receive.
0	INITUNIT	RW	0	Initial units space − When initial unit is set to 1, the corresponding buffer only receives asynchronous packets that have destination addresses within the initial units space, specified in IEEE-1394-1995 3.3. This bit is ignored if RcvAllAddr is set or when this buffer is configured for isochronous receive.

0x358 0x36C 0x380 0x394 0x3A8 0x3BC 0x3D0 0x3E4				
RXDP(N)CFG2 – Receive Data Path Buffer #N Configuration 2				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:16	SRCIDFILTER MASK	RW	0	Source ID filter mask – This field contains a bit pattern which masks certain bit positions of the 16-bit source ID of asynchronous packets. Default value: 0. Example: Mask: 16'b 0000_0000_0000_0001 Filter: 16'b 0000_0000_0000_0000 In this case only even source IDs are received. Mask: 16'b 0000_0000_0000_0000 Filter: 16'b 0000_0000_0000_0000 In this case every packet is received. Mask: 16'b 1111_1111_1111_1111 Filter: 16'b 0000_0000_0000_0100 In this case only packets with source ID 16'h4 are received.
15:0	SRCIDFLTR	RW	0	Source ID filter – This field contains the expected values at the bit positions specified in the mask field.

0x35C 0x370 0x384 0x398 0x3AC 0x3C0 0x3D4 0x3E8				
RXDP(N)CFG3 – Receive Data Path Buffer #N Configuration 3				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:16	HDR0LOMSK	RW	0	Header 0 lower 16 bit mask − This field contains a bit pattern which masks certain bit positions of the lower 16 bits of the first header quadlet of a packet.
15:0	HDR0LOFLTR	RW	0	Header 0 lower 16 bit filter − This field contains the expected values at the bit positions, specified in the mask field.

0x360 0x374 0x388 0x39C 0x3B0 0x3C4 0x3D8 0x3EC				
RXDP(N)CFG4 – Receive Data Path Buffer #N Configuration 4				
BIT	**NAME**	**TYPE**	**RESET**	**FUNCTION**
31:16	DATALENGTH_MASK	RW	0	Data length mask − This field contains a bit pattern which masks certain bit positions of the data length field of the incoming packet.
15:0	DATALENGTH_FILTER	RW	0	Data length filter − This field contains the expected values at the bit positions specified in the mask field.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings Over Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 4 V
Input voltage range, V_I . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} (TTL/LVCMOS) (V_O < 0 or V_O > V_{CC})
(see Note 2) . . . . . ±20 mA
Operating free-air temperature range, T_A (no suffix) . . . . . 0°C to 70°C
("I" suffix) . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This applies to external input and bidirectional buffers.
2. This applies to external output and bidirectional buffers.

MAXIMUM DISSIPATION RATING TABLE

PACKAGE	BOARD TYPE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PDT	Low-K	1733 mW	17.3 mW/°C	953.2 mW	695 mW
PDT	High-K	2710 mW	27.1 mW/°C	1490 mW	1084 mW

7.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Input voltage, V_I		0		V_{CC}	V
Output voltage, V_O		0		V_{CC}	V
Input transition time, (t_r, t_f) (10% to 90%)		0		25	ns
Operating free-air temperature, T_A	No suffix	0	25	70	°C
	"I" suffix	−40	25	85	
Virtual junction temperature, T_{JC}‡		0	25	115	°C

† This applies to external output buffers.

‡ The junction temperatures listed reflect simulation conditions. The absolute maximum junction temperature is 150°C for 10-year life goal. The customer is responsible for verifying the junction temperature.

7.3 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −8 mA	0.8 V_{CC}			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.22 V_{CC}	V
V_{IH}	High-level input voltage		0.7 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.3 V_{CC}	V
I_{IL}	Low-level input current	$V_I = V_{IL}$			−1	µA
I_{IH}	High-level input current	$V_I = V_{IH}$			1	µA
I_{OZ}	High-impedance-state output current	$V_O = V_{CC}$ or GND			±5	µA
I_{CC}	Static supply current	Recommended operating conditions with PLI_SCLK at 49.152 MHz		100		mA
		PLI_SCLK = low or high		5		

8 Hardware Errata

8.1 $\overline{\text{MCIF\_ACK}}$ Pin Functionality

Section:

3.1.4 When operating the ceLynx host interface in multistrobe mode, the $\overline{\text{MCIF\_ACK}}$ is not asserted at the correct time for read or write mode.

Workaround: Avoid using multistrobe mode if possible. This can be accomplished by using an AND-gate to generate active-low $\overline{\text{MCIF\_STRB}}$ from read-strobe and write-strobe (assuming active-low signalling). The read-strobe or the write-strobe (again depending on signalling) can then be connected directly to the MCIF_RW pin to indicate direction. If multistrobe mode is required without external logic, use an auto-acknowledge/self-acknowledge mode on the host processor that automatically terminates the read or write access after a period greater than 114 ns.

8.2 JTAG

Section:

2.5.1.5 JTAG works in bypass mode only. For details, refer to Notes in section 2.5.1.5.

8.3 Link Layer Controller(LLC)

Section:

6.3 Incorrect Cycle Lost Interrupt . When a series of conditions occur in an unlikely combination, the link layer may falsely declare a cycle lost condition and generate a false interrupt. If the external HW (external to the link), or SW utilizes this interrupt this may cause problem operation. If the node's HW or SW does not utilize this interrupt, there is no problem.

Workaround : Do not respond to a cycle lost interrupt until it happens twice in a row. If a cycle lost interrupt occurs, clear it, and check whether the cycle lost interrupt re−occurs. If another cycle lost interrupt does not occur, it was probably a false cycle lost condition. If another cycle lost interrupt does occur then the node should participate to the extent it can in the selection of a new cycle−master. These conditions are unlikely to occur; it is not thought this presents a significant problem for users.

If a legitimate, single event, cycle lost interrupt occurs, an MPEG isochronous packet to be transmitted may have become stale and should not be sent. If an MPEG packet has been held in the transmit FIFO during the lost cycle, it can be checked by link layer logic (the MPEG aging logic) to determine if the data is stale (too late) and should not be sent. No other type of IEC 61883 isochronous data requires “late” packets to not be sent.

6.3.1 Operating ceLynx in manual cycle master mode (LCTRL.CMAUTO = 0) results in two cycle masters on the bus in some topology configurations.

Workaround: Do not use manual cycle mater mode. Application should use cycle master auto mode by setting LCTRL.CMAUTO bit to 1 during initialization phase. The cycle master auto mode automatically sets LCTRL.CYCMASTER to 1 and enables the cycle master function when the node becomes root.

8.4 High Speed Data Interface(HSDI)

Section:

3.2.3.4 For HSDI sync mode B read operations, the HSDIx_SYNC signal may operate incorrectly if the HSDIx_EN signal is deasserted before the end of the current cell. When the error condition occurs, the HSDIx_SYNC signal may indicate another *new cell* before the end of the current cell.

Note: A *cell* indicates a source packet unit for the stream type being received through the HSDI. For example, one MPEG2−DVB cell = 188 bytes of MPEG source packet, one DV cell = 480 bytes of DV source packet.

Workaround: Program the application to read complete cells from the HSDI and to deassert the HSDIx_EN signal only on cell boundaries. If this is not possible due to system constraints, then the application must ignore the HSDIx_SYNC signal until it has received an entire cell.

6.4.1 For HSDI read operations, never reset the HSDI by setting HSDIx_CFG0.HSDIxRST bit. When HSDI reset is initiated, the HSDI port freezes and is no longer able to receive any data. For this reason, it is recommended for the application to use a separate HSDI port for each type of read or write operation. For example, designate HSDI0 for write operations and HSDI1 for read operations only. This problem is scheduled to be corrected in future ceLynx devices.

8.5 Data Buffer Interface

Section:

4.1.3 The buffer address range for buffer 0/buffer 1 should be set to more than 9 quadlets for correct operation of the buffer status flags.

6.6 When the 1394 packets are received with the packet token attached and the packet token hits the end of the RX buffer boundary, DBSTATx.BUFxEMPTY bit reports a wrong status information of ‘Buffer not empty’ even when it is empty. This problem is scheduled for fix in all future ceLynx devices.

Workaround: Use DBSTATx.BUFxCELLAV bit to check the buffer status.

4.2, 6.6 The time stamp age function does not work when DB(N)CFG0.CELL LENGTH is set to 0. When DB(N)CFG0.CELL LENGTH is set to 0, ceLynx does not abort the old packets with expired time stamps.

Workaround: The CELL LENGTH has to be set to greater than 0. Setting this bit to as small as 1 or 2 will work for all video stream types supported by ceLynx hardware.

8.6 DV Data TX/RX

Section:

4.2.3, 4.2.4 TSOFFSET logic and video stream hardware setting in **DV operations** only. Only one buffer should be programmed to use each video stream hardware: video select A or video select B (DB(N)CFG0.VIDEOSEL = 01 or 10). If more than one buffer is configured to use the same video stream hardware, the TSOFFSET logic uses the lowest numbered buffer, regardless of which buffer is enabled. The default CFR setting for DB(N)CFG0.VIDEOSEL needs to be reconfigured by the application accordingly. The video stream hardware should be set to NONE for buffers 0 and 1 (DB(N)CFG0.VIDEOSEL = 00) when other buffers are used for DV data transactions.

Example: Buffer 2 is configured for DV TX and buffer 3 for DV RX. DB(2)CFG2.TSOFFSET = 6000h and DB(3)CFG2.TSOFFSET = 3000h. Both buffers are programmed for video select A (DB(2)CFG0.VIDEOSEL = 01, DB(3)CFG0.VIDEOSEL = 01). In this case, the TSOFFSET value in buffer 2 (6000h) is reflected in the time stamp calculation even if buffer 3 is the only buffer enabled for DV RX operation.

5.5.3.4 DV release data mode (HSDIxCFG0.ReleaseData) does not work per the data manual description. If the use of release data mode is required by the application, a workaround can be provided.

5.5.3.6 Receiving DV headers only mode: DV headers only mode provides support for receiving DV H0 headers to the DV buffer. Current ceLynx does not support this mode as specified in the data manual. When this mode is enabled, quadlets other than DV H0 are received in the DV buffer.

Workaround: none.

8.7 Receive Data Path(RXDP)

Section:

4.1, 6.8 ceLynx does not correctly deselect the incoming streams that are not configured to be received in ceLynx RX data path/buffer 0.There are some automatic packet abort features in ceLynx HW that flushes thepacket when ceLynx HW detects an error condition. For example, settingRXDPCTL.ABTDBCERR bit to 1 enables the function that aborts an entire MPEGcell or DV frame when ceLynx hardware sees the discontinuity in incoming packetswhich causes the DBC error. However, this function may incorrectly behave in thecondition that there are multiple ISO streams broadcasted on the bus and ceLynxbuffer 0 is configured to receive. In this condition, ceLynx hardware aborts all incomingpackets including the ones that are programmed to receive into buffer 0 andflags RXDPINT.PKTRCVERR = 1.

Example: There are two ISO streams, DVB and DV being broadcasted in separate ISO channels, and buffer 0 is configured to receive DV streams. In this condition, nothing willbe received into buffer 0 and RXDPINT.PKTRCVERR0 keeps being set to 1 untilRXDPCTL.ABTDBCERR is set to 0. As soon as RXDPCTL.ABTDBCERR set to0, DV stream RX recovers correctly and no RXDPINT.PKTRCVERR0 flagged. Noproblem when buffers other than buffer 0 is configured to receive DV streams, orthere is another buffer configured to receive the second ISO stream(DVB streamin this example) so that there is no stream on the bus that ceLynx is not configuredto receive.

Workaround: Use buffers other than buffer 0 for 1394 RX operations. If the application has to use buffer 0 for 1394 RX operation, disable all automatic abort functions such asRXDPCTL.ABTDBCERR for correct RX operation. In this case, automatic abort functions are not supported by ceLynx hardware.

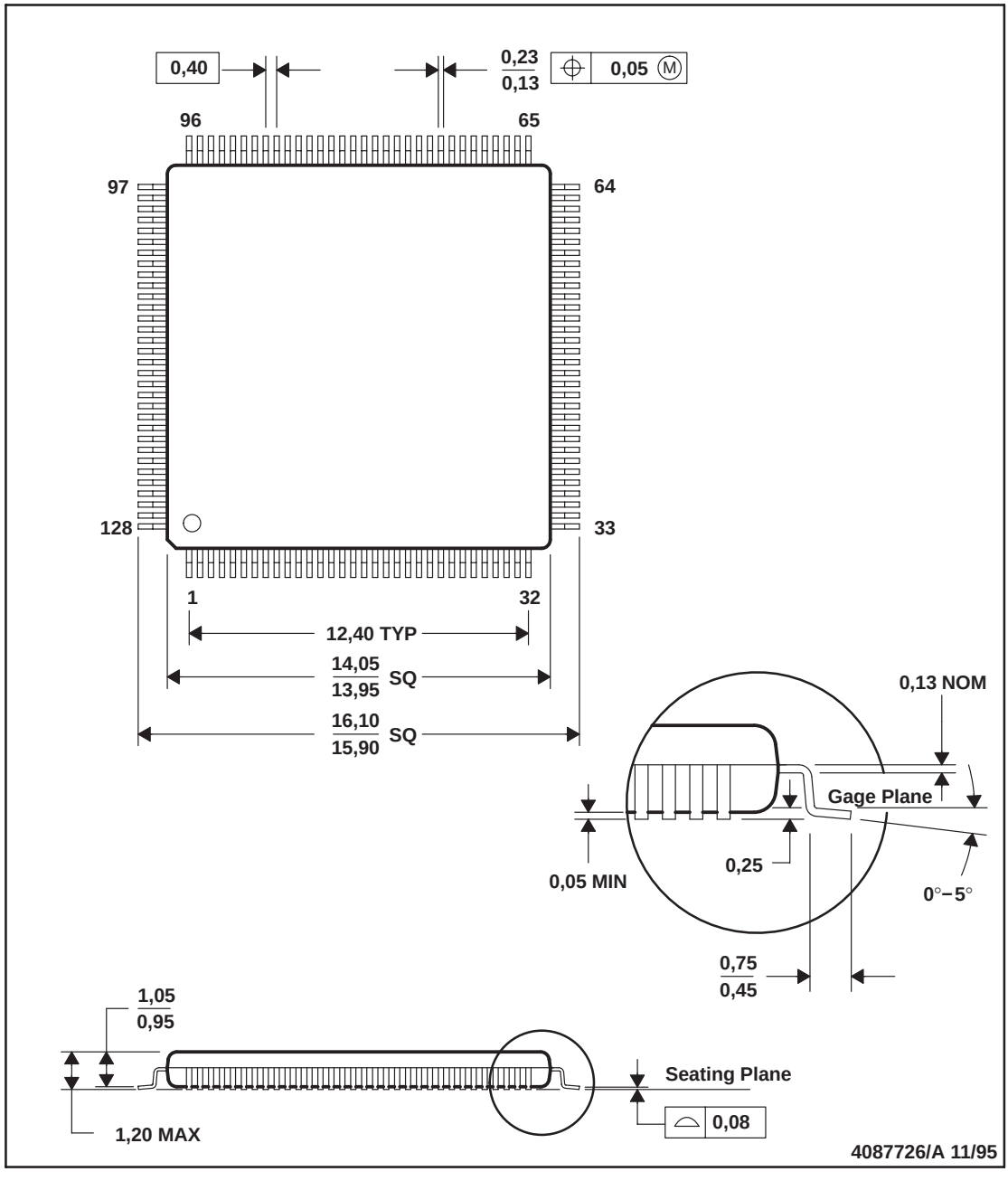
6.8 If the application wants to keep receiving ISO streams while it is forcing to acknowledge the incoming asynchronous packets with ACK_TARDY or ACK_BUSY_X, do not set RXDPCTL.ACKTARDYEN or RXDPCTL.BSYALLPKTS bit. Setting any of these bits will block ISO stream RX.

Workaround: The application can force the node to acknowledge the incoming Asynchronous packets with ACK_BUSY_X by setting RXDP(N)CFG1 = 0x00000000.

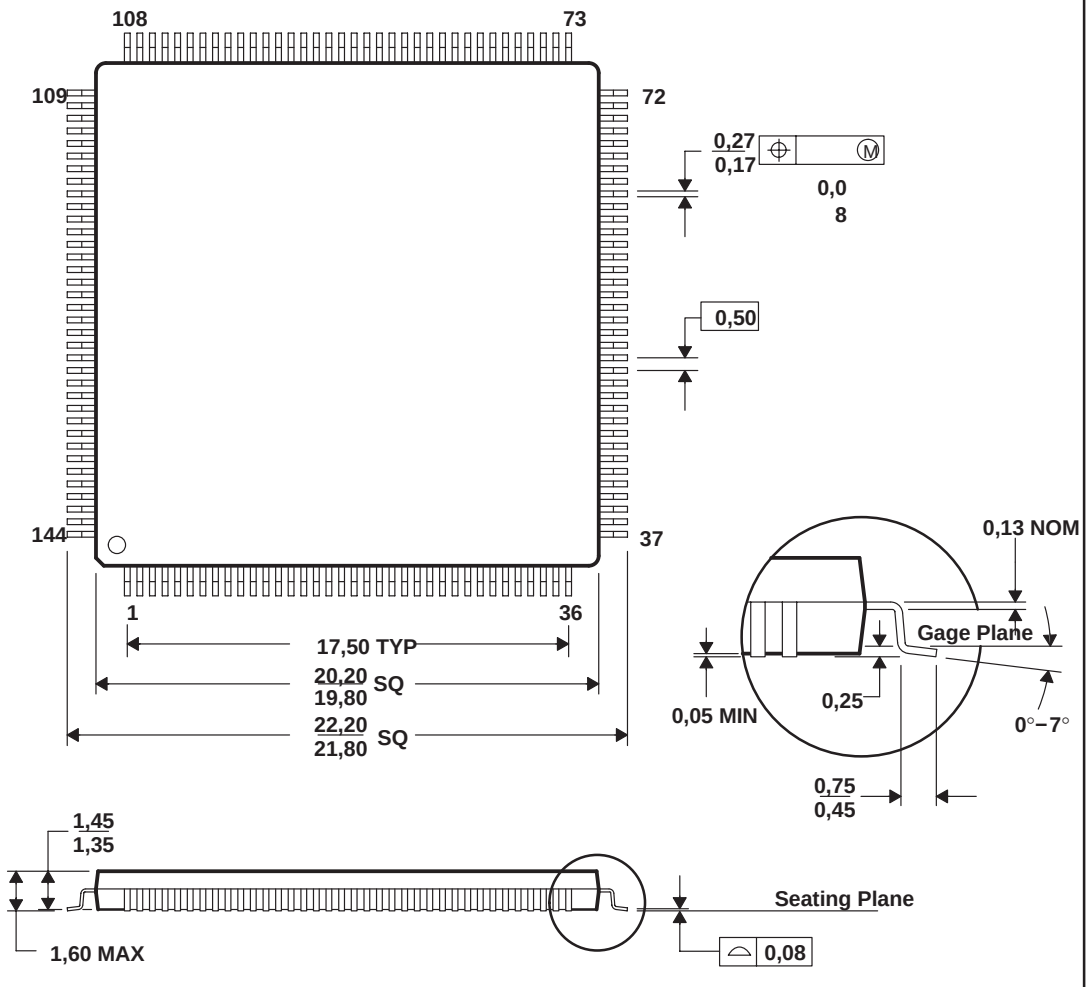
9 Mechanical Information

The TSB42AA4/TSB42AB4 is packaged in a high-performance 128-pin PDT package. The following shows the mechanical dimensions of the PDT package.

PDT (S-PQFP-G128) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026