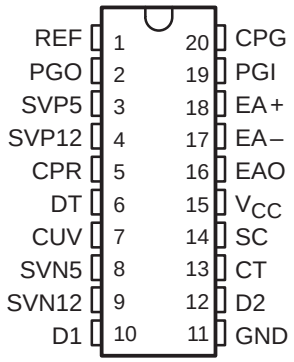
SLVS082A – APRIL 1994 – REVISED SEPTEMBER 1994

- **Single-Chip Switching-Power-Supply Control With Limited External Components**
- **Built-In PWM Control Circuit**
- **Open-Collector Output for Direct Drive of Transformer**
- **Variable Dead-Time Control**
- **Overvoltage and Undervoltage Detection and Latch-Up for Each Supply Voltage: 5 V, 12 V, –5 V, and –12 V**
- **System Overcurrent Protection**
- **Wide Supply Range From 7 V to 40 V**
- **Power-Good Indicator Function**

N PACKAGE
(TOP VIEW)



description

The TPS5206CN is a bipolar monolithic integrated circuit designed for push-pull-type switching-power-supply (SPS) control in desktop PC applications. It offers pulse-width-modulation (PWM) control and power-supply supervisor functions, including detection of undervoltage and overvoltage conditions on ±5 V and ±12 V system supplies. It also detects overcurrent conditions on the SPS system output. This single chip reduces the total component count and provides additional design flexibility, which minimizes cost and printed-circuit-board (PCB) space requirements in present and new SPS designs.

overvoltage-protection lockout feature

The overvoltage-protection lockout feature monitors four different supply voltages. When an overvoltage (OV) condition is detected, the power-good output (PGO) is set low and the PWM function is disabled. The OV condition is detected on the SVP5, SVP12, SVN5, and SVN12 inputs. Threshold voltages are typically 5.9 V, 14.1 V, –8.4 V, and –15.3 V, respectively.

undervoltage-protection lockout feature

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overcurrent-protection lockout feature

The overcurrent (OC) protection lockout feature is designed to protect the SPS from excessive load or short-circuit conditions. The circuit converts the output current of the SPS to a voltage, which is then monitored at SC. It sets PG low and shuts down the PWM circuit when the sensed voltage is higher than 5 V.

reference regulator

The internal 5-V reference regulator is designed primarily to provide the internal circuitry with a stable supply rail for varying input voltages. The regulator employs a band-gap circuit as its primary reference to maintain thermal stability of less than 100-mV variation over the operating free-air temperature range of 0°C to 70°C. In addition to supplying an internal reference, the regulator provides a precision 5-V reference that can support 5 mA of load current for external bias circuits. The regulated voltage has a margin of error of 2%. Short-circuit protection is provided to protect the internal circuit from overload or short-circuit conditions.

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oscillator

The timing capacitor (CT) is charged by the oscillator with a 350-μA current source set by the timing resistor (RT) (10 kΩ), internally. This produces a linear-ramp voltage waveform across CT. When the voltage across CT reaches 3 V, it is discharged by the oscillator circuit and the charging cycle is reinitiated. The frequency of the oscillator is programmable over a range of 1 kHz to 300 kHz by the selection of CT. The programmed frequency of the oscillator can be calculated with the equation $f = 1/(10^4 \times CT)$. The PWM output frequency is one-half of the oscillator frequency.

dead-time (DT) control

The DT input provides control of minimum dead time (off time). An input offset of 110 mV ensures a minimum dead time of 3% with the DT input grounded. Additional dead time can be imposed by applying voltage to the DT input. This provides a linear control of the dead time from its minimum of 3% to its maximum of 100% as the DT input voltage varies from 0 V to 3.3 V. The DT input is a relatively high-impedance input and is used where additional control of the output duty cycle is required. The input must be terminated; leaving this terminal open causes an undefined condition.

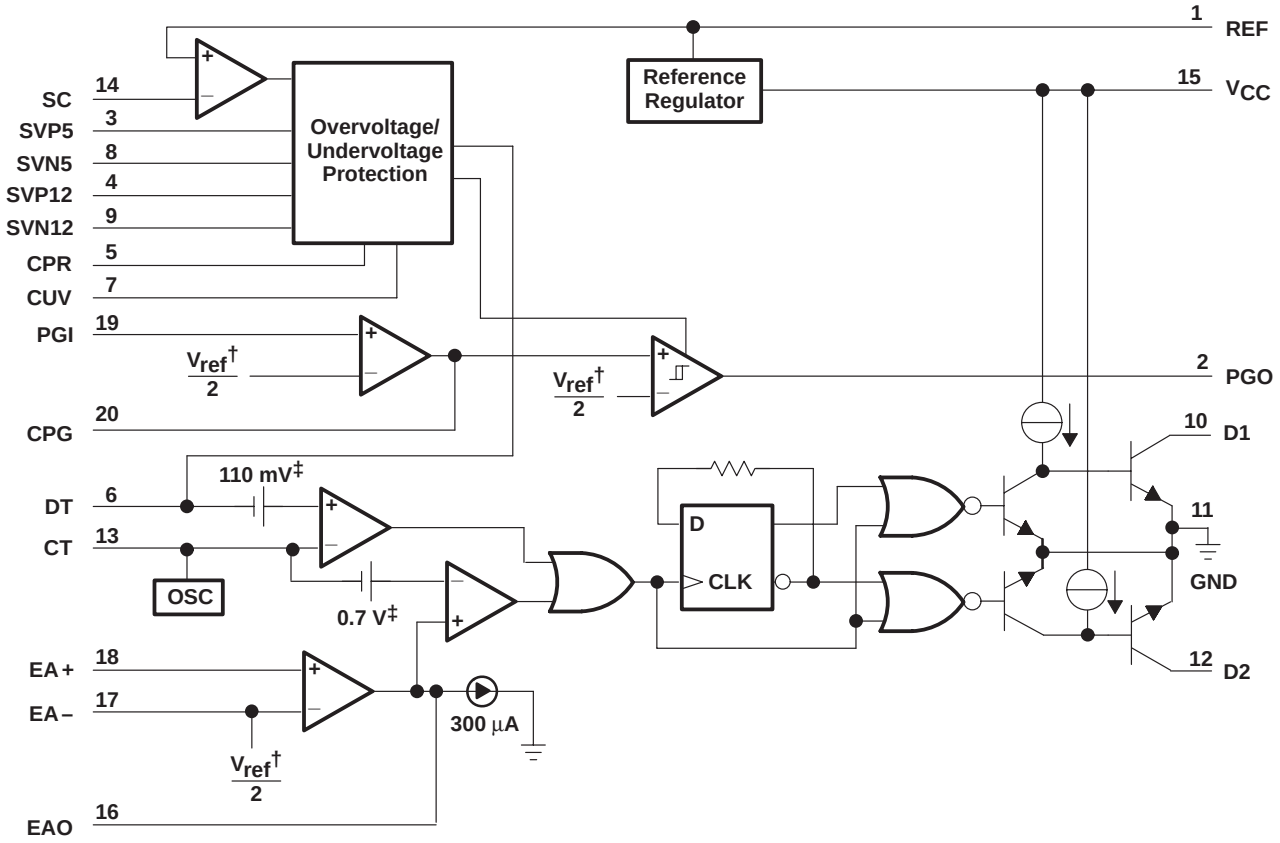
pulse-width modulation

The ramp voltage across CT is compared to the output of the error amplifier. The CT input incorporates a series diode, which is omitted from the DT control input. This requires the error-amplifier output to be 0.7-V greater than the voltage across CT to inhibit the PWM output. This also ensures PWM maximum-duty-cycle operation without requiring the control voltage to sink to true ground potential. The output pulse width varies from 97% of the period to 0 as the voltage at the error-amplifier output varies from 0.5 V to 3.5 V.

error amplifier

The high-gain error amplifier receives bias from the V_{CC} power rail. The inverting input, EA–, is biased by $V_{ref}/2$ internally. The amplifier output is biased low by a current sink to provide PWM maximum duty cycle when the amplifier is off. Since the amplifier output is biased low only through $I_{O(sink)}$ of 300 μA (see functional block diagram), bias current required by external circuitry into the amplifier output for feedback must not exceed the capability of $I_{O(sink)}$; otherwise, the PWM maximum duty cycle is limited.

functional block diagram



† Internally generated voltage
‡ Fixed-voltage offset

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CPG	20	O	Power-good-capacitor connection. Connects a capacitor to power-good signal delay.
CPR	5	O	Protection-delay-capacitor connection. Connects a capacitor to protection-delay circuit to bypass high-frequency noise.
CT	13	O	Timing capacitor. Connects a capacitor to sawtooth oscillator circuit for programming the operating frequency.
CUV	7	O	UV capacitor connection. Connects a capacitor to UV power-on delay circuit to avoid malfunction in the initial state.
D1	10	O	PWM driver-1 output
D2	12	O	PWM driver-2 output
DT	6	I	Dead time. Control input to control the PWM minimum dead time (off time).
EA–	17	I	Error-amplifier inverting input
EA+	18	I	Error-amplifier noninverting input
EAO	16	I/O	Error-amplifier output
GND	11		Ground
PGI	19	I	Power-good input
PGO	2	O	Power-good output
REF	1	O	5-V reference voltage output
SC	14	I	Overcurrent sense input. When an OV/UV condition is sensed, the TLS1206 output is locked and PGO is set to low.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
SVN5	8	I	–5-V OV/UV detection input. When an OV/UV condition is sensed, the TLS1206 output is locked and PGO is set to low.
SVN12	9	I	–12-V OV/UV detection input. When an OV/UV condition is sensed, the TLS1206 output is locked and PGO is set to low.
SVP5	3	I	5-V OV/UV detection input. When an OV/UV condition is sensed, the TLS1206 output is locked and PGO is set to low.
SVP12	4	I	12-V OV/UV detection input. When an OV/UV condition is sensed, the TLS1206 output is locked and PGO is set to low.
V_{CC}	15		Supply voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 41 V
Amplifier input voltage, V_I . . . . . V_{CC} + 0.3 V
Collector output voltage, V_O . . . . . 41 V
Collector output current, I_O . . . . . 250 mA
Total power dissipation at (or below) 25°C free-air temperature . . . . . 1 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 70°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	7	40	V
Collector output voltage, $V_{O(D1)}$, $V_{O(D2)}$		40	V
Collector output current, $I_{O(D1)}$, $I_{O(D2)}$		150	mA
Timing capacitor, CT	0.47	10000	nF
Operating free-air temperature, T_A	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ref}	Reference output voltage		I_O = 5 mA		4.9	5	5.1	V
$V_{IH(SC)}$	High-level input voltage, SC overcurrent protection		SVP5 = 5 V, SVN5 = –5 V, $V_{O(DT)} \geq$ 3.5 V	SVP12 = 12 V, SVN12 = –12 V,	5.1			V
$V_{IL(SC)}$	Low-level input voltage, SC overcurrent protection		SVP5 = 5 V, SVN5 = –5 V, $V_{O(DT)} \leq$ 0.4 V	SVP12 = 12 V, SVN12 = –12 V,			4.9	V
$V_{IT(UV)}$	Input threshold voltage, undervoltage sense	SVP5	SVP12 = 12 V, SVN12 = –12 V,	SVN5 = –5 V, $V_{O(DT)} \leq$ 0.4 V	3.5	3.9	4.5	V
		SVP12	SVP5 = 5 V, SVN12 = –12 V,	SVN5 = –5 V, $V_{O(DT)} \leq$ 0.4 V	9	9.5	10.5	
		SVN5	SVP5 = 5 V, SVN12 = –12 V,	SVP12 = 12 V, $V_{O(DT)} \leq$ 0.4 V	–3	–3.4	–4	
		SVN12	SVP5 = 5 V, SVN5 = –5 V,	SVP12 = 12 V, $V_{O(DT)} \leq$ 0.4 V	–8	–9.3	–10	
$V_{IT(OV)}$	Input threshold voltage, overvoltage sense	SVP5	SVP12 = 12 V, SVN12 = –12 V,	SVN5 = –5 V, $V_{O(DT)} \leq$ 0.4 V	5.5	5.9	6.3	V
		SVP12	SVP5 = 5 V, SVN12 = –12 V,	SVN5 = –5 V, $V_{O(DT)} \leq$ 0.4 V	13.5	14.1	14.8	
		SVN5	SVP5 = 5 V, SVN12 = –12 V,	SVP12 = 12 V, $V_{O(DT)} \leq$ 0.4 V	–7	–8.4	–9	
		SVN12	SVP5 = 5 V, SVN5 = –5 V,	SVP12 = 12 V, $V_{O(DT)} \leq$ 0.4 V	–14	–15.3	–16	
$V_{OL(D1)}$, $V_{OL(D2)}$	Low-level output voltage, output drivers		$V_{O(DT)} \geq$ 3.5 V	I_{OL} = 0			0.4	V
				I_{OL} = 150 mA		1.6	2.5	
$V_{O(DT)}$	Dead-time output voltage		SVP5 = 7 V,	$I_{O(DT)}$ = –250 µA	3.5			V
$V_{IH(PGI)}$	High-level input voltage, PGI		$V_{O(PGO)} \geq$ 4 V,	See Figure 3	2.8			V
$V_{IL(PGI)}$	Low-level input voltage, PGI		$V_{O(PGO)} \leq$ 0.4 V,	See Figure 3			2.42	V
$V_{IH(CPG)}$	High-level input voltage, CPG		$V_{I(PGI)}$ = 4 V, See Figure 4	$V_{O(PGO)} \geq$ 4 V,	2.95			V
$V_{IL(CPG)}$	Low-level input voltage, CPG		$V_{I(PGI)}$ = 4 V, See Figure 4	$V_{O(PGO)} \leq$ 0.4 V,			2.6	V
$V_{OH(PGO)}$	High-level output voltage, PGO		V_{CPG} = 4 V, See Figure 5	$I_{O(PGO)}$ = –240 µA,	4.75			V
$V_{OL(PGO)}$	Low-level output voltage, PGO		V_{CPG} = 0 V, See Figure 6	$I_{O(PGO)}$ = 9.6 mA,			0.4	V
I_{CC}	Standby supply current		All other inputs and outputs open				32	mA
f_{osc}	Oscillator frequency		C_T = 1200 pF			80		kHz

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Rise time of power good	V_{CPG} L → H, $V_{O(PGO)}$ L → H,	See Figures 4 and 6			100	ns
t_d	Delay time of power good	R_L = 150 kΩ, CPG = 2.2 µF, $V_{I(PGI)}$ H → L, $V_{O(PGO)}$ H → L,	See Figures 4 and 6		500	600	µs

APPLICATION INFORMATION

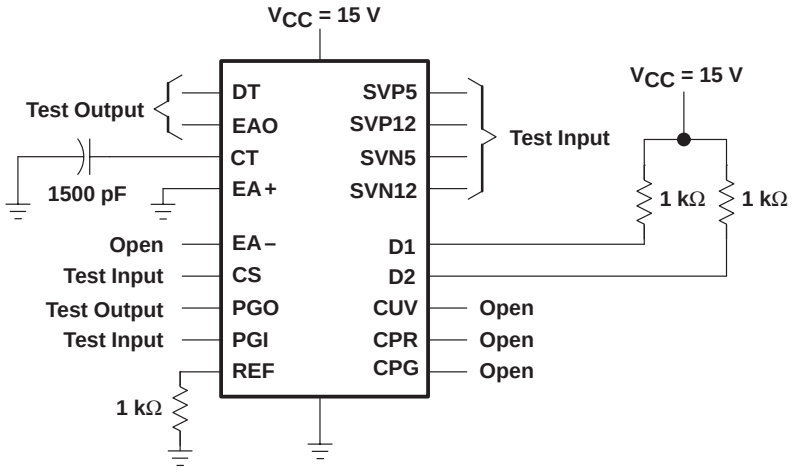


Figure 1. Test Circuit

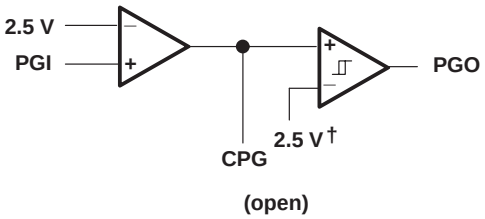


Figure 2. PGI Input Voltage Test Circuit

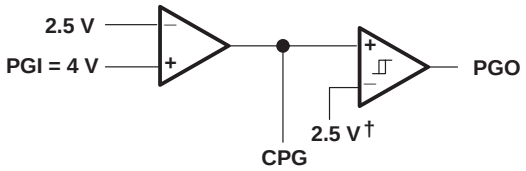


Figure 3. CPG Input Voltage and PGO Output Voltage Test Circuit

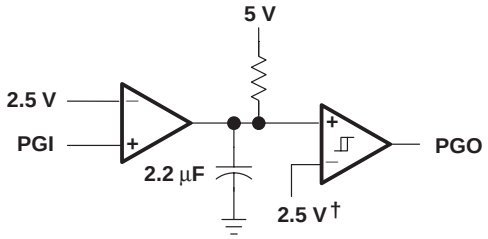


Figure 4. PG Delay Time and Rise Time Test Circuit

† Internally biased at $V_{ref}/2$ or 2.5 V

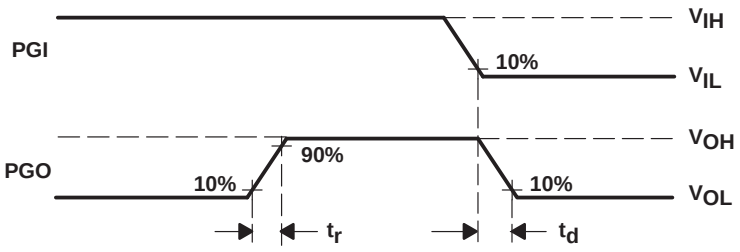


Figure 5. PG Output Voltage Waveform

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