TLC320AD57C
Data Manual

Sigma-Delta Stereo Analog-to-Digital Converter

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1 Introduction

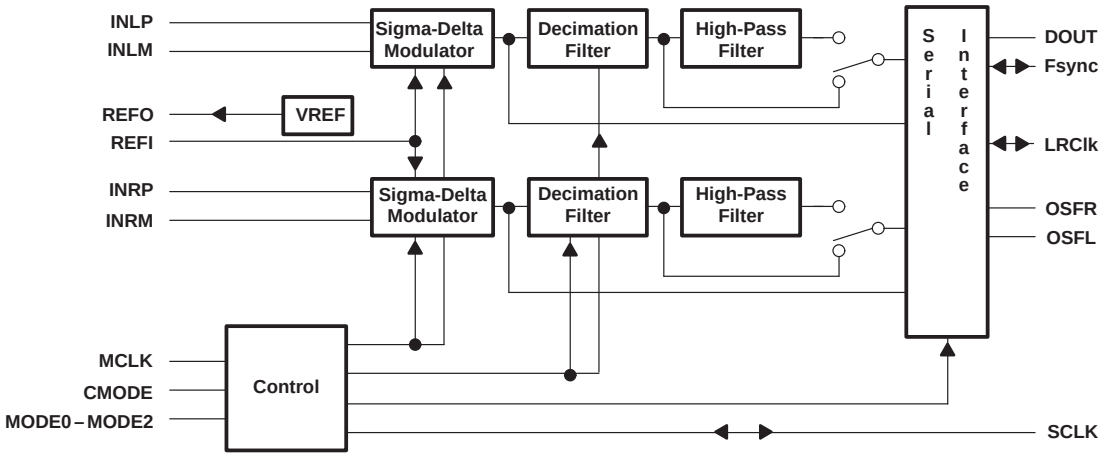
The TLC320AD57C provides high-resolution signal conversion from analog to digital using oversampling sigma-delta technology. This device consists of two synchronous conversion paths. Also included is a decimation filter after the modulator as shown in the functional block diagram. Other functions provide analog filtering and on-chip timing and control.

A functional block diagram of the TLC320AD57C is included in section 1.2. Each block is described in the Detailed Description section.

1.1 Features

- Single 5-V Power Supply
- Sample Rates (f_S) up to 48 kHz
- 18-Bit Resolution
- Signal-to-Noise (EIAJ) of 97 dB
- Dynamic Range of 95 dB
- Total Signal-to-Noise+Distortion of 91 dB
- Internal Reference Voltage (V_{ref})
- Serial Port Interface
- Differential Architecture
- Power Dissipation of 200 mW. Power-Down Mode for Low-Power Applications
- One Micron Advanced LinEPIC1Z™ Process

1.2 Functional Block Diagram



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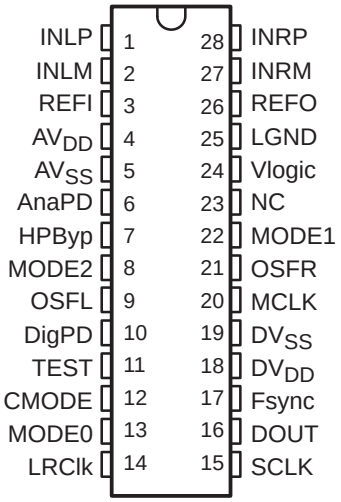
1.3 Terminal Assignments

DW PACKAGE
(TOP VIEW)



NC – No internal connection

1.4 Ordering Information

T_A	PACKAGE
	SMALL OUTLINE (DW)
0°C to 70°C	TLC320AD57CDW

1.5 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AnaPD	6	I	Analog power-down mode. The analog power-down mode disables the analog modulators. The single-bit modulator outputs become invalid, which renders the outputs of the digital filters invalid. When AnaPD is pulled low, normal operation of the device resumes.
AV_{DD}	4	I	Analog supply voltage
AV_{SS}	5	I	Analog ground
CMODE	12	I	Clock mode. CMODE selects between two methods of determining the master clock frequency. When CMODE is high, the master clock input is 384× the conversion frequency. When CMODE is low, the master clock input is 256× the conversion frequency.
DOUT	16	O	Data output. DOUT transmits the sigma-delta audio analog-to-digital converter (ADC) output data to a digital signal processor (DSP) serial port or other compatible serial interface and is synchronized to SCLK. DOUT is low when DigPD is high.
DV_{DD}	18	I	Digital supply voltage

1.5 Terminal Functions (Continued)

<table>
<tr><th colspan="2">TERMINAL
NAME</th><th>NO.</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><td colspan="2">DV$_{SS}$</td><td>19</td><td>I</td><td>Digital ground</td></tr>
<tr><td colspan="2">DigPD</td><td>10</td><td>I</td><td>Digital power-down mode. The digital power-down mode shuts down the digital filters and clock generators. All digital outputs are brought to unasserted levels. When DigPD is pulled low, normal operation of the device resumes.</td></tr>
<tr><td colspan="2">Fsync</td><td>17</td><td>I/O</td><td>Frame synchronization. Fsync designates valid data from the ADC.</td></tr>
<tr><td colspan="2">HPByp</td><td>7</td><td>I</td><td>High-pass filter bypass. When HPByp is high, the high-pass filter is bypassed. This allows dc analog signal conversion.</td></tr>
<tr><td colspan="2">INLM</td><td>2</td><td>I</td><td>Inverting input to left analog input amplifier</td></tr>
<tr><td colspan="2">INLP</td><td>1</td><td>I</td><td>Noninverting input to left analog input amplifier</td></tr>
<tr><td colspan="2">INRM</td><td>27</td><td>I</td><td>Inverting input to right analog input amplifier</td></tr>
<tr><td colspan="2">INRP</td><td>28</td><td>I</td><td>Noninverting input to right analog input amplifier</td></tr>
<tr><td colspan="2">LGND</td><td>25</td><td>I</td><td>Logic-power-supply ground for analog modulator</td></tr>
<tr><td colspan="2">LRClk</td><td>14</td><td>I/O</td><td>Left/right clock. LRClk signifies whether the serial data is associated with the left channel ADC (when high) or the right channel ADC (when low). LRClk is low when DigPD is high.</td></tr>
<tr><td colspan="2">MCLK</td><td>20</td><td>I</td><td>Master clock. MCLK derives all of the key logic signals of the sigma-delta audio ADC. The nominal input frequency range is 18.432 MHz to 256 kHz.</td></tr>
<tr><td colspan="2">MODE0–MODE2</td><td>8, 13, 22</td><td>I</td><td>Serial modes. MODE0–MODE2 configure this device for many different modes of operation. The different configurations are:
Master versus slave
16 bit versus 18 bit
MSB first versus LSB first
Slave: Fsync controlled versus Fsync high
Each of these modes is described in the Serial Interface section with timing diagrams.
<table>
<tr><th>MODE
0 1 2</th><th>MASTER/
SLAVE</th><th>BITS</th><th>MSB/LSB
FIRST</th></tr>
<tr><td>0 0 0</td><td>slave</td><td>up to 18</td><td>MSB</td></tr>
<tr><td>0 0 1</td><td>slave</td><td>18</td><td>LSB</td></tr>
<tr><td>0 1 0</td><td>slave</td><td>up to 18</td><td>MSB</td></tr>
<tr><td>0 1 1</td><td>master</td><td>16</td><td>MSB</td></tr>
<tr><td>1 0 0</td><td>master</td><td>18</td><td>MSB</td></tr>
<tr><td>1 0 1</td><td>master</td><td>18</td><td>LSB</td></tr>
<tr><td>1 1 0</td><td>master</td><td>16</td><td>MSB</td></tr>
<tr><td>1 1 1</td><td>master</td><td>16</td><td>LSB</td></tr>
</table></td></tr>
<tr><td colspan="2">OSFL, OSFR</td><td>9, 21</td><td>O</td><td>Over scale flag left/right. If the left/right channel analog input exceeds the full scale input range for two consecutive conversions, OSFL and OSFR are set high for 4096 LRClk periods. OSFL and OSFR are low when DigPD is high.</td></tr>
<tr><td colspan="2">SCLK</td><td>15</td><td>I/O</td><td>Shift clock. If SCLK is confirgured as an input, SCLK clocks serial data out of the sigma-delta audio ADC. If SCLK is configured as an output, SCLK stops clocking when DigPD is high.</td></tr>
<tr><td colspan="2">TEST</td><td>11</td><td>I</td><td>Test mode. TEST should be low for normal operation.</td></tr>
<tr><td colspan="2">REFI</td><td>3</td><td>I</td><td>Input voltage for modulator reference (normally connected to REFO, terminal 26).</td></tr>
<tr><td colspan="2">REFO</td><td>26</td><td>I</td><td>Internal voltage reference</td></tr>
<tr><td colspan="2">Vlogic</td><td>24</td><td>I</td><td>Logic power supply (5 V) for analog modulator</td></tr>
</table>

2 Detailed Description

The following sections contain a detailed description of the TLC320AD57C.

2.1 Power-Down and Reset Functions

The following sections contain descriptions of the power-down and reset functions of the TLC320AD57C.

2.1.1 Power Down

The power-down state is comprised of a separate digital and analog power down. The power consumption of each is detailed in Section 3.3, Electrical Characteristics.

The digital power-down mode shuts down the digital filters and clock generators. All digital outputs are set to an unasserted level. When the digital power-down terminal (DigPD) is pulled low, normal operation of the device is initiated.

In slave mode, the conversion process must synchronize to an input on the LRClk terminal and the SCLK terminal. Therefore, the conversion process is not initiated until the first rising edges on both SCLK and LRClk are detected after DigPD is pulled low. This synchronizes the conversion cycle. All conversions are performed at a fixed LRClk rate [MCLK/256 (CMODE low) or MCLK/384 (CMODE high)] after the initial synchronization. After the digital power-down terminal is brought low, the output of the digital filters remains invalid for 50 LRClk cycles [see Figures 2–1(a) and 2–1(b)].

In master mode, LRClk is an output; therefore, the conversion process initiates based on internal timing. The first valid data out occurs as shown in Figure 2–1(c).

The analog power-down mode disables the analog modulators. The single-bit modulator outputs become invalid, which renders the outputs of the digital filters invalid. When the analog power-down terminal is brought low, the modulators are brought back online; however, the outputs of the digital filters require 50 LRClk cycles for valid results.

2.1.2 Reset Function

The conversion process is not initiated until the first rising edges on both SCLK and LRClk are detected after DigPD is pulled low. This synchronizes the conversion cycle. All conversions are performed at a fixed LRClk rate [MCLK/256 (CMODE low) or MCLK/384 (CMODE high)] after the initial synchronization.

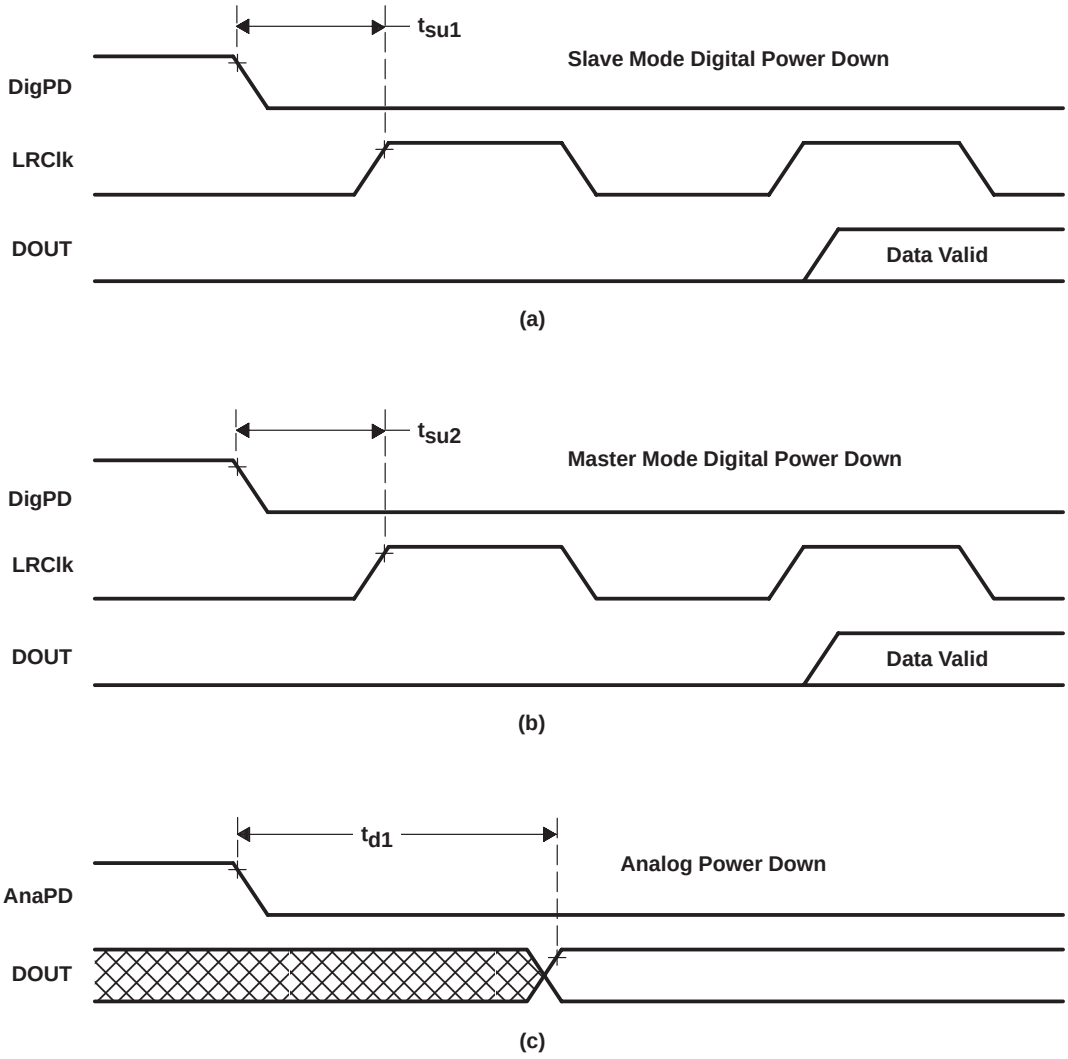


Figure 2–1. Power-Down Timing Relationships

2.2 Differential Input

The input is differential in order to provide common-mode noise rejection and increase the input dynamic range. Figure 2–2 shows the analog input signals used in a differential configuration to achieve 6.4-V peak-to-peak differential swing with a 3.2-V peak-to-peak swing per input line.

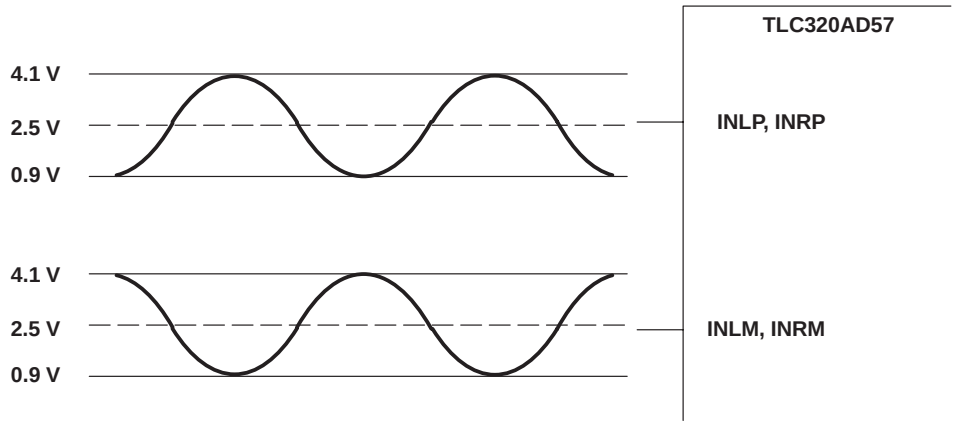


Figure 2–2. Differential Analog Input Configuration

2.3 Sigma-Delta Modulator

The modulator is a fourth order sigma-delta modulator with 64 times oversampling. The ADC provides high-resolution, low-noise performance from a one-bit converter using oversampling techniques.

2.4 Decimation Filter

The decimation filter used after the sigma-delta modulator reduces the digital data rate to the sampling rate of LRClk. This is accomplished by decimating with a ratio of 1:64. The output of this filter is a 2s complement data word of up to 18 bits serially clocked out.

If the input value exceeds the full range of the converter, the output of the decimator is held at the appropriate extreme until the input returns to within the dynamic range of the device.

2.5 High-Pass Filter

The high-pass filter removes dc from the input. With this filtering, offset calibration is not needed. The high-pass filter can be circumvented by asserting the HPByp terminal to pass dc signals through the converter. However, an offset due to the converter can be present when bypassing the high-pass filter.

2.6 Master-Clock Circuit

The master-clock circuit generates and distributes necessary clocks throughout the device. MCLK is the external master-clock input. CMODE selects the relationship of MCLK to the sample rate, LRClk. When CMODE is low, the sample rate of the data paths is set to LRClk = MCLK/256. When CMODE is high, the sample rate is set to LRClk = MCLK/384. With a fixed oversampling ratio of 64×, the effect of changing MCLK is shown in Table 2–1.

When the device is in master mode, SCLK is derived from MCLK in order to provide clocking of the serial communications between the sigma-delta audio ADC and a digital signal processor (DSP) or control logic. This is equivalent to a clock running at 64 × LRClk.

When the device is in slave mode, SCLK is externally derived.

Table 2–1. Master-Clock to Sample-Rate Comparison (modes 1, 3, 4, 5)

MCLK (MHz)	CMODE	SCLK (MHz)	LRClk (kHz)
12.2880	Low	3.0720	48
18.4320	High		
11.2896	Low	2.8224	44.1
16.9344	High		
8.1920	Low	2.0480	32
12.2880	High		
0.2560	Low	0.0640	1
0.3840	High		

2.7 Test

When the TEST input is high, the test mode is selected, which routes the high speed one-bit modulator result to the serial port output. When in the test mode, the SCLK output frequency is equal to the data output rate. LRClk is an input when the test mode is selected. This allows for the selection of the left or right modulator output to be routed to the serial port (high = left and low = right).

2.8 Serial Interface

Although the serial data is shifted out in two seperate time packets that represent the left and right channels, the inputs are sampled and converted simultaneously.

The serial interface protocol has master and slave modes each with different read-out modes. The master mode sources the control signals for conversion synchronization while the slave mode allows an external controller to provide conversion synchronization signals.

The five master modes are shown in Figures 2–3(a) through 2–3(e) and the three slave modes are shown in Figures 2–4(a) through 2–4(c). For a 16-bit word, D15 is the most significant bit and D0 is the least significant bit. Unless otherwise specified, all values are in 2s complement format.

In the master mode, SCLK is generated internally and is sourced as an output. The relationship of SCLK to LRClk is 64× (modes 1, 3, 4, 5) or 32× (modes 6, 7). In the slave mode, SCLK is an input. SCLK timing must meet the timing specifications listed in the Recommended Operating Conditions section.

2.8.1 Master Mode

As the master, the TLC320AD57C generates LRClk, Fsync, and SCLK from MCLK. These signals are provided for synchronizing the serial port of a DSP or other control devices.

Fsync designates valid data from the ADC, and accomplishes this in the master modes by one of two methods. The first method is to place a single pulse on Fsync prior to valid data. This indicates the starting point for the data. The second method of frame synchronization is to hold Fsync high during the entire valid data cycle which provides boundaries for the data.

LRClk is generated internally from MCLK. The frequency of this signal is fixed at the sampling frequency f_S [MCLK/256 (CMODE low) or MCLK/384 (CMODE high)]. During the high period of this signal, the left channel data is serially shifted to the output; during the low period, the right channel data is shifted to the output. The conversion cycle synchronizes with the rising edge of LRClk.

Five modes are available when the device is configured as a master. Two modes are for 18-bit communications. These modes differ from each other in that the MSB is transferred first in one mode while the LSB is transferred first in the second mode [see Figures 2–3(b) and 2–3(c)]. When the LSB is transferred first, the data is right justified to the LRClk [see Figures 2–3(a) through 2–3(e)]. The three other modes

available as a master are 16-bit modes. Two of the modes differ as MSB first versus LSB first. These two modes set SCLK = LRClk × 32. This is one half the frequency used in the other transfer modes [see Figures 2–3(d) and 2–3(e)]. The third 16-bit mode provides the data MSB first with one clock delay after LRClk [see Figure 2–3(a)].

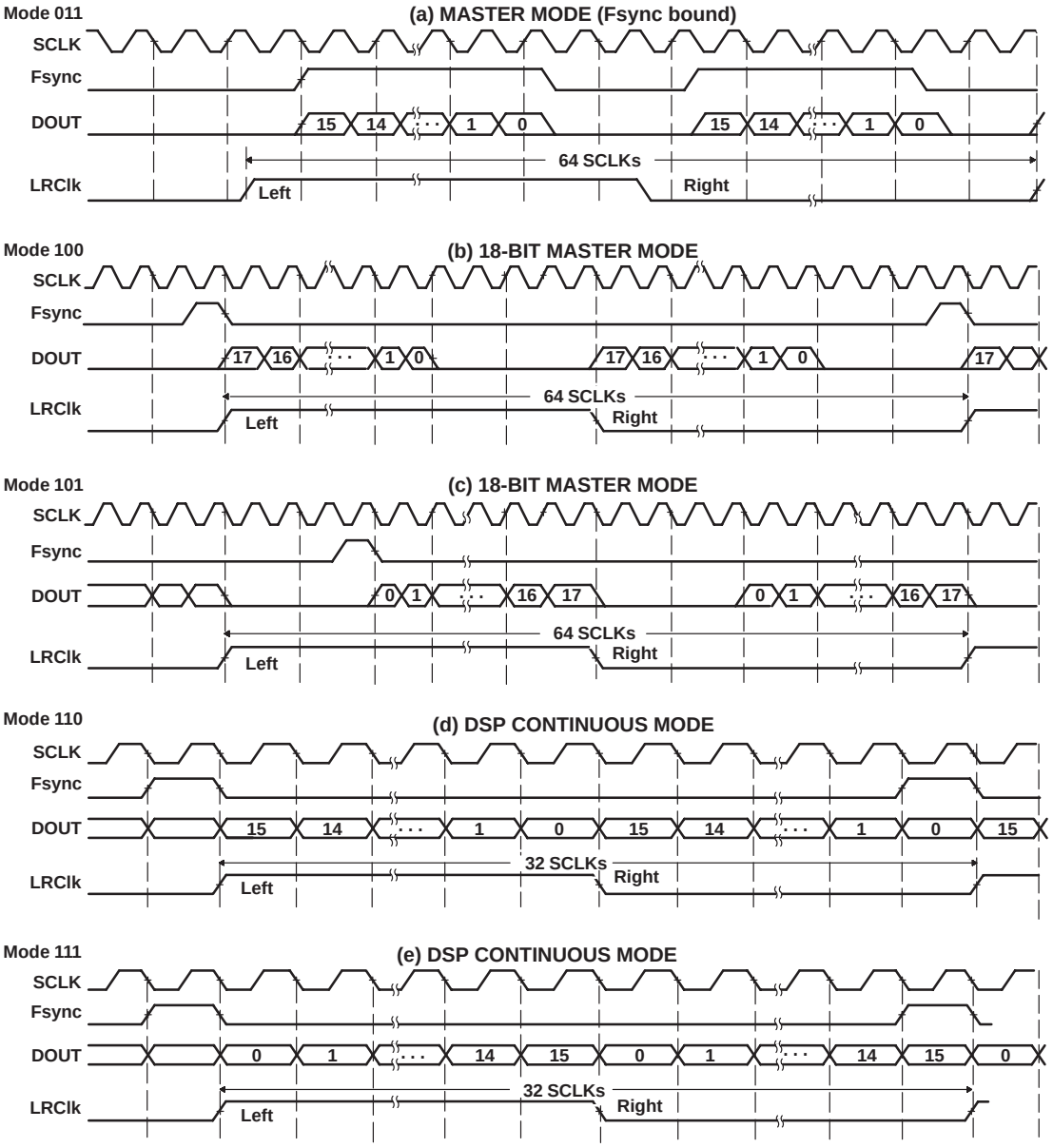


Figure 2–3. Serial Master Transfer Modes

2.8.2 Slave Mode

As a slave, the TLC320AD57C receives LRClk, Fsync, and SCLK as inputs. The conversion cycle synchronizes to the rising edge of LRClk, and the data synchronizes to the falling edge of SCLK. SCLK must meet the setup time requirements specified in Section 3.2, Recommended Operating Conditions. Synchronization of the slave modes is accomplished with the digital power-down control.

In slave mode, Fsync is an input. Three modes are provided as shown in Figures 2–4(a) through 2–4(c).

SCLK and LRClk are externally generated and sourced. The first rising edges of SCLK and LRClk after a power-down cycle initiate the conversion cycle. Refer to Section 2.8.1, Master Mode for signal functions.

Several modes are available when the TLC320AD57C is configured as a slave. Using the Mode0, Mode1, and Mode2 terminals, the TLC320AD57C can be set to shift out the MSB first or the LSB first [see Figures 2–4(a) and 2–4(b)]. The number of bits shifted out can be controlled by the number of valid SCLK cycles provided within the left or right channel period. If only enough clocks are provided to shift out 16 data bits before LRClk changes state, this is equivalent to a 16-bit mode.

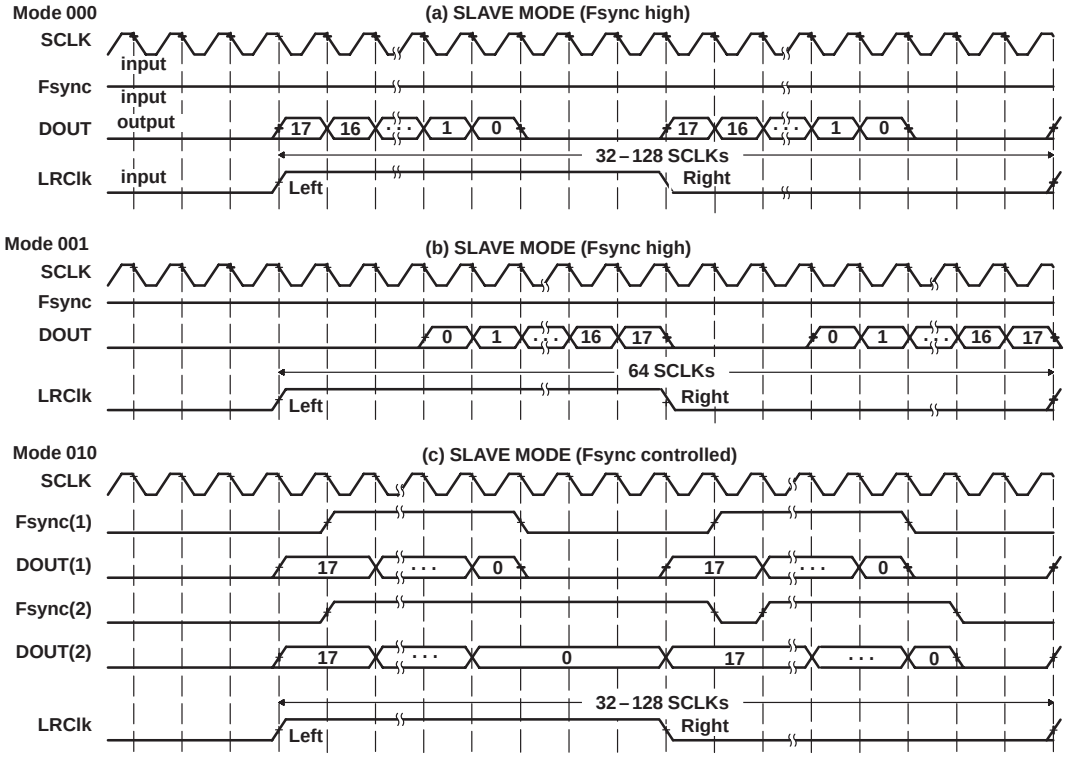


Figure 2–4. Serial Slave Transfer Modes

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Analog supply voltage range, AV_{DD} (see Note 1) . . . . . −0.3 V to 6.5 V
Digital supply voltage range, DV_{DD} (see Note 2) . . . . . −0.3 V to 6.5 V
Digital output voltage range, (externally applied) . . . . . −0.3 V to DV_{DD} + 0.3 V
Digital input voltage range, MODE0 – MODE2 . . . . . −0.3 V to DV_{DD} + 0.3 V
Analog input voltage range, INLP, INLM, INRP, INRM . . . . . −0.3 V to AV_{DD} + 0.3 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Case temperature for 10 seconds, T_C . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values for maximum ratings are with respect to AV_{SS}.
2. Voltage values for maximum ratings are with respect to DV_{SS}.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Analog supply voltage, AV_{DD} (see Note 3)	4.75	5	5.25	V
Digital supply voltage, DV_{DD}	4.75	5	5.25	V
Analog logic supply voltage, at Vlogic	4.75	5	5.25	V
Reference voltage, V_{ref}		3.2		V
Setup time, DigPD↓ to LRClk↑, slave mode, t_{su1} (see Figure 2–1(a))		30		ns
Setup time, DigPD↓ to LRClk↑, master mode, t_{su2} (see Figure 2–1(b))		30		ns
Setup time, SCLK↑ to LRClk, slave mode, t_{su3} (see Figures 4–5 and 4–6)	30			ns
Setup time, LRClk to SCLK↑, slave mode, t_{su4} (see Figure 4–5)	30			ns
Setup time, SCLK↑ to Fsync, slave mode, t_{su5} (see Figure 4–6)	30			ns
Setup time, Fsync to SCLK↑, slave mode, t_{su6} (see Figure 4–6)	30			ns
Load resistance at DOUT, R_L		10		kΩ
Operating free-air temperature, T_A	0		70	°C

NOTE 3: Voltages at analog inputs and outputs and AV_{DD} are with respect to the AV_{SS} terminal.

3.3 Electrical Characteristics

3.3.1 Digital Interface, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2	4.6		V
V_{IL}	Low-level input voltage			0.2	0.8	V
V_{OH}	High-level output voltage, DOUT	I_{OH} = 2 mA	2.4	4.6		V
V_{OL}	Low-level output voltage, DOUT	I_{OL} = 2 mA		0.2	0.4	V
I_{IH}	High-level input current, any digital input			1		µA
I_{IL}	Low-level input current, any digital input			1		µA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

3.3.2 Analog Interface

3.3.2.1 ADC Modulator, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V, f_s = 48 kHz, Bandwidth = 24 kHz, HPByp = 1, CMODE = 0, MODE0 – 2 = 101

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			18		Bits
DYNAMIC PERFORMANCE					
Signal to noise (EIAJ)	INLP = INRP = 2.5 V dc INLM = INRM = 2.5 V dc	93	97		dB
Dynamic range	–1dB down from 6-V differential input between INRP (INLP) and INRM (INLM)	91	95		dB
Signal to noise + distortion (THD + N)			91		dB
Total harmonic distortion (THD)			0.001%		
Interchannel isolation			108		dB
DC ACCURACY					
Gain error			±0.2		dB
Interchannel gain mismatch			±0.2		dB
Offset error (18-bit resolution)			±5		mV
Offset drift			±0.17		LSB/°C

3.3.2.2 Inputs/Supplies, T_A = 25°C, AV_{DD} = DV_{DD} = 5 V, f_s = 48 kHz, Bandwidth = 24 kHz, HPByp = 1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Input voltage	Differential input		6.4		V
	Single-ended input		3.2		
Input impedance			50		kΩ
POWER SUPPLIES					
Power-supply current	I_{DD} (analog), operating		22	30	mA
	I_{DD} (digital), operating		24	32	mA
	I_{DD} (analog), power down		100		μA
	I_{DD} (digital), power down		40		μA
Power dissipation			230		mW

3.3.3 Channel Characteristics, T_A = 25°C, AV_{DD}=DV_{DD} = 5 V, f_s = 48 kHz, HPByp = 1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband (–3 dB)	HPByp = 0	0.001		24	kHz
Passband ripple	30 Hz – 21.8 kHz		±0.01		dB
Stopband attenuation	26.2 kHz – 3046 kHz	80			dB
Group delay			$25/F_S$		s

3.4 Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
t_{d1}	Delay time, AnaPD↓ to DOUT valid (see Figure 2–1(c))		30		ns
$t_{d(MFSD)}$	Delay time, SCLK↓ to Fsync, master mode (see Figures 4–1, 4–2, 4–3, and 4–4)	–20		20	ns
$t_{d(MDD)}$	Delay time, SCLK↓ to DOUT, master mode (see Figures 4–1, 4–2, 4–3, and 4–4)	0		50	ns
$t_{d(MIRD)}$	Delay time, SCLK↓ to LRClk, master mode (see Figures 4–2 and 4–4)	–20		20	ns
$t_{d(SDD1)}$	Delay time, LRClk to DOUT, slave mode (see Figure 4–5)			50	ns
$t_{d(SDD2)}$	Delay time, SCLK↓ to DOUT, slave mode (see Figures 4–5 and 4–6)			50	ns

4 Parameter Measurement Information

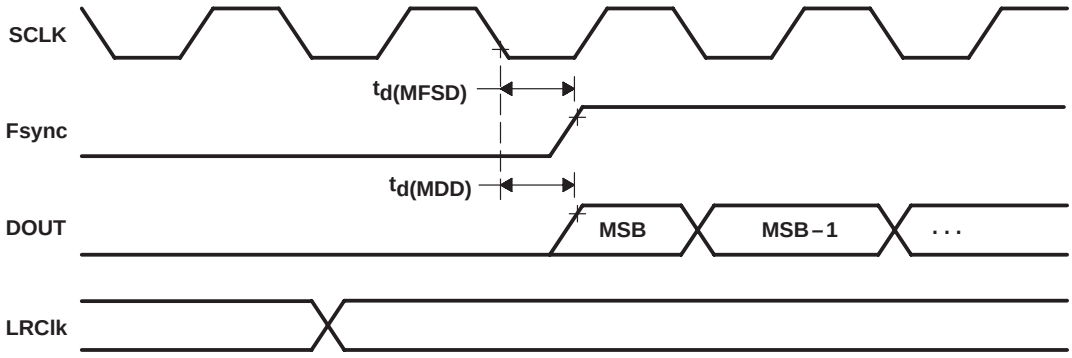


Figure 4–1. SCLK to Fsync and DOUT – Master Mode 3

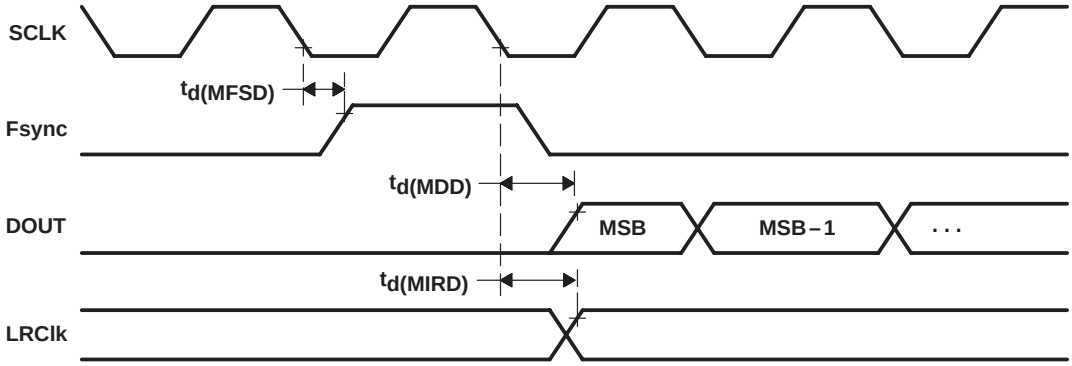


Figure 4–2. SCLK to Fsync, DOUT, and LRClk – Master Modes 4 and 6

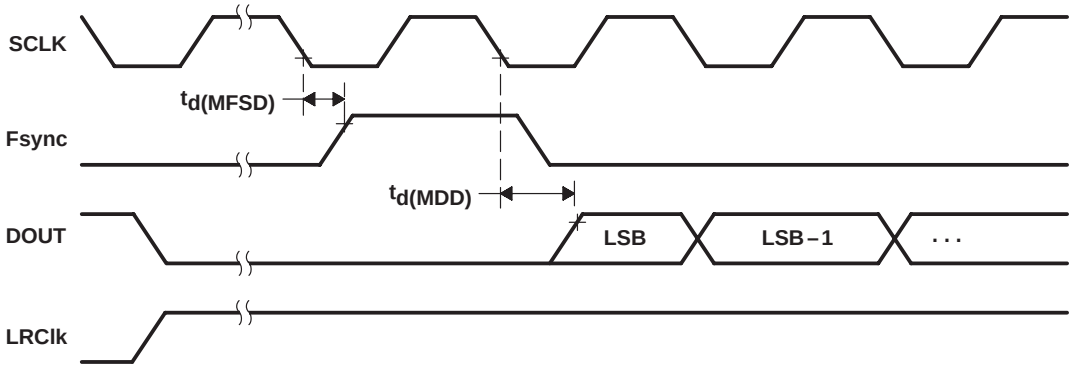


Figure 4–3. SCLK to Fsync, DOUT, and LRClk – Master Mode 5

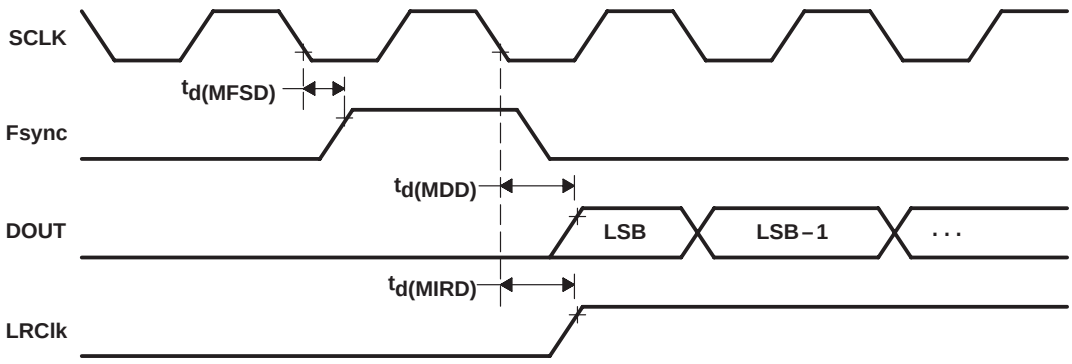


Figure 4–4. SCLK to Fsync, DOUT, and LRClk – Master Mode 7

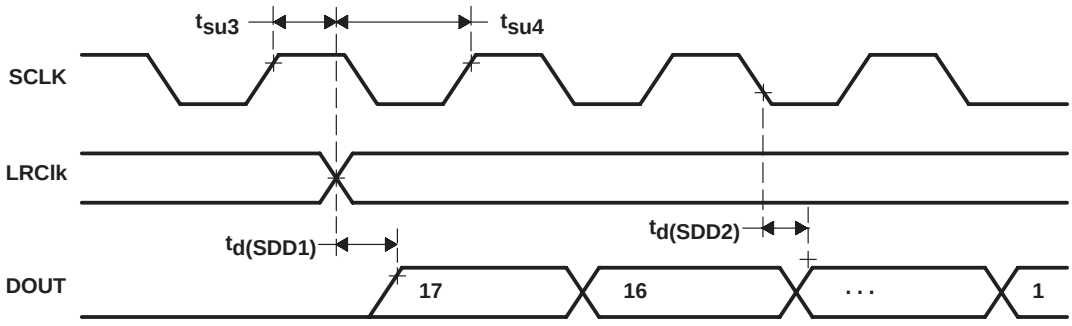


Figure 4–5. SCLK to LRClk and DOUT – Slave Mode 0, Fsync High

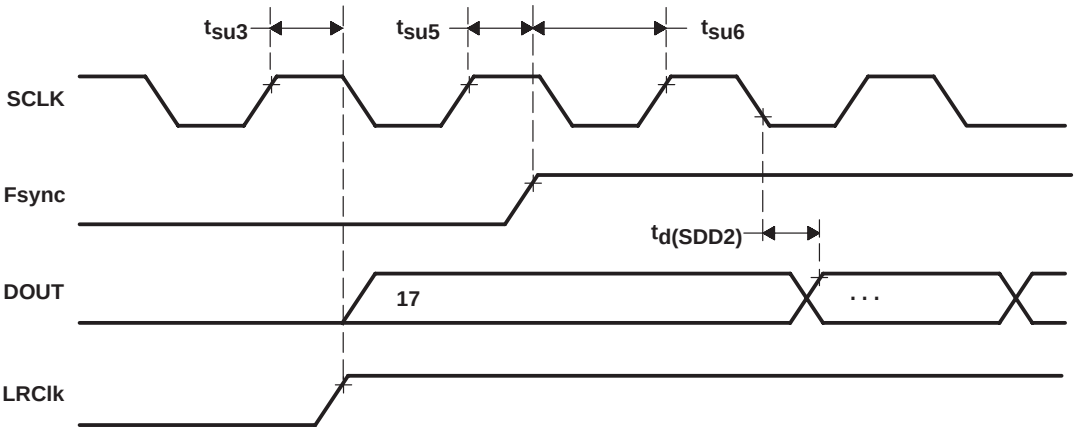


Figure 4–6. SCLK to Fsync, LRClk, and DOUT – Slave Mode 2, Fsync Controlled

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