SLLS053C – MAY 1989 – REVISED AUGUST 1999

- **Integrates Most Communications Card Functions From the IBM PC/AT™ or Compatibles With Single- or Dual-Channel Serial Ports**
- **TL16C451 Consists of One TL16C450 Plus Centronix Printer Interface**
- **TL16C452 Consists of Two TL16C450s Plus a Centronix-Type Printer Interface**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2 Stop-Bit Generation**
  - **Programmable Baud Rate (dc to 256 kbit/s)**
- **Fully Double Buffered for Reliable Asynchronous Operation**

description

The TL16C451 and TL16C452 provide single- and dual-channel (respectively) serial interfaces along with a single Centronix-type parallel-port interface. The serial interfaces provide a serial-to-parallel conversion for data received from a peripheral device or modem and a parallel-to-serial conversion for data transmitted by a CPU. The parallel interface provides a bidirectional parallel data port that fully conforms to the requirements for a Centronix-type printer interface. A CPU can read the status of the asynchronous communications element (ACE) interfaces at any point in the operation. The status includes the state of the modem signals ($\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{RLSD}}$, and RI) and any changes to these signals that have occurred since the last time they were read, the state of the transmitter and receiver including errors detected on received data, and printer status. The TL16C451 and TL16C452 provide control for modem signals ($\overline{\text{RTS}}$ and $\overline{\text{DTR}}$), interrupt enables, baud rate programming, and parallel-port control signals.

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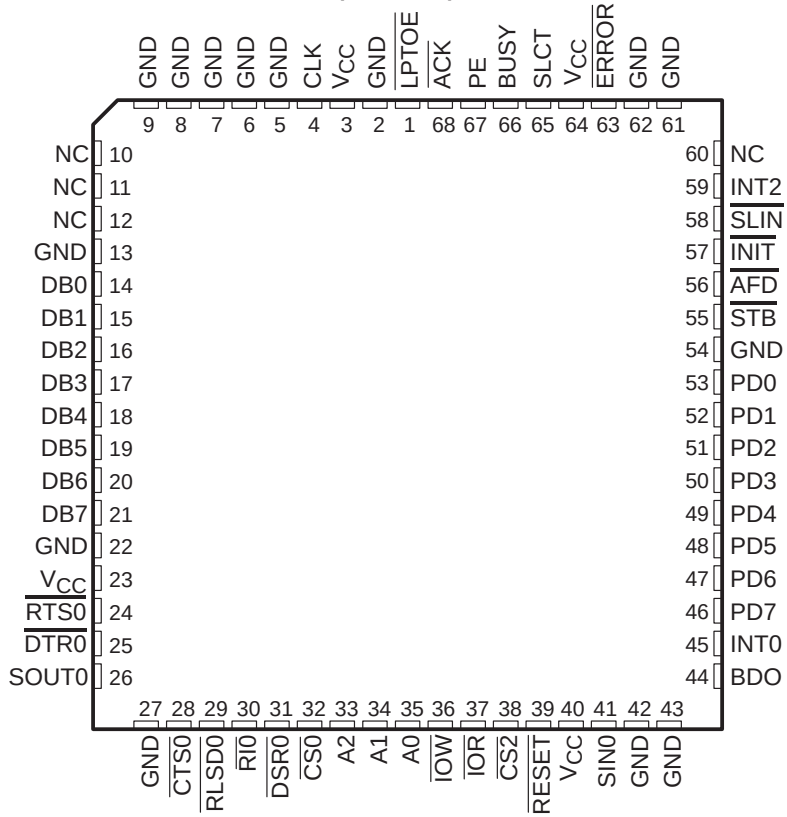
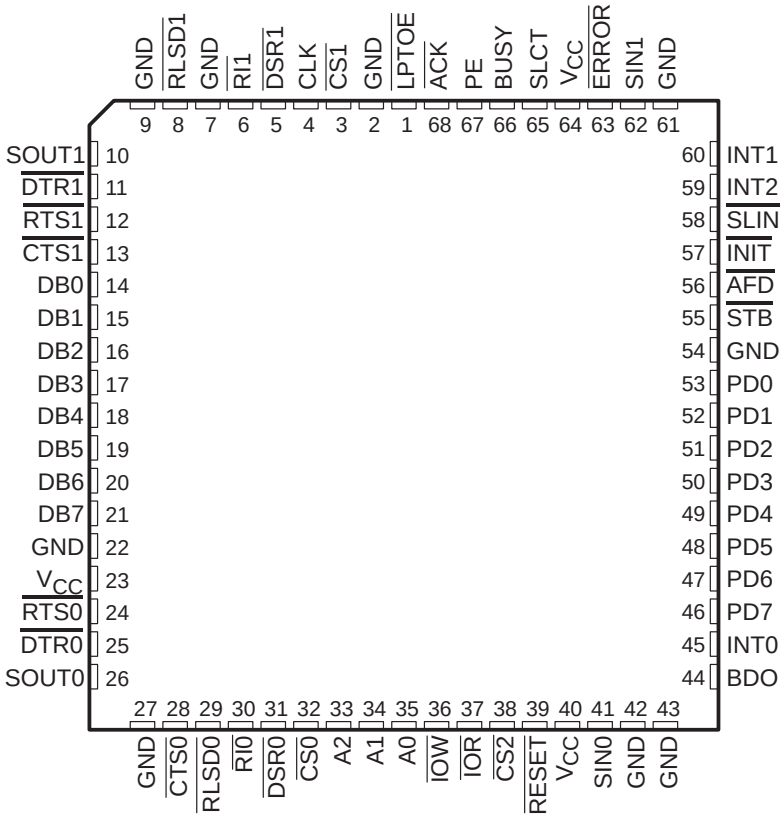
TL16C451 . . . FN PACKAGE
(TOP VIEW)

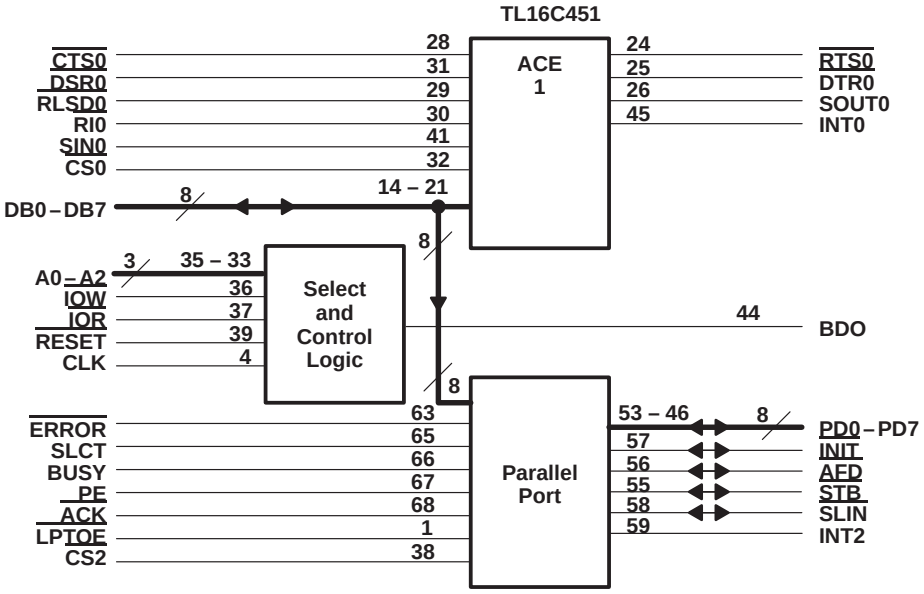


NC – No internal connection

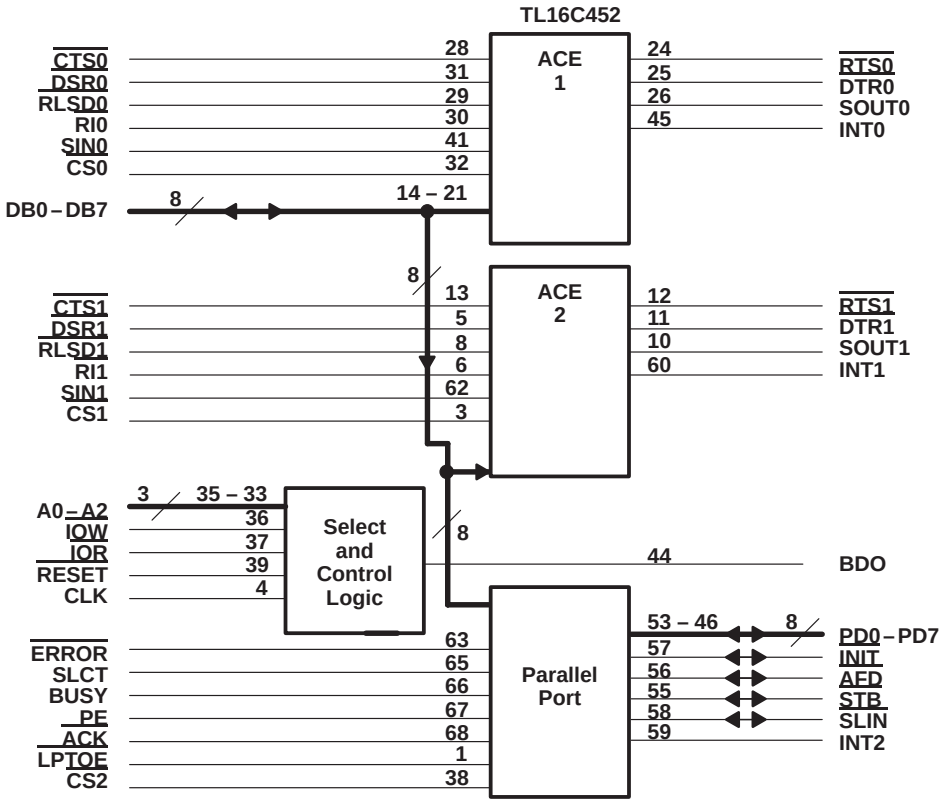
TL16C452 . . . FN PACKAGE
(TOP VIEW)



TL16C451 functional block diagram



TL16C452 functional block diagram



Terminal Functions

TERMINAL NAME†	TERMINAL NO.	I/O	DESCRIPTION
A0 A1 A2	35 34 33	I	Register select. A0, A1, and A2 are used during read and write operations to select the register to read from or write to. Refer to Table 1 for register addresses, also refer to the chip select signals ($\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$).
$\overline{ACK}$	68	I	Printer acknowledge. $\overline{ACK}$ goes low to indicate that a successful data transfer has taken place. It generates a printer port interrupt during its positive transition.
$\overline{AFD}$	56	I/O	Printer autofeed. $\overline{AFD}$ is an open-drain line that provides the printer with a low signal when continuous-form paper is to be autofed to the printer. An internal pullup is provided.
BDO	44	O	Bus buffer output. BDO is active (high) when the CPU is reading data. When active, this output can disable an external transceiver.
BUSY	66	I	Printer busy. BUSY is an input line from the printer that goes high when the printer is not ready to accept data.
CLK	4	I/O	External clock. CLK connects the ACE to the main timing reference.
$\overline{CS0}$ $\overline{CS1}$ [V_{CC}] $\overline{CS2}$	32 3 38	I	Chip selects. Each chip select enables read and write operations to its respective channel. $\overline{CS0}$ and $\overline{CS1}$ select serial channels 0 and 1, respectively, and $\overline{CS2}$ selects the parallel port.
$\overline{CTS0}$ CTS1 [GND]	28 13	I	Clear to send. $\overline{CTSx}$ is an active-low modem status signal. Its state can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{CTSx}$ changes state, an interrupt is generated.
DB0 – DB7	14 – 21	I/O	Data bus. Eight 3-state data lines provide a bidirectional path for data, control, and status information between the TL16C451/TL16C452 and the CPU. DB0 is the least significant bit (LSB).
$\overline{DSR0}$ DSR1 [GND]	31 5	I	Data set ready. $\overline{DSRx}$ is an active-low modem status signal. Its state can be checked by reading bit 5 (DSR) of the modem status register. Bit 1 (DDSR) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DSRx}$ changes state, an interrupt is generated.
$\overline{DTR0}$ $\overline{DTR1}$ [NC]	25 11	O	Data terminal ready. $\overline{DTRx}$, when active (low), informs a modem or data set that the ACE is ready to establish communication. $\overline{DTRx}$ is placed in the active state by setting the DTR bit of the modem control register. $\overline{DTRx}$ is placed in the inactive state either as a result of a reset or during loop mode operation or clearing bit 0 (DTR) of the modem control register.
$\overline{ERROR}$	63	I	Printer error. $\overline{ERROR}$ is an input line from the printer. The printer reports an error by holding this line low during the error condition.
$\overline{INIT}$	57	I/O	Printer initialize. $\overline{INIT}$ is an open-drain line that provides the printer with a signal that allows the printer initialization routine to be started. An internal pullup is provided.
INT0 INT1 [NC]	45 60	O	Interrupt. INTx is an active-high 3-state output that is enabled by bit 3 of the MCR. When active, INTx informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data is available, the transmitter holding register is empty, and an enabled modem status interrupt. The INTx output is reset (low) either when the interrupt is serviced or as a result of a reset.
INT2	59	O	Printer port interrupt. INT2 is an active-high 3-state output generated by the positive transition of $\overline{ACK}$. It is enabled by bit 4 of the write control register.
$\overline{IOR}$	37	I	Data read strobe. When $\overline{IOR}$ input is active (low) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register.
$\overline{IOW}$	36	I	Data write strobe. When $\overline{IOW}$ input is active (low) while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register.
$\overline{LPTOE}$	1	I	Parallel data output enable. When low, $\overline{LPTOE}$ enables the write data register to the PD0–PD7 lines. A high puts the PD0–PD7 lines in the high-impedance state allowing them to be used as inputs. $\overline{LPTOE}$ is usually tied low for printer operation.

† Names shown in brackets are for the TL16C451.

Terminal Functions (continued)

TERMINAL NAME†	TERMINAL NO.	I/O	DESCRIPTION
PD0–PD7	53–46	I/O	Parallel data bits (0–7). These eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when $\overline{\text{LPTOE}}$ is high.
PE	67	I	Printer paper empty. This is an input line from the printer that goes high when the printer runs out of paper.
$\overline{\text{RESET}}$	39	I	Reset. When active (low), $\overline{\text{RESET}}$ clears most ACE registers and sets the state of various output signals. Refer to Table 2.
$\overline{\text{RI0}}$ $\overline{\text{RI1}}$ [GND]	30 6	I	Ring indicator. $\overline{\text{RIx}}$ is an active-low modem status signal. Its state can be checked by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates that the $\overline{\text{RIx}}$ input has transitioned from a low to a high state since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{\text{RLSD0}}$ $\overline{\text{RLSD1}}$ [GND]	29 8	I	Receive line signal detect. $\overline{\text{RLSDx}}$ is an active-low modem status signal. Its state can be checked by reading bit 7 of the modem status register. Bit 3 (DRLSD) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{\text{RLSDx}}$ changes state, an interrupt is generated. This bit is low when a data carrier is detected.
$\overline{\text{RTS0}}$ $\overline{\text{RTS1}}$ [NC]	24 12	O	Request to send. When active (low), $\overline{\text{RTSx}}$ informs the modem or data set that the ACE is ready to transmit data. $\overline{\text{RTSx}}$ is set to its active state by setting the RTS modem control register bit and is set to its inactive (high) state either as a result of a reset or during loop mode operations or by clearing bit 1 (RTS) of the modem control register.
SIN0 SIN1 [GND]	41 62	I	Serial input. SINx is a serial data input from a connected communications device.
SLCT	65	I	Printer selected. SLCT is an input line from the printer that goes high when the printer has been selected.
$\overline{\text{SLIN}}$	58	I/O	Printer select. $\overline{\text{SLIN}}$ is an open-drain line that selects the printer when it is active (low). An internal pullup is provided on this line.
SOUT0 SOUT1 [NC]	26 10	I	Serial output. SOUTx is a composite serial data output to a connected communication device. SOUTx is set during a reset.
$\overline{\text{STB}}$	55	I/O	Printer strobe. $\overline{\text{STB}}$ is an open-drain line that provides communication synchronization between the TL16C451/TL16C452 and the printer. When it is active (low), it provides the printer with a signal to latch the data currently on the parallel port. An internal pullup is provided on this line.
V_{CC}	23,40, 64		5-V supply voltage
GND	2,7,9 22,27,42, 43,54,61		Supply common

† Names shown in brackets are for the TL16C451.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range at any input, V_I . . . . . –0.5 V to 7 V
Output voltage range, V_O . . . . . –0.5 V to 7 V
Continuous total power dissipation . . . . . 1100 mW
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 10 seconds, T_C . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level Input voltage, V_{IH}	2		V_{CC}	V
Low-level Input voltage, V_{IL}	–0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –0.4 mA on DB0–DB7	2.4			V
		I_{OH} = –2 mA to 4 mA on PD0–PD7				
		I_{OH} = –0.2 mA on INIT, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$				
		I_{OH} = –0.2 mA on all other outputs				
V_{OL}	Low-level output voltage	I_{OL} = 4 mA on DB0–DB7			0.4	V
		I_{OL} = 12 mA on PD0–PD7				
		I_{OL} = 10 mA on $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see Note 2)				
		I_{OL} = 2 mA on all other outputs				
I_{Ikg}	Input leakage current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other terminals floating			±10	µA
I_{oz}	High-impedance output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 to 5.25 V, Chip selected and in write mode, or chip deselected			±20	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, V_{SS} = 0, SIN, $\overline{DSR}$, $\overline{RLSD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs, Baud rate = 50 kbit/s			10	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ are open-collector output terminals that each have an internal pullup to V_{CC}. This generates a maximum of 2 mA of internal I_{OL} per terminal. In addition to this internal current, each terminal sinks at least 10 mA while maintaining the V_{OL} specification of 0.4 V maximum.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	MIN	MAX	UNIT
t_{cR}	Cycle time, read (t_{w7} + t_{d8} + t_{d9})		175		ns

t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)		175	ns
t_{w1}	Pulse duration, clock↑	1	50	ns
t_{w2}	Pulse duration, clock↓	1	50	ns
t_{w5}	Pulse duration, write strobe ($\overline{IOW}$)↑	2	80	ns
t_{w6}	Pulse duration, read strobe ($\overline{IOR}$)↓	3	80	ns
t_{wRST}	Pulse duration, reset		1000	ns
t_{su1}	Setup time, address (A0 – A2) valid before $\overline{IOW}$↓	2,3	15	ns
t_{su2}	Setup time, chip select ($\overline{CSx}$) valid before $\overline{IOW}$↓	2,3	15	ns
t_{su3}	Setup time, data (D0 – D7) valid before $\overline{IOW}$↑	2	15	ns
t_{h1}	Hold time, address (A0 – A2) valid after $\overline{IOW}$↑	2,3	20	ns
t_{h2}	Hold time, chip select ($\overline{CSx}$) valid after $\overline{IOW}$↑	2,3	20	ns
t_{h3}	Hold time, data (D0 – D7) valid before $\overline{IOW}$↑	2	15	ns
t_{d3}	Delay time, write cycle ($\overline{IOW}$)↑ to $\overline{IOW}$↓	2	80	ns
t_{d4}	Delay time, read cycle ($\overline{IOR}$)↑ to $\overline{IOR}$↓	3	80	ns

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d5}	Delay time, data (D0 – D7) valid before read ($\overline{IOR}$)↑	3	C_L = 100 pF		60	ns
t_{d6}	Delay time, floating data (D0 – D7) valid after read ($\overline{IOR}$)↑	3	C_L = 100 pF	0	60	ns
$t_{dis(R)}$	Read to driver disable, $\overline{IOR}$↓ to BD0↓	3	C_L = 100 pF		60	ns

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d7}	Delay time, RCLK↑ to sample clock↑	4			100	ns
t_{d8}	Delay time, stop (sample clock)↑ to set interrupt (INTRPT)↑	4		1	1	RCLK cycles
t_{d9}	Delay time, read RBR/LSR ($\overline{IOR}$)↑ to reset interrupt (INTRPT)↓	4	C_L = 100 pF		140	ns

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d10}	Delay time, initial write THR ($\overline{IOW}$)↑ to transmit start (SOUT)↓	5		8	24	baudout cycles
t_{d11}	Delay time, stop (SOUT) low to interrupt (INTRPT)↑	5		8	8	baudout cycles
t_{d12}	Delay time, write THR ($\overline{IOW}$)↓ to reset interrupt (INTRPT) low	5	C_L = 100 pF		140	ns
t_{d13}	Delay time, initial write ($\overline{IOW}$)↑ to THRE interrupt (INTRPT)↑	5		16	32	baudout cycles
t_{d14}	Delay time, read IIR ($\overline{IOR}$)↑ to reset THRE interrupt (INTRPT) low	5	C_L = 100 pF		140	ns

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature

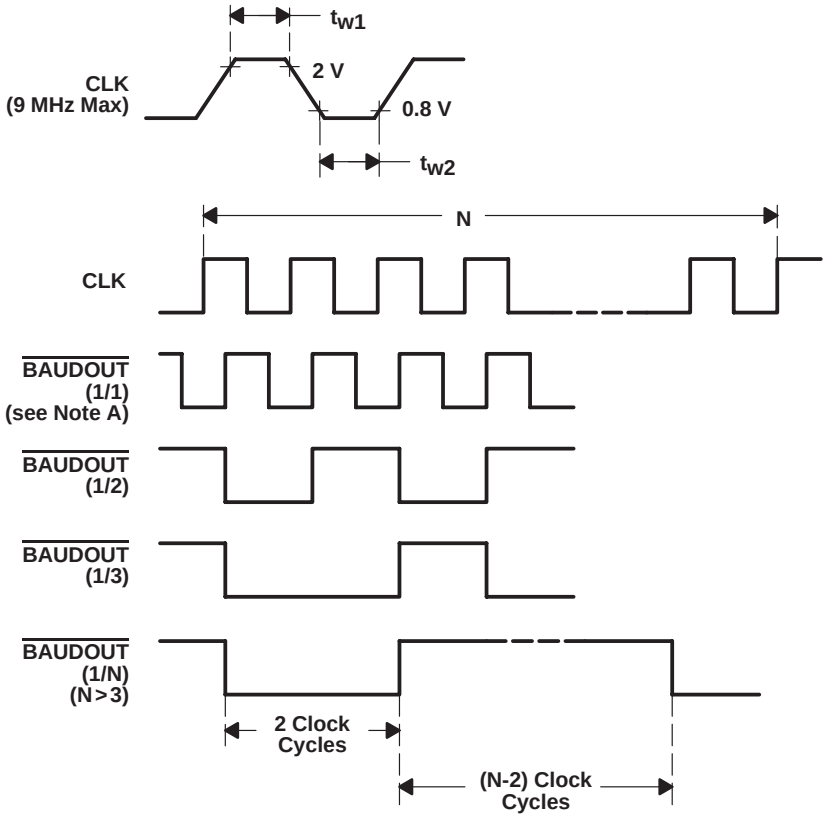
PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, write MCR ($\overline{IOW}$)↑ to output ($\overline{RTS}$, $\overline{DTS}$)↓↑	6	C_L = 100 pF		100	ns

t_{d16}	Delay time, modem input ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$)↑ to set interrupt (INTRPT) high	6	C_L = 100 pF	170	ns
t_{d17}	Delay time, read MSR ($\overline{IOR}$)↑ to reset interrupt (INTRPT) low	6	C_L = 100 pF	140	ns

parallel port switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d18}	Delay time, write parallel port control ($\overline{SLIN}$, $\overline{AFD}$, $\overline{STB}$, $\overline{INIT}$)↓↑ to output ($\overline{IOW}$) high	7	C_L = 100 pF		60	ns
t_{d19}	Delay time, write parallel port data (P0 – P7)↓↑ to output ($\overline{IOW}$) high	7	C_L = 100 pF		60	ns
t_{d20}	Delay time, output enable to data, PD0 – PD7 valid after $\overline{LPTOE}$↓	7	C_L = 100 pF		60	ns
t_{d21}	Delay time, $\overline{ACK}$↓↑ to INT2↓↑	7	C_L = 100 pF		100	ns

PARAMETER MEASUREMENT INFORMATION



NOTE A: $\overline{BAUDOUT}$ is an internally generated signal used in the receiver and transmitter circuits to synchronize data.

Figure 1. Baud Generator Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

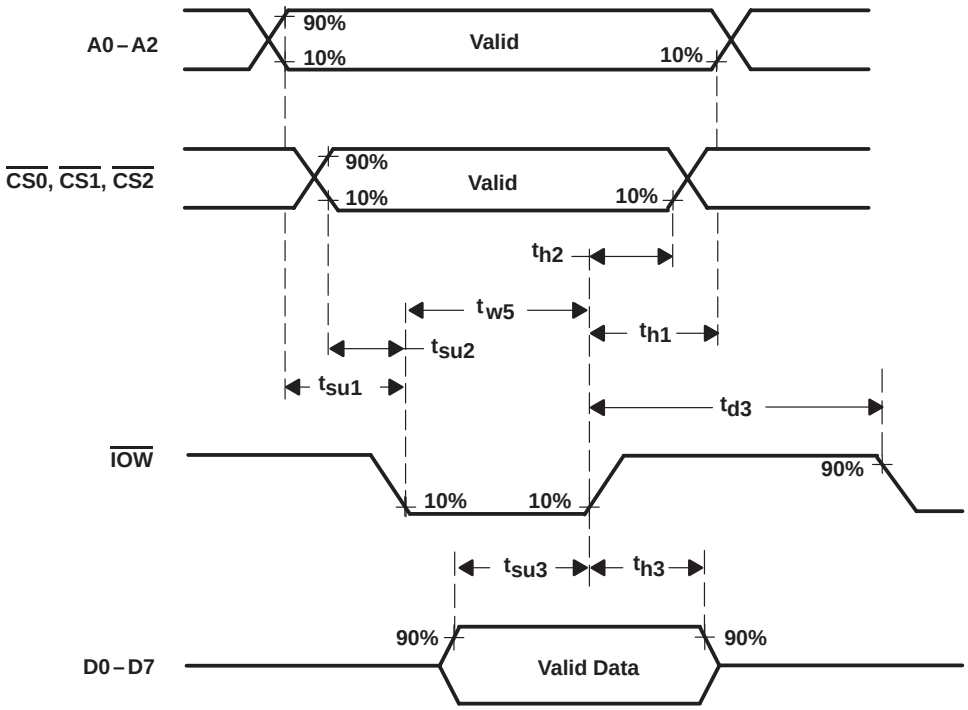


Figure 2. Write Cycle Timing Waveforms

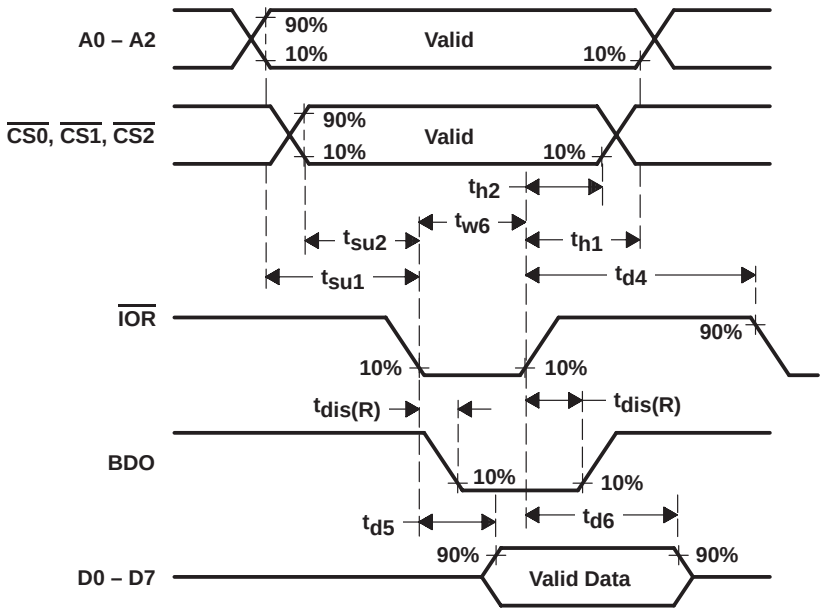


Figure 3. Read Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

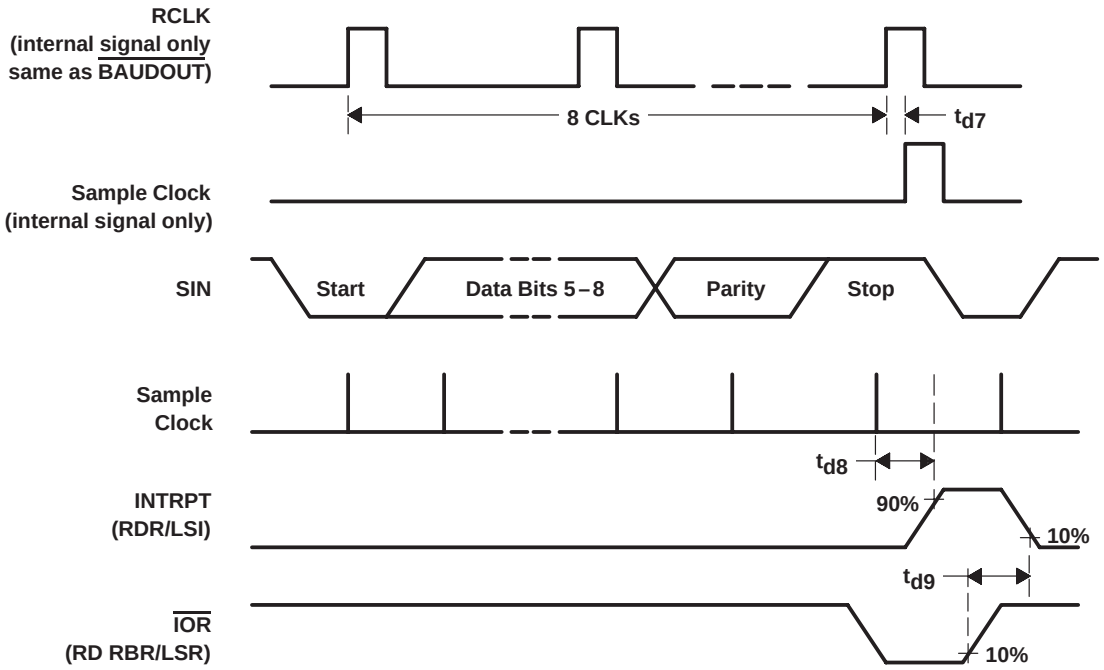


Figure 4. Receiver Timing Waveforms

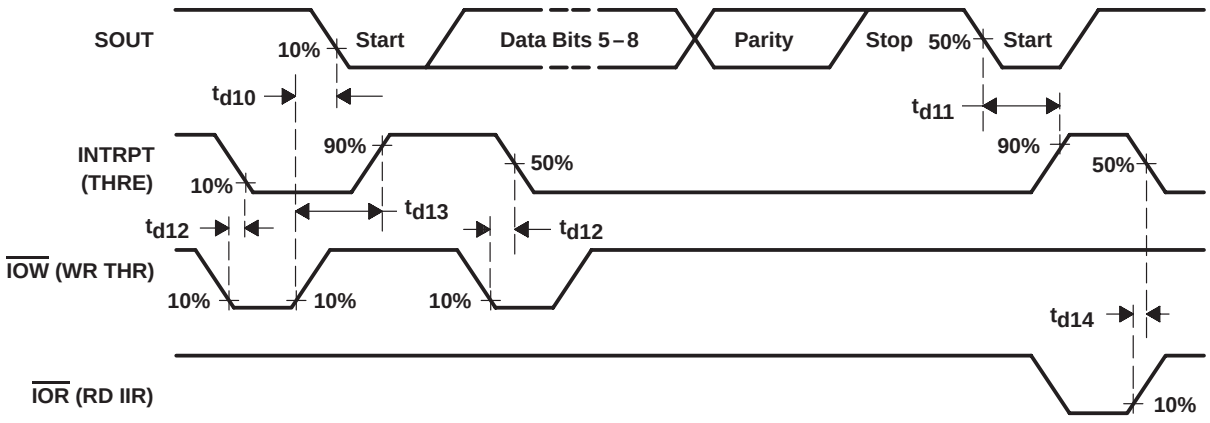


Figure 5. Transmitter Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

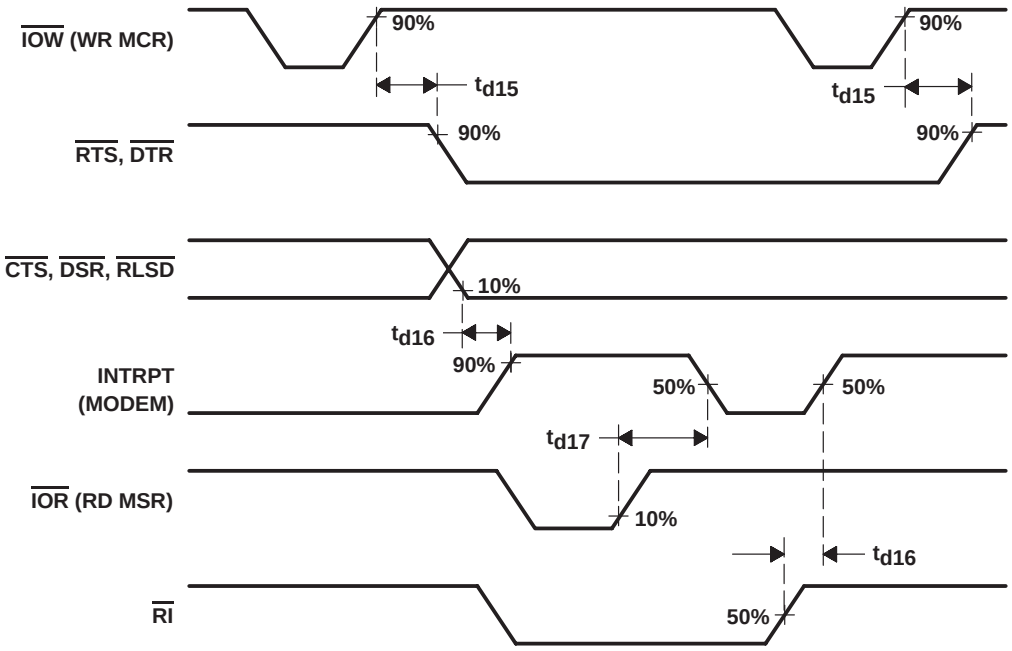


Figure 6. Modem Control Timing Waveforms

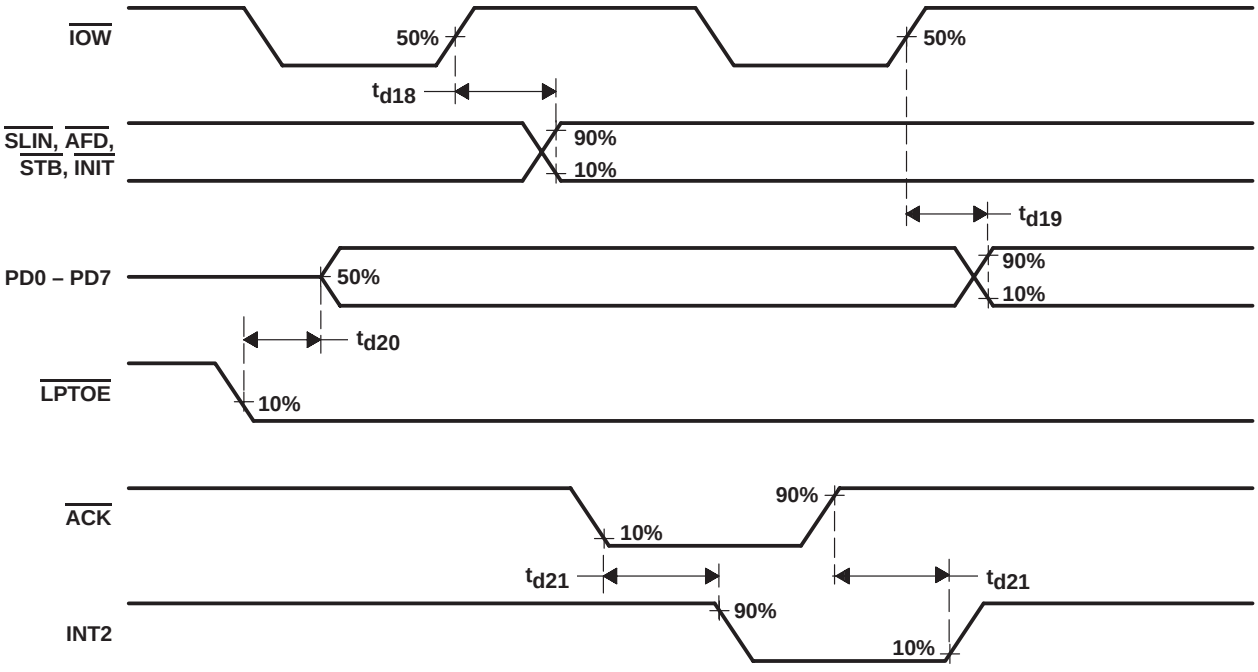


Figure 7. Parallel Port Timing Waveforms

APPLICATION INFORMATION

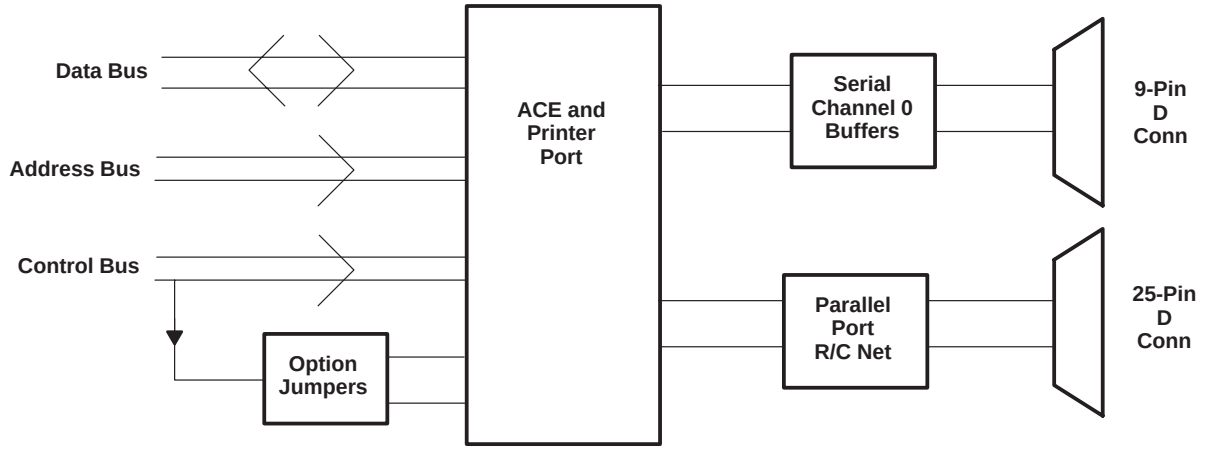


Figure 8. Basic TL16C451 Test Configuration

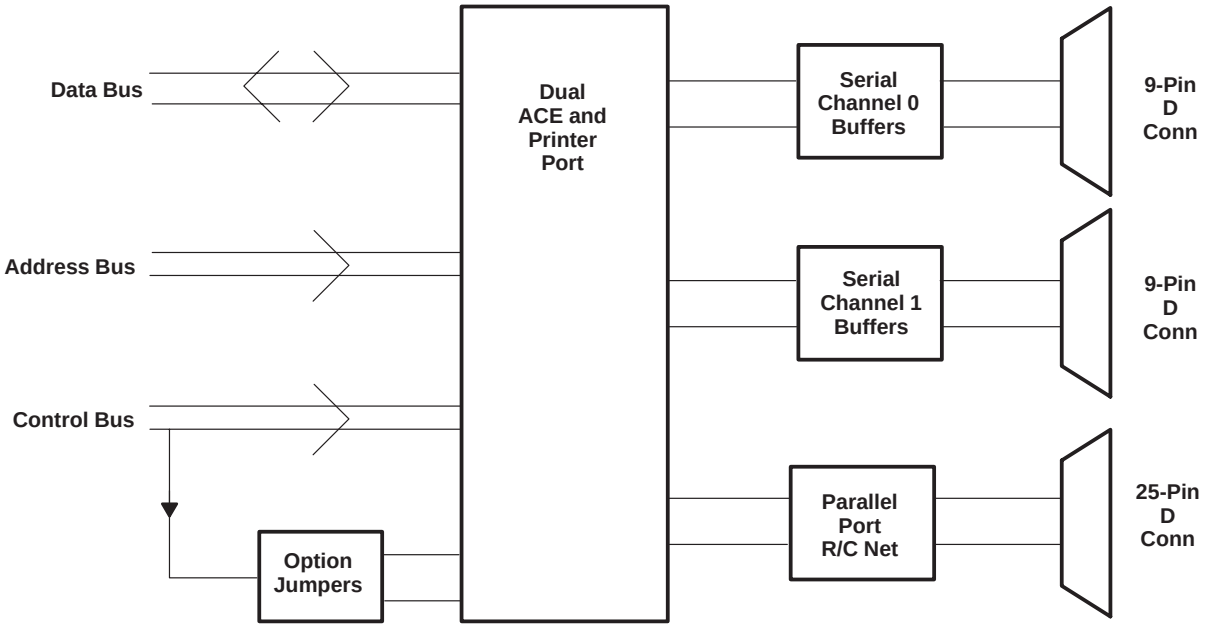


Figure 9. Basic TL16C452 Test Configuration

PRINCIPLES OF OPERATION

Table 1. Register Selection

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable register
X	L	H	L	Interrupt identification register (read only)
X	L	H	H	Line control register
X	H	L	L	Modem control register
X	H	L	H	Line status register
X	H	H	L	Modem status register
X	H	H	H	Scratch register
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

† The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 3).

Table 2. ACE Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt enable register	$\overline{\text{RESET}}$	All bits cleared (0–3 forced and 4–7 permanent)
Interrupt identification register	$\overline{\text{RESET}}$	Bit 0 is set, bits 1 and 2 are cleared, and bits 3–7 are permanently cleared
Line control register	$\overline{\text{RESET}}$	All bits cleared
Modem control register	$\overline{\text{RESET}}$	All bits cleared
Line status register	$\overline{\text{RESET}}$	Bits 5 and 6 are set, all other bits are cleared
Modem status register	$\overline{\text{RESET}}$	Bits 0–3 are cleared, bits 4–7 are input signals
SOUT	$\overline{\text{RESET}}$	High
INTRPT (receiver error flag)	Read LSR/$\overline{\text{RESET}}$	Low
INTRPT (received data available)	Read RBR/$\overline{\text{RESET}}$	Low
INTRPT (transmitter holding register empty)	Read IIR/Write THR/$\overline{\text{RESET}}$	Low
INTRPT (modem status changes)	Read MSR/$\overline{\text{RESET}}$	Low
$\overline{\text{OUT2}}$ (interrupt enable)	$\overline{\text{RESET}}$	High
$\overline{\text{RTS}}$	$\overline{\text{RESET}}$	High
$\overline{\text{DTR}}$	$\overline{\text{RESET}}$	High
$\overline{\text{OUT1}}$	$\overline{\text{RESET}}$	High
Scratch register	$\overline{\text{RESET}}$	No effect
Divisor latch (LSB and MSB) registers	$\overline{\text{RESET}}$	No effect
Receiver buffer registers	$\overline{\text{RESET}}$	No effect
Transmitter holding registers	$\overline{\text{RESET}}$	No effect

PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers are given in Table 3.

Table 3. Summary of Accessible Registers

Bit No.	REGISTER ADDRESS										
	O DLAB = 0	O DLAB = 0	1 DLAB = 0	2	3	4	5	6	7	O DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0†	Data Bit 0	Enable Received Data Available Interrupt (ERBF)	"0" If Interrupt Pending	Word Length Select Bit 0 (WLSO)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBE)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2 (Interrupt Enable)	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmit-ter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmit-ter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Receive Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15

† Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

PRINCIPLES OF OPERATION

interrupt control logic

The interrupt control logic is shown in Figure 10.

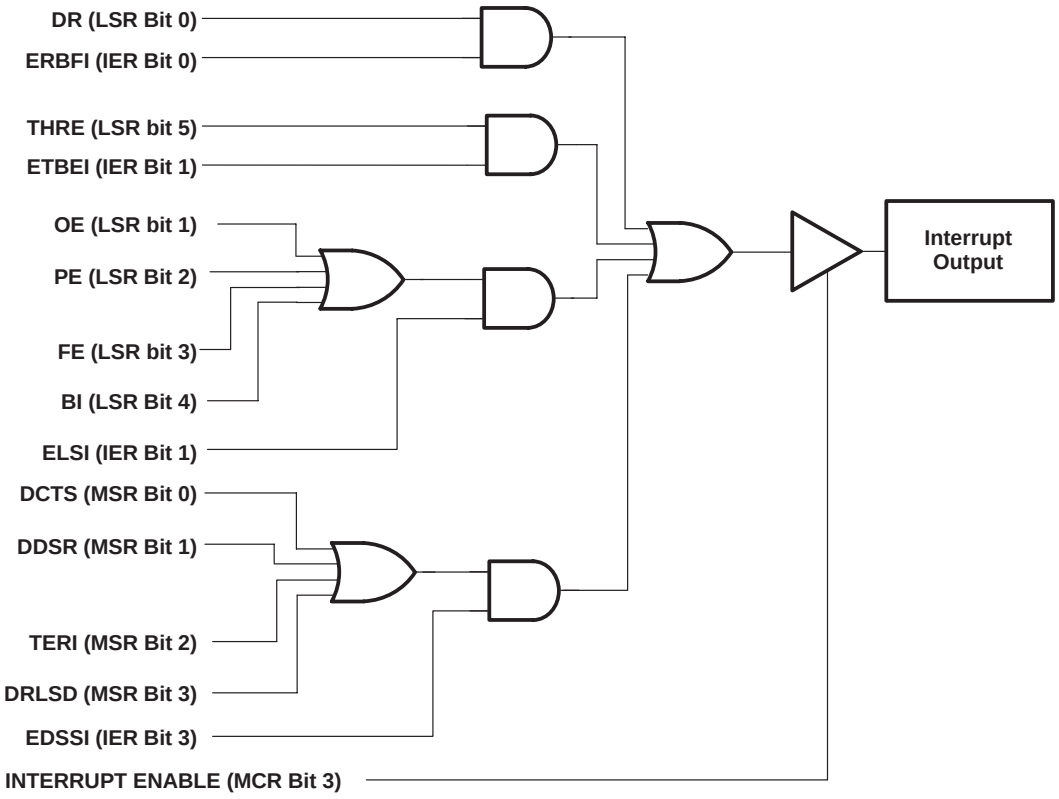


Figure 10. Interrupt Control Logic

interrupt enable register (IER)

The IER enables each of the four types of interrupts (refer to Table 4) and the INTRPT output signal in response to an interrupt generation. The IER can also disable the interrupt system by clearing bits 0 through 3. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit, when set, enables the received data available interrupt.
- Bit 1: This bit, when set, enables the THRE interrupt.
- Bit 2: This bit, when set, enables the receiver line status interrupt.
- Bit 3: This bit, when set, enables the modem status interrupt.
- Bits 4 thru 7: These bits in the IER are not used and are always cleared.

PRINCIPLES OF OPERATION

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most microprocessors.

The ACE provides four prioritized levels of interrupts:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the IIR indicates that an interrupt is pending and indicates the type of interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4.

- Bit 0: This bit can be used either in a hardwire prioritized or polled interrupt system. When this bit is cleared, an interrupt is pending. When bit 0 is set, no interrupt is pending.
- Bits 1 and 2: These two bits identify the highest priority interrupt pending as indicated in Table 4.
- Bits 3 – 7: These bits in the interrupt identification register are not used and are always clear.

Table 4. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER			PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 2	BIT 1	BIT 0				
0	0	1	None	None	None	–
1	1	0	1	Receiver line status	Overrun error, parity error, framing error or break interrupt	Reading the line status register
1	0	0	2	Received data available	Receiver data available	Reading the receiver buffer register
0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Reading the interrupt Identification register (if source of interrupt) or writing into the transmitter holding register
0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Reading the modem status register

PRINCIPLES OF OPERATION

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the LCR. In addition, the programmer is able to retrieve, inspect, and modify the contents of the LCR; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as shown in Table 5.

Table 5. Serial Character Word Length

Bit 1	Bit 0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- Bit 2: This bit specifies either one, one and one-half, or two stop bits in each transmitted character. When bit 2 is cleared, one stop bit is generated in the data. When bit 2 is set, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The number of stop bits generated in relation to word length and bit 2 is as shown in Table 6.

Table 6. Number of Stop Bits Generated

Bit 2	Word Length Selected by Bits 1 and 2	Number of Stop Bits Generated
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

- Bit 3: This bit is the parity enable bit. When bit 3 is set, a parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, when bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.
- Bit 4: This bit is the even parity select bit. When parity is enabled (bit 3 is set) and bit 4 is set, even parity (an even number of logic is in the data and parity bits) is selected. When parity is enabled and bit 4 is cleared, odd parity (an odd number of logic 1s) is selected.
- Bit 5: This is the stick parity bit. When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set.
- Bit 6: This bit is the break control bit. Bit 6 is set to force a break condition, i.e, a condition where SOUT terminal is forced to the spacing (cleared) state. When bit 6 is cleared, the break condition is disabled. The break condition has no affect on the transmitter logic, it only affects the serial output.
- Bit 7: This bit is the divisor latch access bit (DLAB). Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the receiver buffer, the THR, or the IER.

PRINCIPLES OF OPERATION

line status register (LSR)†

The LSR provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit is the data ready (DR) indicator for the receiver. Bit 0 is set whenever a complete incoming character has been received and transferred into the RBR and is cleared by reading the RBR.
- Bit 1‡: This bit is the overrun error (OE) indicator. When bit 1 is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. The OE indicator is cleared every time the CPU reads the contents of the LSR.
- Bit 2‡: This bit is the parity error (PE) indicator. When bit 2 is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). The PE bit is cleared every time the CPU reads the contents of the LSR.
- Bit 3‡: This bit is the framing error (FE) indicator. When bit 3 is set, it indicates that the received character did not have a valid (set) stop bit. The FE bit is cleared every time the CPU reads the contents of the LSR.
- Bit 4‡: This bit is the break interrupt (BI) indicator. When bit 4 is set, it indicates that the received data input was held clear for longer than a full-word transmission time. A full-word transmission time is defined as the total time of the start, data, parity, and stop bits. The BI bit is cleared every time the CPU reads the contents of the LSR.
- Bit 5: This bit is the THRE indicator. Bit 5 is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is set, then an interrupt is generated. THRE is set when the contents of the THR are transferred to the transmitted shift register. This bit is cleared concurrent with the loading of the THR by the CPU.
- Bit 6: This bit is the transmitter empty (TEMT) indicator, bit 6 is set when the THR and the transmitter shift register are both empty. When either the THR or the transmitter shift register contains a data character, the TEMT bit is cleared.
- Bit 7: This bit is always clear.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

modem control register (MCR)

The MCR is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit (DTR) controls the data terminal ready ($\overline{\text{DTR}}$) output. Setting bit 0 forces the $\overline{\text{DTR}}$ output to its active state (low). When bit 0 is cleared, $\overline{\text{DTR}}$ goes high.
- Bit 1: This bit (RTS) controls the request to send ($\overline{\text{RTS}}$) output in a manner identical to bit 0's control over the $\overline{\text{DTR}}$ output.
- Bit 2: This bit (OUT 1) is a reserved location used only in the loopback mode.
- Bit 3: This bit (OUT 2) controls the output enable for the interrupt signal. When set, the interrupt is enabled. When bit 3 is cleared, the interrupt is disabled.

PRINCIPLES OF OPERATION

modem control register (MCR) (continued)

- Bit 4: This bit provides a local loopback feature for diagnostic testing of the ACE. When this bit is set, the following occurs:

  1. The SOUT is asserted high.
  2. The SIN is disconnected.
  3. The output of the transmitter shift register is looped back into the receiver shift register input.
  4. The four modem status inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected.
  5. The MCR bits (DTR, RTS, OUT1, and OUT2) are connected to the modem status register bits (DSR, CTS, RI, and RLSD), respectively.
  6. The four modem control output terminals are forced to their inactive states (high).

  In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit and receive data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt sources are now the lower four bits of the MCR instead of the four modem control inputs. All interrupts are still controlled by the IER.

- Bits 5 through 7: These bits are always cleared.

modem status register (MSR)

The MSR is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provides change information; when a control input from the modem changes state the appropriate bit is set. All four bits are cleared when the CPU reads the MSR. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0. This bit is the delta clear to send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input has changed states since the last time it was read by the CPU. When this bit is set and the modem status Interrupt is enabled, a modem status interrupt is generated.
- Bit 1. This bit is the delta data set ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input has changed states since the last time it was read by the CPU. When this bit is set and the modem status Interrupt is enabled, a modem status interrupt is generated.
- Bit 2. This bit is the trailing edge of ring indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state. When this bit is set and the modem status Interrupt is enabled, a modem status interrupt is generated.
- Bit 3. This bit is the delta receive line signal detect (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed states since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 4. This bit is the complement of the clear to send ($\overline{CTS}$) input. When bit 4 (loop) of the MCR is set, bit 4 is equivalent to the MCR bit 1 (RTS).
- Bit 5. This bit is the complement of the data set ready ($\overline{DSR}$) input. When bit 4 (loop) of the MCR is set, bit 5 is equivalent to the MCR bit 0 (DTR).
- Bit 6. This bit is the complement of the ring indicator ($\overline{RI}$) input. When bit 4 (loop) of the MCR is set, bit 6 is equivalent to the MCR bit 2 (OUT 1).
- Bit 7. This bit is the complement of the receive line signal detect ($\overline{RLSD}$) input. When bit 4 (loop) of the MCR is set, bit 7 is equivalent to the MCR bit 3 (OUT 2).

PRINCIPLES OF OPERATION

parallel port registers

The parallel port registers interface either device to a Centronix-style printer interface. When chip select 2 ($\overline{CS2}$) is low, the parallel port is selected. Tables 7 and 8 show the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read ($\overline{IOR}$) and write ($\overline{IOW}$) terminal as shown. The read data register allows the microprocessor to read the information on the parallel bus.

The read status register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are printer busy ($\overline{BUSY}$), acknowledge ($\overline{ACK}$) which is a handshake function, paper empty (PE), printer selected (SLCT), and error ($\overline{ERROR}$). The read control register allows the state of the control lines to be read. The write control register sets the state of the control lines, which are interrupt enable (IRQ ENB), select in (SLIN), initialize the printer ($\overline{INIT}$), autofeed the paper (AFD), and strobe (STB), which informs the printer of the presence of a valid byte on the parallel bus. These signals are cleared when a reset occurs. The write data register allows the microprocessor to write a byte to the parallel bus. The parallel port is completely compatible with the parallel port implementation used in the IBM serial/parallel adaptor.

Table 7. Parallel Port Registers

REGISTER	REGISTER BITS							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Read data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read status	$\overline{BUSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	1	1	1
Read control	1	1	1	IRQ ENB	SLIN	$\overline{INIT}$	AFD	STB
Write data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write control	1	1	1	IRQ ENB	SLIN	$\overline{INIT}$	AFD	STB

Table 8. Parallel Port Register Select

CONTROL TERMINALS					REGISTER SELECTED
$\overline{IOR}$	$\overline{IOW}$	$\overline{CS2}$	A1	A0	
L	H	L	L	L	Read data
L	H	L	L	H	Read status
L	H	L	H	L	Read control
L	H	L	H	H	Invalid
H	L	L	L	L	Write data
H	L	L	L	H	Invalid
H	L	L	H	L	Write control
H	L	L	H	H	Invalid

PRINCIPLES OF OPERATION

programmable baud generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 9 MHz and divides it by a divisor in the range between 1 and ($2^{16}-1$). The output frequency of the baud generator is sixteen times (16×) the baud rate. The formula for the divisor is:

divisor # = CLK frequency input ÷ (desired baud rate × 16)

Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load. For baud rates of 38.4 kilobits per second and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency.

receiver buffer register (RBR)

The ACE receiver section consists of a receiver shift register and an RBR. Timing is supplied by the 16× receiver clock (RCLK). Receiver section control is a function of the ACE line control register.

The ACE receiver shift register receives serial data from the serial input (SIN) terminal. The receiver shift register then converts the data to a parallel form and loads it into the RBR. When a character is placed in the RBR and the received data available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the RBR.

scratch register

The scratch register is an 8-bit register that is intended for programmer use as a scratchpad, in the sense that it temporarily holds programmer data without affecting any other ACE operation.

transmitter holding register (THR)

The ACE transmitter section consists of a THR and a transmitter shift register. Timing is supplied by the baud out ($\overline{\text{BAUDOUT}}$) clock signal. Transmitter section control is a function of the ACE line control register.

The ACE THR receives data off of the internal data bus and, when the shift register is idle, moves it into the transmitter shift register. The transmitter shift register serializes the data and outputs it at the serial output (SOUT). When the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register.

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