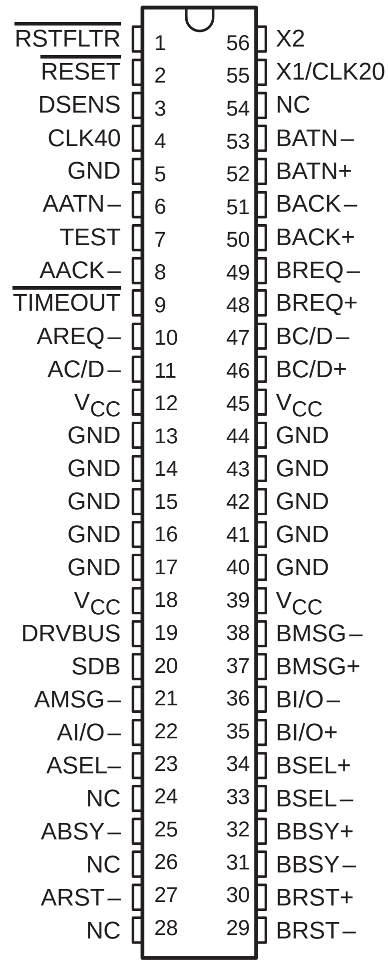
- **Provides Differential SCSI from Single-Ended Controller When Used With the SN75LBC971A Data Transceiver**
- **Designed to Operate at Fast-SCSI Speeds of 10 Million Data Transfers per Second**
- **Nine Transceivers Meet or Exceed the Requirements of ANSI Standard EIA-485 and ISO-8482 Standards**
- **Packaged in Shrink Small-Outline Package with 25 mil Terminal Pitch**
- **Low Disabled Supply Current**
  22 mA Typ
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Power-Up/-Down Glitch Protection**

DL PACKAGE
(TOP VIEW)



NC – no internal connection

Terminals 13 through 17 and 40 through 44 are connected together to the package lead frame and signal ground.

description

The SN75LBC970A SCSI differential converter-control is an adaptation of the industry's first 9-channel RS-485 transceiver, the SN75LBC976. When used in conjunction with one or more of its companion data transceiver(s), SN75LBC971A, the chip set provides the superior electrical performance of differential SCSI from a single-ended SCSI bus controller. A 16-bit, Fast-SCSI bus can be implemented with just three devices (two for data and one for control) in the space-efficient, 56-pin, shrink small-outline package (SSOP) and a few external components.

In a typical differential SCSI node, the SCSI controller provides the enables for each external RS-485 transceiver. This could require as many as 27 additional terminals for a 16-bit differential bus controller or relegate a 16-bit single-ended controller to only an 8-bit differential bus. Using the standard nine SCSI control signals, the SN75LBC970A control transceiver decodes the state of the bus and enables the SN75LBC971A data transceiver(s) to transmit the single-ended SCSI input signals differentially to the cable or receive the differential cable signals and drive the single-ended outputs to the controller.

The single-ended SCSI bus interface consists of CMOS bidirectional inputs and outputs. The drivers are rated at ±16 mA of output current. The receiver inputs are pulled high with approximately 4 mA to eliminate the need for external pullup resistors for the open-drain outputs of most single-ended SCSI controllers. The single-ended side of the device is not intended to drive the SCSI bus directly.

description (continued)

The differential SCSI bus interface consists of bipolar bidirectional inputs and outputs that meet or exceed the requirements of EIA-485 and ISO 8482-1982/TIA TR30.2 referenced by the American National Standard of Information Systems (ANSI) X3.131-1994 Small Computer System Interface-2 (SCSI-2).

The SN75LBC970A is characterized for operation over the temperature range of 0°C to 70°C.

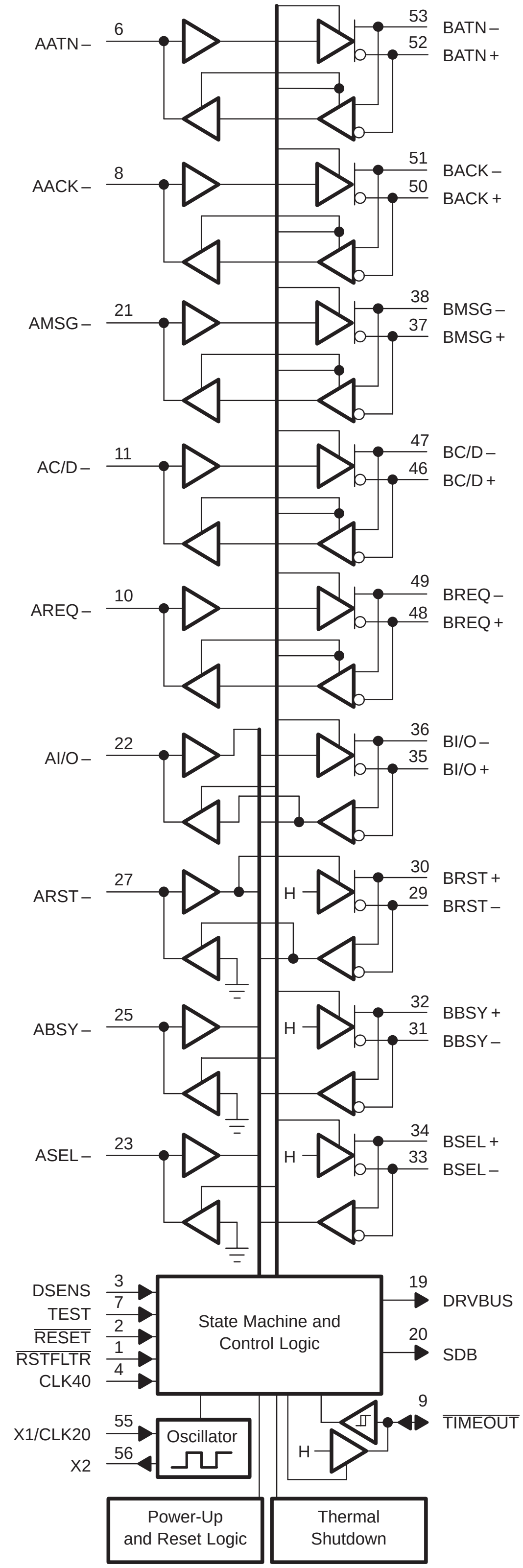
The SN75LBC970A consists of nine RS-485 differential transceivers, nine TTL- or CMOS-level compatible transceivers, a state machine and control logic block, a 20-MHz crystal-controlled oscillator, a timer, a power-up/-down glitch protection circuit, and a thermal-shutdown protection circuit.

The single-ended or controller interface is designated as the A side and the differential port is the B side. Since the device uses the SCSI control signals to decode the state of the bus and data flow direction, the terminal assignments must be matched to the corresponding signal on the SCSI bus. The signal name followed by a minus sign (–) indicates an active-low signal while a plus sign (+) indicates an active-high signal.

A reset function, which disables all outputs and clears internal latches, can be accomplished from two external inputs and two internally-generated signals. $\overline{\text{RESET}}$ (Reset) and DSENS (differential sense) are available to external circuits for a bus reset or to disable all outputs should a single-ended cable be inadvertently connected to a differential connector. The power-up and thermal-shutdown are internally generated signals that have the same effect when the supply voltage is below 3.5 V or the junction temperature exceeds approximately 175°C.

This data sheet contains descriptions of the SN75LBC970A input and output signals followed by the electrical characteristics. The parameter measurement information is followed by the theory of operation, a state flow chart, and a typical circuit in the application information section.

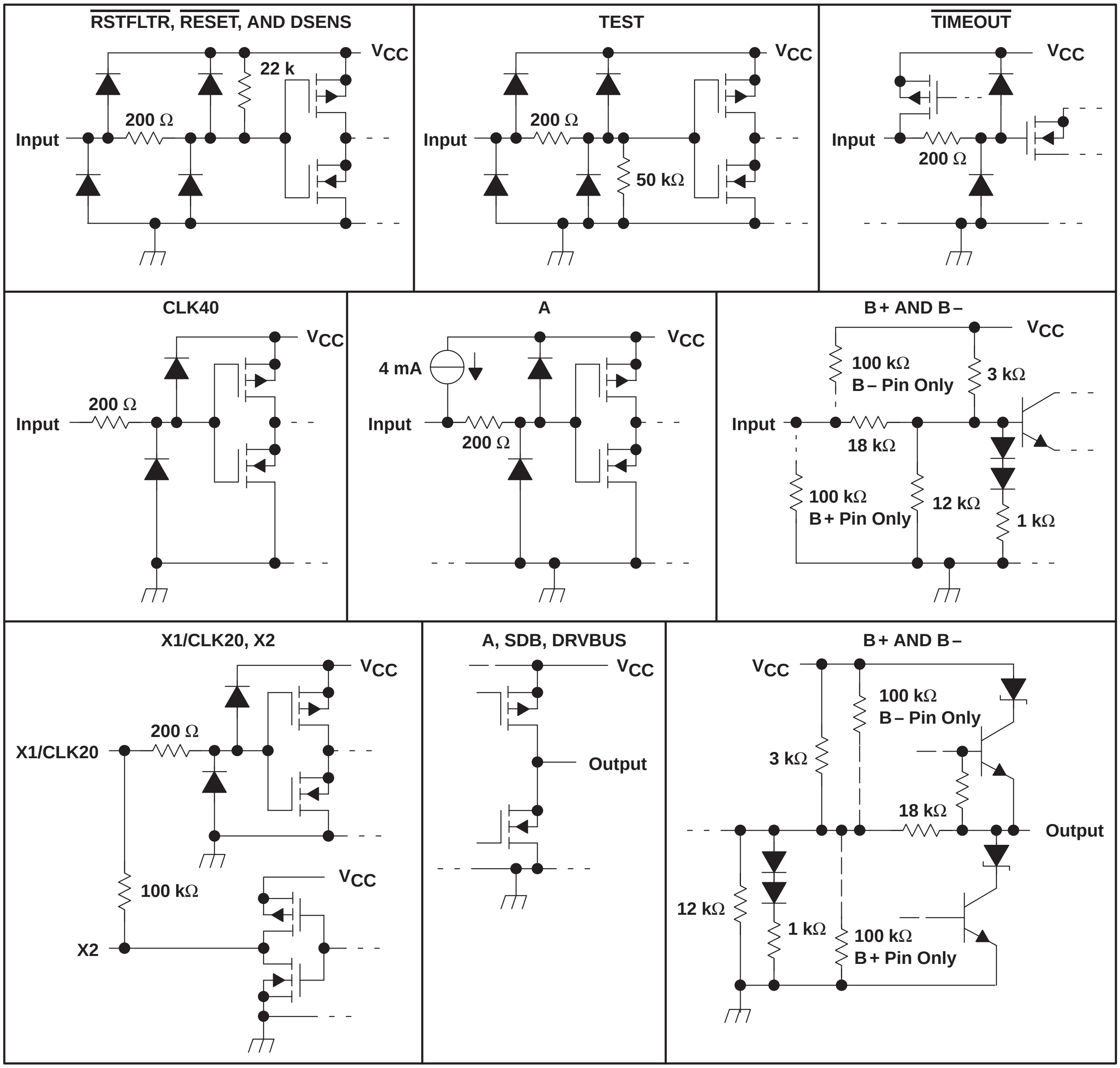
logic diagram (positive logic)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	Logic Level	I/O	Termination	DESCRIPTION
AACK–	8	TTL	I/O	Strong pullup	SCSI acknowledge (–ACK) signal to/from controller
AATN–	6	TTL	I/O	Strong pullup	SCSI attention (–ATN) signal to/from controller
ABSY–	25	TTL	I/O	Strong pullup	SCSI busy (–BSY) signal to/from the controller
AC/D–	11	TTL	I/O	Strong pullup	SCSI control/data (–C/D) signal to/from the controller
AI/O–	22	TTL	I/O	Strong pullup	SCSI input/output (–I/O) signal to/from the controller
AMSG–	21	TTL	I/O	Strong pullup	SCSI message (–MSG) signal to/from the controller
AREQ–	10	TTL	I/O	Strong pullup	SCSI request (–REQ) signal to/from controller
ARST–	27	TTL	I/O	Strong pullup	SCSI reset (–RST) signal to/from the controller
ASEL–	23	TTL	I/O	Strong pullup	SCSI select (–SEL) signal to/from the controller
BACK–	51	RS-485	I/O	Weak pullup	SCSI acknowledge (–ACK) signal to/from the bus
BACK+	50	RS-485	I/O	Weak pulldown	SCSI acknowledge (+ACK) signal to/from the bus
BATN–	53	RS-485	I/O	Weak pullup	SCSI attention (–ATN) signal to/from the bus
BATN+	52	RS-485	I/O	Weak pulldown	SCSI attention (+ATN) signal to/from the bus
BBSY–	31	RS-485	I/O	Weak pulldown	SCSI busy (–BSY) signal to/from the bus
BBSY+	32	RS-485	I/O	Weak pullup	SCSI busy (+BSY) signal to/from the bus
BC/D–	47	RS-485	I/O	Weak pullup	SCSI control/data (–C/D) signal to/from the bus
BC/D+	46	RS-485	I/O	Weak pulldown	SCSI control/data (+C/D) signal to/from the bus
BI/O–	36	RS-485	I/O	Weak pullup	SCSI input/output (–I/O) signal to/from the bus
BI/O+	35	RS-485	I/O	Weak pulldown	SCSI input/output (+I/O) signal to/from the bus
BMSG–	38	RS-485	I/O	Weak pullup	SCSI message (–MSG) signal to/from the bus
BMSG+	37	RS-485	I/O	Weak pulldown	SCSI message (+MSG) signal to/from the bus
BREQ–	49	RS-485	I/O	Weak pullup	SCSI request (–REQ) signal to/from the bus
BREQ+	48	RS-485	I/O	Weak pulldown	SCSI request (+REQ) signal to/from the bus
BRST–	29	RS-485	I/O	Weak pulldown	SCSI reset (–RST) signal to/from the bus
BRST+	30	RS-485	I/O	Weak pullup	SCSI reset (+RST) signal to/from the bus
BSEL–	33	RS-485	I/O	Weak pulldown	SCSI select (–SEL) signal to/from the bus
BSEL+	34	RS-485	I/O	Weak pullup	SCSI select (+SEL) signal to/from the bus
CLK40	4	CMOS	I	Strong pulldown	40-MHz clock input
DRVBUS	19	TTL	O	N/A	Driver bus. A high-level logic signal that indicates the SCSI bus is in one of the information transfer phases.
DSENS	3	TTL	I	Weak pullup	A low-level input initializes the internal latches and disables all drivers.
GND	5, 13–17, 40–44	N/A	N/A	N/A	Supply common
$\overline{\text{RESET}}$	2	TTL	I	Weak pullup	Reset. A low-level input initializes the internal latches and disables all drivers.
$\overline{\text{RSTFLTR}}$	1	TTL	I	Weak pullup	Reset filter. Filtered input from the SCSI bus for a system reset. $\overline{\text{RSTFLTR}}$ differs from $\overline{\text{RESET}}$ by keeping the ARST and BRST drivers enabled.
SDB	20	TTL	O	N/A	A high-level logic signal that indicates a differential to single-ended data flow.
TEST	7	TTL	I	Weak pulldown	Test. A high-level input that places the device in a test mode (see Table 1). It is grounded during normal operation.
$\overline{\text{TIMEOUT}}$	9	Analog	I/O	N/A	Time out. This signal connects to an external RC time constant for a time out during bus arbitration.
V_{CC}	12, 18, 39, 45	N/A	N/A	N/A	5-V supply voltage
X1/CLK20	55	CMOS	I	None	20-MHz crystal oscillator or clock input
X2	56	Analog	O	None	20-MHz crystal oscillator feedback

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . –0.3 V to 7V
Differential bus voltage range (B side) . . . . –15 V to 15 V
Signal-ended bus voltage range (A side and control) . . . . –0.3 V to 7 V
Continuous total power dissipation . . . . See Dissipation Rating Table
Electrostatic discharge: B side (see Note 2): Class 2, A: . . . . 2 kV
Class 2, B: . . . . 200 V
All terminals: Class 1, A: . . . . 500 V
Class 1, B: . . . . 200 V
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminals.
2. This absolute maximum rating is tested in accordance with MIL-STD-883C, Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DL	2500 mW	20 mW/°C	1600 mW

‡ This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	A side, DSENS, TEST, $\overline{\text{RESET}}$, AND $\overline{\text{RSTFLTR}}$	2			V
	CLK40 AND X1/CLK20	0.7 V_{CC}			
Low-level input voltage, V_{IL}	A side, DENS, TEST, $\overline{\text{RESET}}$, and $\overline{\text{RSTFLTR}}$			0.8	V
	CLK40 AND X1/CLK20			0.2 V_{CC}	
Input voltage at any bus terminal (separately or common-mode), V_I	B side			12	V
				–7	
Output voltage at any bus terminal (separately or common-mode), V_O	B side			12	V
				–7	
High-level output current, I_{OH}	B side			–60	mA
	A side, DRVBUS, SDB, $\overline{\text{TIMEOUT}}$			–16	
	X2			– 4	
Low-level output current, I_{OL}	B side			60	mA
	A side, DRVBUS, and SDB			16	
	X2			4	mA
Clock frequency, f_{CLK}	CLK20		20		MHz
	CLK40		40		
Operating case temperature, T_C		0		125	°C
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{OD(H)}$	Driver differential high-level output voltage	B side except BBSY, BRST, and BSEL	See Figure 1	1	1.8		V
$V_{OD(L)}$	Driver differential low-level output voltage	B side	See Figure 1	–1	– 2.2		V
V_{OH}	High-level output voltage	AACK–, AATN–, AC/D–, AI/O–, AMSG–, AREQ–	V_{ID} = –200 mA, I_{OH} = –16 mA	2.5	4.3		V
		DRVBUS, SDB	I_{OH} = –16 mA	2.5	4.4		
		$\overline{\text{TIMEOUT}}$	Test and $\overline{\text{RESET}}$ at 0.8 V, All others open, I_{OH} = –16 mA	2.5	4.5		
		B side			3.4		
		X2	I_{OH} = - 4 mA	3.2			
V_{OL}	Low-level output voltage	DRVBUS, SDB	I_{OL} = 16 mA			0.8	V
		A side	V_{ID} = 200 mV, I_{OL} =16 mA			0.8	
		B side			1.6		
		X2	I_{OL} = 4 mA			0.8	
V_{IT+}	Receiver positive-going input threshold voltage	B side	I_{OH} = –16 mA, See Figure 2			0.2	V
		$\overline{\text{TIMEOUT}}$			2.6		
V_{IT-}	Receiver negative-going input threshold voltage	B side	I_{OL} = 16 mA, See Figure 2	–0.2			V
		$\overline{\text{TIMEOUT}}$		0.32 V_{CC}		0.4 V_{CC}	
V_{hys}	Receiver input hysteresis ($V_{IT+} - V_{IT-}$)	B side			45		mV
		$\overline{\text{TIMEOUT}}$		0.5			V
I_I	Bus input current	B side	V_I = 12 V, V_{CC} = 5 V, All other inputs at 0 V		0.6	1	mA
			V_I = 12 V, V_{CC} = 0, All other inputs at 0 V		0.7	1	
			V_I = –7 V, V_{CC} = 5 V, All other inputs at 0 V		–0.5	–0.8	
			V_I = –7 V, V_{CC} = 0, All other inputs at 0 V		–0.4	–0.8	
I_{IH}	High-level input current	A side	V_{IH} = 2 V	–2.9	–6	–8	mA
		DSENS, $\overline{\text{RESET}}$, RSTFLTR			–60	–100	µA
		CLK40, X1/CLK20				±20	
		TEST				100	
		$\overline{\text{TIMEOUT}}$	TEST at 2 V, A side and other control inputs at 0.8 V, B side open, V_{IH} = 2 V			±1	
I_{IL}	Low-level input current	A side	V_{IH} = 0.8 V		–6	–8	mA
		DSENS, $\overline{\text{RESET}}$, RSTFLTR				–100	µA
		CLK40, TEST, X1/CLK20				±20	
		$\overline{\text{TIMEOUT}}$	TEST at 0.8 V, A side and other control inputs at 0.8 V, B side open, V_{IH} = 2 V			±1	
I_{OS}	Short circuit output current	B side	V_O = 5 V and 0 V			±250	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (Continued)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}	Supply current	Disabled	$\overline{RESET}$ at 0.8 V, All others open		27	36	mA
		All A-side to B-side channels enabled	TEST and $\overline{RSTFLTR}$ at 2 V $\overline{RESET}$ at 0.8 V, All other inputs open, no load		72	94	
		All B-side to A-side channels enabled	TEST at 2 V, $\overline{RESET}$ and RSTFLTR at 0.8 V, All other inputs open, No load		38	50	
C_o	Bus output capacitance		B side to GND, $V_I = 0.6 \sin(2\pi\ 10^6\ t) + 1.5$ V		19	21	pF
C_{pd}	Power dissipation capacitance (see Note 3)		B side to A side, one channel		100		pF
			A side to B side, one channel		450		pF

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.

NOTE 3: C_{pd} determines the no-load dynamic current consumption, $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$ (I_{CC} depends upon the output states and load circuits and is not necessarily the same I_{CC} as specified in the electrical tables).

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

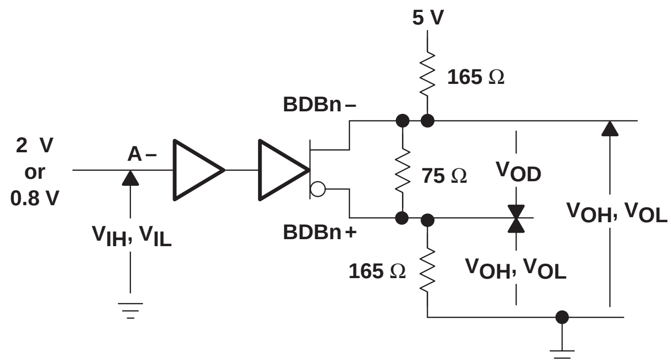
PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{d1}, t_{d2}	Delay time, A to B, high- to low-level or low- to high-level output	AATN– AC/D– AI/O– AMSG–	BATN± BC/D± BI/O± BMSG±	See Figure 3	7.6		26.6	ns
		AACK– AREQ–	BACK± BREQ±		8.5		25.3	
				V_{CC} = 5 V, T_A = 25°C	10		18	
				V_{CC} = 5 V, T_A = 70°C	12.5		20.5	
$t_{sk(lim)}$	Skew limit	AACK– AREQ–	BACK± BREQ±	See Note 4			8	ns
$t_{sk(p)}$	Pulse skew			See Note 5			6	ns
t_{d3}, t_{d4}	Delay time, B to A, high- to low-level or low- to high-level output	BATN± BC/D± BI/O± BMSG±	AATN– AC/D– AI/O– AMSG–	See Figure 4	21.5		36.2	ns
		BACK± BREQ±	AACK– AREQ–		21.5		36.2	
				V_{CC} = 5 V, T_A = 25°C	23.6		32.6	
				V_{CC} = 5 V, T_A = 70°C	24.4		33.4	
$t_{sk(lim)}$	Skew limit	BACK± BREQ±	AACK– AREQ–	See Note 4			9	ns
$t_{sk(p)}$	Pulse skew			See Note 5			6	ns
t_{PHL}	Delay time, high- to low-level	TIMEOUT	DRVBUS	See Figure 5			200	ns
t_{PLH}	Delay time, low- to high-level						200	ns
t_{dis}	Disable time	ABSY–	BBSY±	See Figure 6			200	ns
		ARST–	BRST±				200	
		ASEL–	BSEL±				200	
t_{en}	Enable time	ABSY–	BBSY±	See Figure 6			40	ns
		ARST–	BRST±				55	
		ASEL–	BSEL±				39	
t_{dis1}	Disable time	BRST±	ARST–	See Figure 7			93	ns
t_{dis2}	Disable time	BSEL±	ASEL–				55	ns
t_{dis3}	Disable time	BBSY±	ABSY–				60	ns
t_{en1}	Enable time	BRST±	ARST–				63	ns
t_{en2}	Enable time	BSEL±	ASEL–				45	ns
t_{en3}	Enable time	BBSY±	ABSY–				45	ns
t_{en4}	Enable time	BSEL±	ASEL–				92	ns

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.

NOTES: 4. This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions and to any two devices.

5. Pulse skew is the difference between the high-to-low and low-to-high propagation delay times of any single channel.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns PRR ≤ 1 MHz, 45% < duty cycle < 50%, $Z_O = 50\ \Omega$.
B. Resistance values are with a tolerance of 5%.
C. All input voltage levels are held to within 0.01 V.

Figure 1. Differential Driver V_{OD}, V_{OH}, and V_{OL} Test Circuit

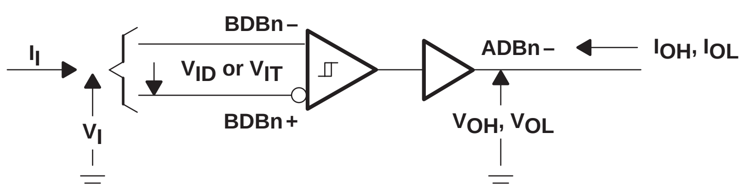
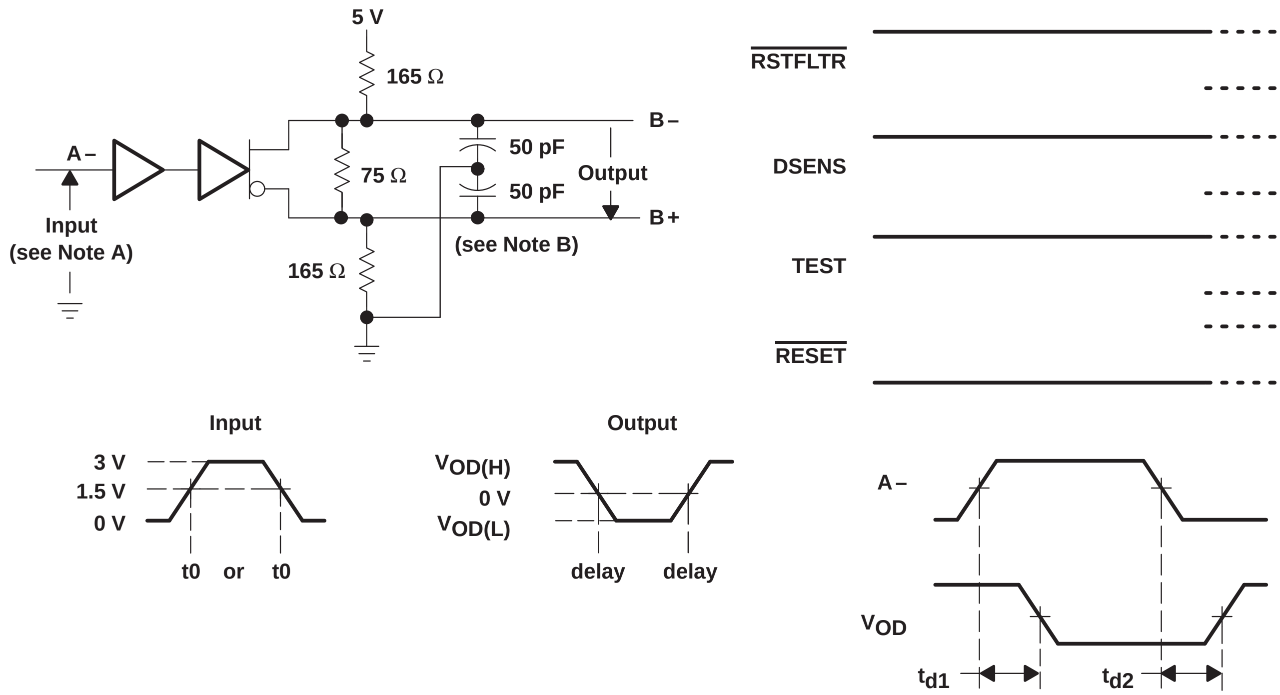


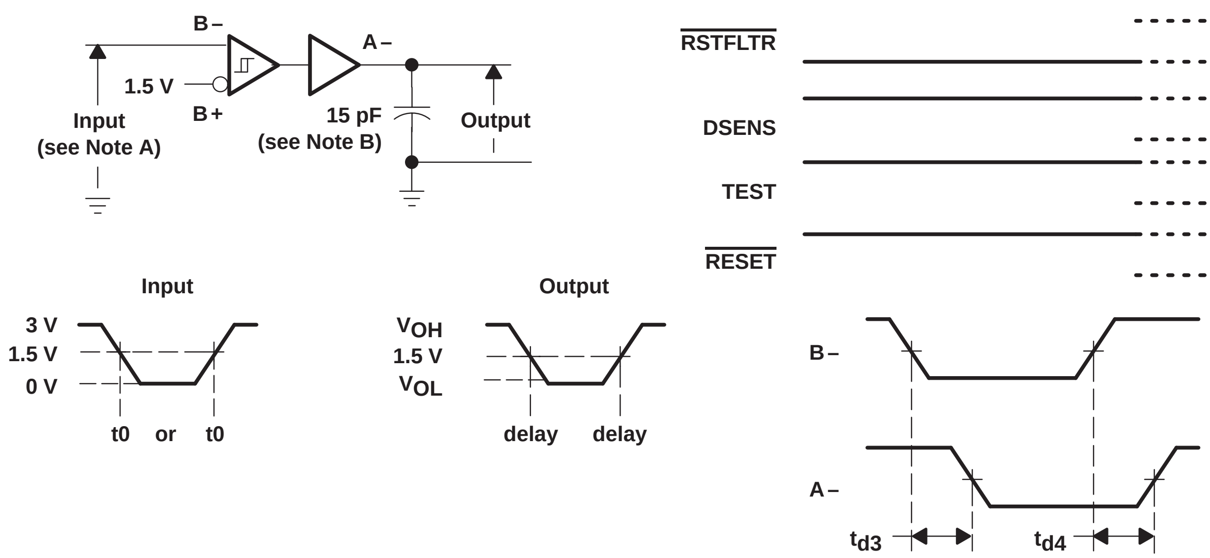
Figure 2. Single-Ended Driver V_{OD}, V_{OH}, and V_{OL} Test Circuit

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 6$ ns, $t_f \le 6$ ns PRR ≤ 1 MHz, 45% < duty cycle < 50%, $Z_O = 50\ \Omega$.
B. Resistance values are with a tolerance of ±5%.
C. All input voltage levels are held to within 0.01 V.

Figure 3. A-Side to B-Side Propagation Delay Time Test Circuit and Timing Definitions



NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 6$ ns, $t_f \le 6$ ns PRR ≤ 1 MHz, 45% < duty cycle < 50%, $Z_O = 50\ \Omega$.
B. Resistance values are with a tolerance of ±5%.
C. All input voltage levels are held to within 0.01 V.

Figure 4. B-Side to A-Side Propagation Delay Time Test Circuit and Timing Definitions

PARAMETER MEASUREMENT INFORMATION

Table 1. Output Test Enabling (No Clock Input)

SIGNAL	BUS		CONTROL INPUT(s)						
	INPUT(s)	OUTPUT	TEST	$\overline{\text{RSTFLTR}}$	$\overline{\text{RESET}}$	BBSY–	BBSY+	ABSY–	DSENS
ATN, ACK, MSG, C/D, REQ, I/O	A	B	H	H	L				
ATN, ACK, MSG, C/D, REQ, I/O	B	A	H	L	L				
RST	A	B			L—>H	H	L	H	H
RST	B	A			L—>H	H	L	H	H
SEL, BSY	B	A	L	H	L—>H				H
SEL, BSY		B	H	H	L				
$\overline{\text{TIMEOUT}}$	N/A	H	L		L				
DRVBUS†	BBSY–/ BBSY+, $\overline{\text{BSEL–/BSEL+}}$, $\overline{\text{TIMEOUT}}$	DRVBUS	H	L	L				
$\overline{\text{TIMEOUT}}$	N/A	Z	H		L				

† For these conditions, DRVBUS = $\overline{\text{BSEL}}$ or BBSY and $\overline{\text{TIMEOUT}}$ together.

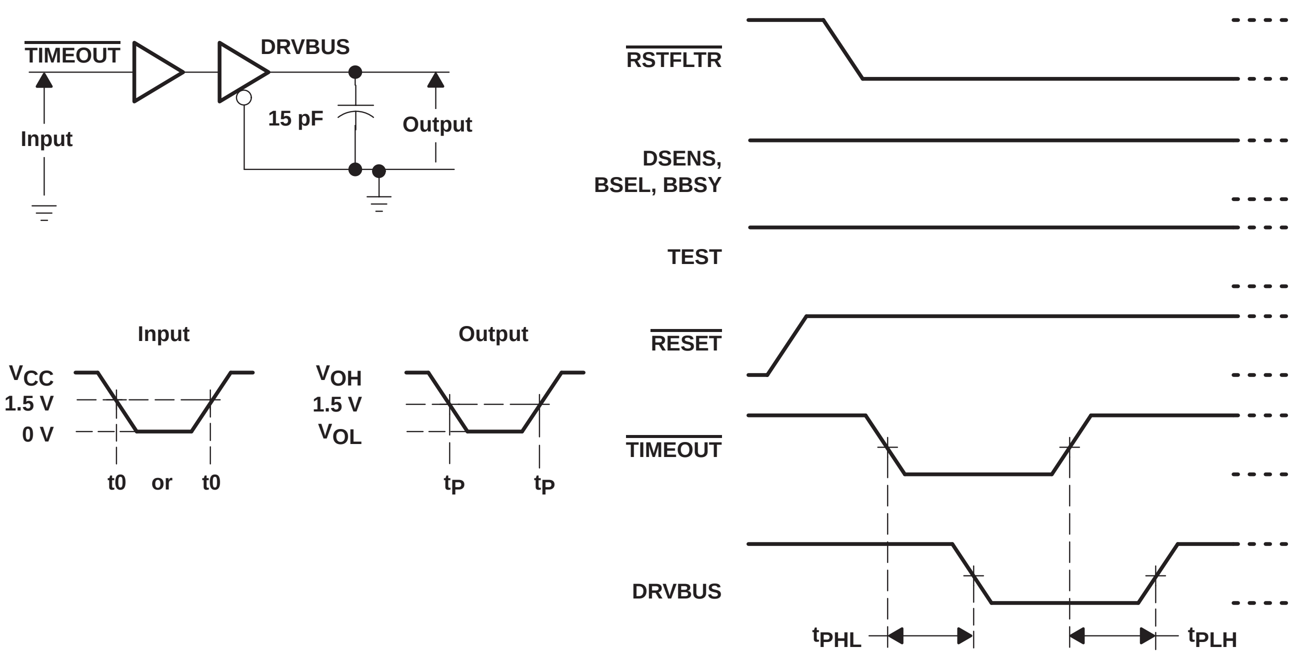
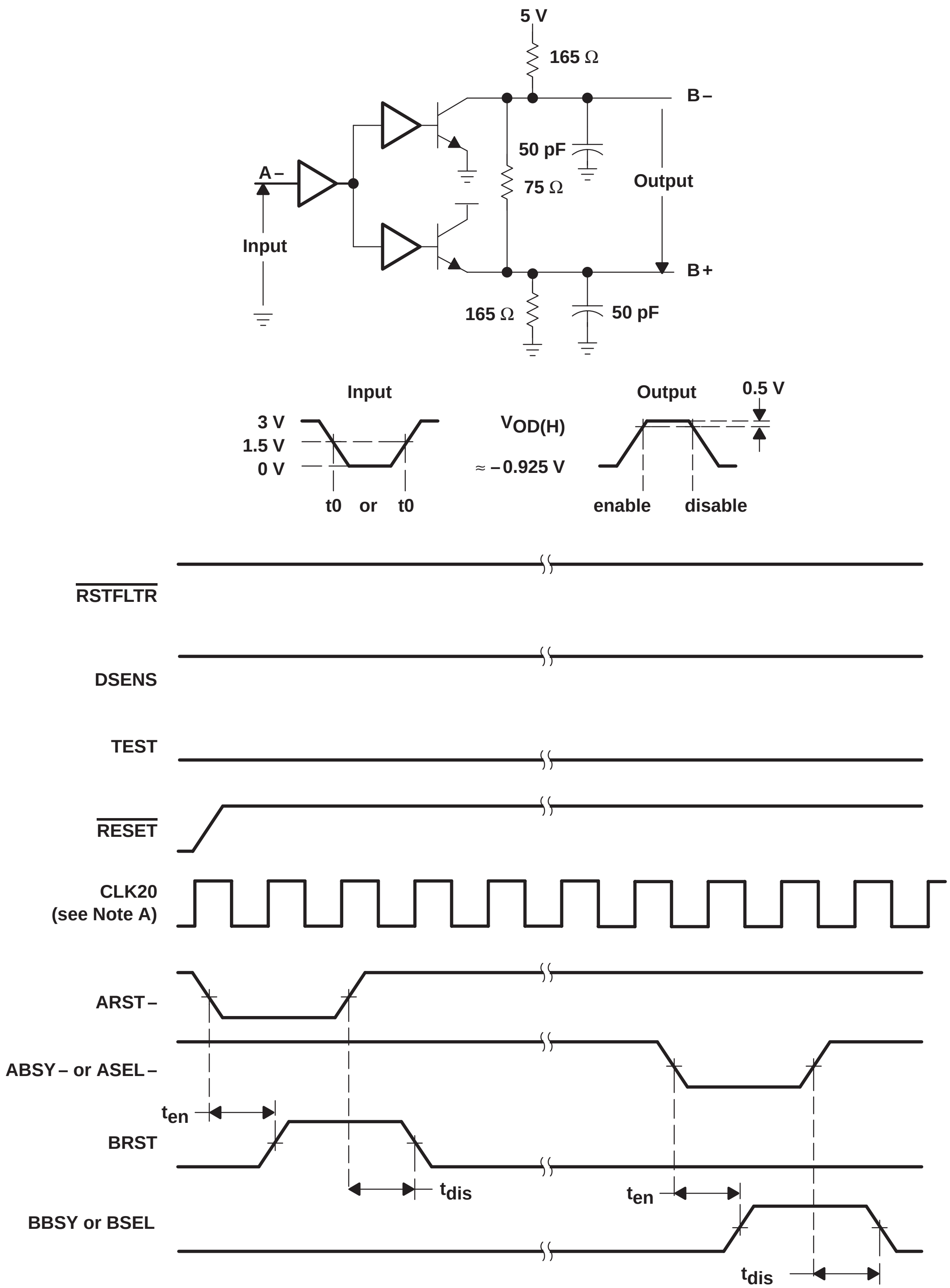


Figure 5. $\overline{\text{TIMEOUT}}$ to DRVBUS Delay Time Test Circuit and Timing Definitions

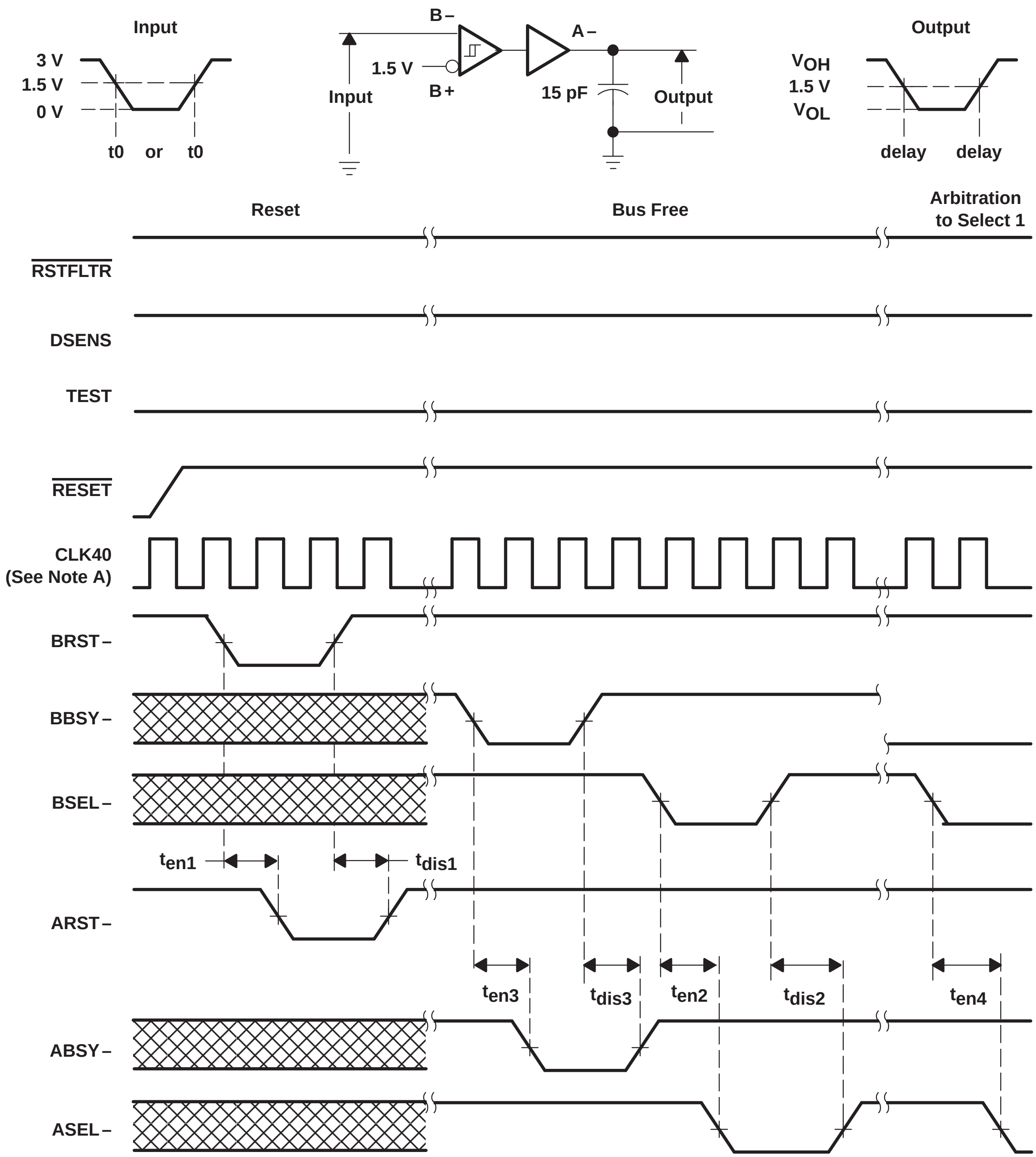
PARAMETER MEASUREMENT INFORMATION



NOTE A: These are asynchronous events and do not necessarily align with clock edges.

Figure 6. A-Side to B-Side Enable and Disable Delay Time Test Circuit and Timing Definitions

PARAMETER MEASUREMENT INFORMATION



NOTE A: These are asynchronous events and do not necessarily align with clock edges.

Figure 7. B-Side to A-Side Enable and Disable Delay Time Test Circuit and Timing Definitions

APPLICATION INFORMATION

To correctly set the direction of the SCSI bus signals, the SN75LBC970A must follow the activity on the bus. An asynchronous, 5-state controller watches the state of all the bus control signals, sets the direction of each control signal as needed, and generates the DRVBUS and SDB outputs to control one or two external SN75LBC971A SCSI differential converter-data devices. The controller never generates the data driven on a bus signal; it only enables the drivers. The clock input implements a 400-ns timer that is not part of the controller itself. Controller-state transitions occur immediately when all the transition conditions are met. Note that the frequency of the supplied clock, either 20 MHz or 40 MHz, must be correct in order to meet the SCSI specifications.

As shown in Figure 8, after reset, the controller begins in the bus free state. In case the controller was attached to an active differential bus, it waits for the SCSI bus free condition, defined as when BBSY and BSEL are deasserted for 400 ns. While waiting for the SCSI bus free condition, the state of BBSY and BSEL passes through to the A side. The A side bus device cannot take part in bus activity during this condition before the SCSI bus free condition. Once SCSI bus free is detected, the SCSI arbitration state is entered. Both ABSY and BBSY are enabled; thus when either signal asserts, both drivers turn on and both signals remain asserted until this state is left. Normally the SCSI arbitration state ends after the winner of arbitration asserts BSEL. This would cause the controller to go to the select 1 state. However, when BSEL is not asserted, a timeout would eventually be detected and cause a reset of the controller. In the select 1 state, two latches are open, DSEL_LATCH and RESEL_LATCH. The first latch captures the state of BSEL so that following states can determine whether the arbitration winner was on the A side or B side.

APPLICATION INFORMATION

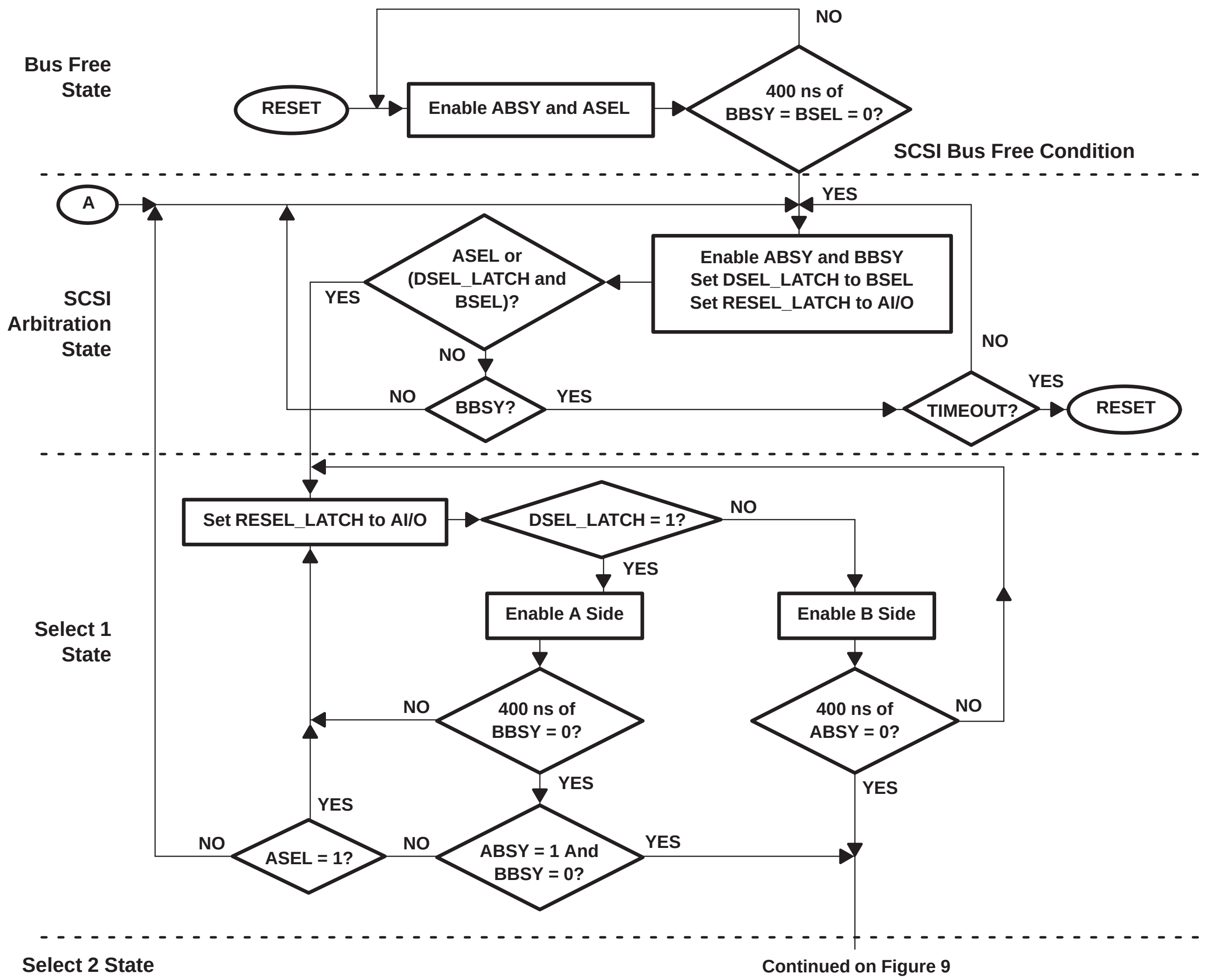


Figure 8. Bus Free, SCSI Arbitration, and Select 1 State Flow Chart

The second latch captures the state of AI/O. This is true during a reselection phase but not during the selection phase. When the bus is in the selection or reselection phase, the controller enters the select 1 state. There are three possible flows depending on bus events. The first flow is that the SCSI controller on the A side won the arbitration and asserted ASEL. In this event DSEL_LATCH would not be set. The controller passes all signals to the B side and waits for ABSY to deassert for 400 ns, indicating that the A side controller is selecting or reselecting a device on the B side. The object of the A side controller must be on the B side since only one device is allowed on the A side.

The second possible flow is that DSEL_LATCH is set, indicating that the arbitration winner is on the B side, and the winner is selecting or reselecting the device on the A side. The controller passes all signals to the A side and waits for BBSY to deassert for 400 ns. When the A side controller responds by asserting ABSY, the controller detects ABSY asserted and BBSY deasserts and goes to the select 2 state.

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The third possible flow is that a device on the B side won the arbitration and is selecting or reselecting another device on the B side. DSEL_LATCH is set, and 400 ns of BBSY is asserted first by the object of the selection or reselection. Since ASEL is still asserted, the controller remains in the select 1 state throughout the selection or reselection. If the BBSY deassertion is missed by the timer, again the controller remains in the select 1 state. Once the transfer state is entered, BBSY is asserted and BSEL is dropped. This again returns the controller to a select 1 state. At the end of the transfer both BBSY and BSEL are deasserted. After the timer limit is reached, the controller goes to the arbitration state for the next bus arbitration.

The controller enters the select 2 state (see Figure 9) during the selection or reselection phases when the initiator and terminator are on the opposite side of SDCC. In this state the RESEL_LATCH is closed, capturing the value of the I/O. When RESEL_LATCH is one, reselection is indicated. When RESEL_LATCH equals zero, a selection is indicated. RESEL_LATCH, along with the DSEL_LATCH, now defines which side the initiator is on and therefore what direction to establish for all the bus signals. The target must be on the other side; if both target and initiator were on the B side, the select 2 state would never be entered.

When the RESEL_LATCH is zero, indicating a selection, the connection is not made. When DSEL_LATCH is one, the initiator is on the B side and the control lines it drives have their A side drivers enabled. These terminals are the initiator group of ACK and ATN along with SEL. The other terminals are driven by the target and have the B side drivers enabled. They are the target group of REQ, MSG, C/D, and I/O, along with BSY. When DSEL_LATCH is zero the connection is reversed. Since transfer states are not started, DRVBUS is set to 1, indicating that the data transceiver chips should not take their direction control from SDB and should be actively negated. SDB is generated from I/O and is the bus signal that determines data transfer direction. In this case it indicates the selection phase, the controller immediately transfers to the transfer state, where exactly the same actions are done.

When the RESEL_LATCH is 1 indicating a reselection, there is one or more actions before information states can be entered. When the target reselects the initiator, the initiator responds by asserting BSY. Once the connection is made, the assertion of BSY must be changed over to the target, and the controller must reverse the BSY driver direction. It does this when SEL deasserts by transferring to the transfer state where the BSY direction is reversed. In the select 2 state all the control line directions are set as appropriate, except that DRVBUS is not yet asserted. In the transfer state DRBVUS is set as well.

The controller remains in the transfer state during all other SCSI states. When a bus free state is detected, it goes back to the arbitration state to wait for the next activity. Note that after BBSY and BSEL deassert, the controller continues to actively drive the control lines and the data lines through DRVBUS until 400 ns of continuous deassertion is detected. The drivers are turned off only when the state change occurs.

Figure 10 shows a typical system configuration. The timeout function used in the arbitration state is implemented with a resistor and capacitor connected to the $\overline{\text{TIMEOUT}}$ terminal. During reset and whenever the timer is not in use, the terminal is driven to V_{CC}. The timer starts when the driver turns off, allowing the capacitor to charge and the $\overline{\text{TIMEOUT}}$ terminal to drop to ground. When V_{IT-} is reached, the driver turns on, discharging the capacitor and returning $\overline{\text{TIMEOUT}}$ to V_{CC}. A timeout event is declared after the driver turns back on and $\overline{\text{TIMEOUT}}$ exceeds V_{IT+}.

RST can be asserted on either the A or B side, and is driven to the other side. The drive to the other side is controlled by a bidirectional latch. When one side asserts, the other side is asserted and a latch is set to that direction. When the first side deasserts, the driver turns off, but the direction is held until both sides are deasserted. Only then can the direction change.

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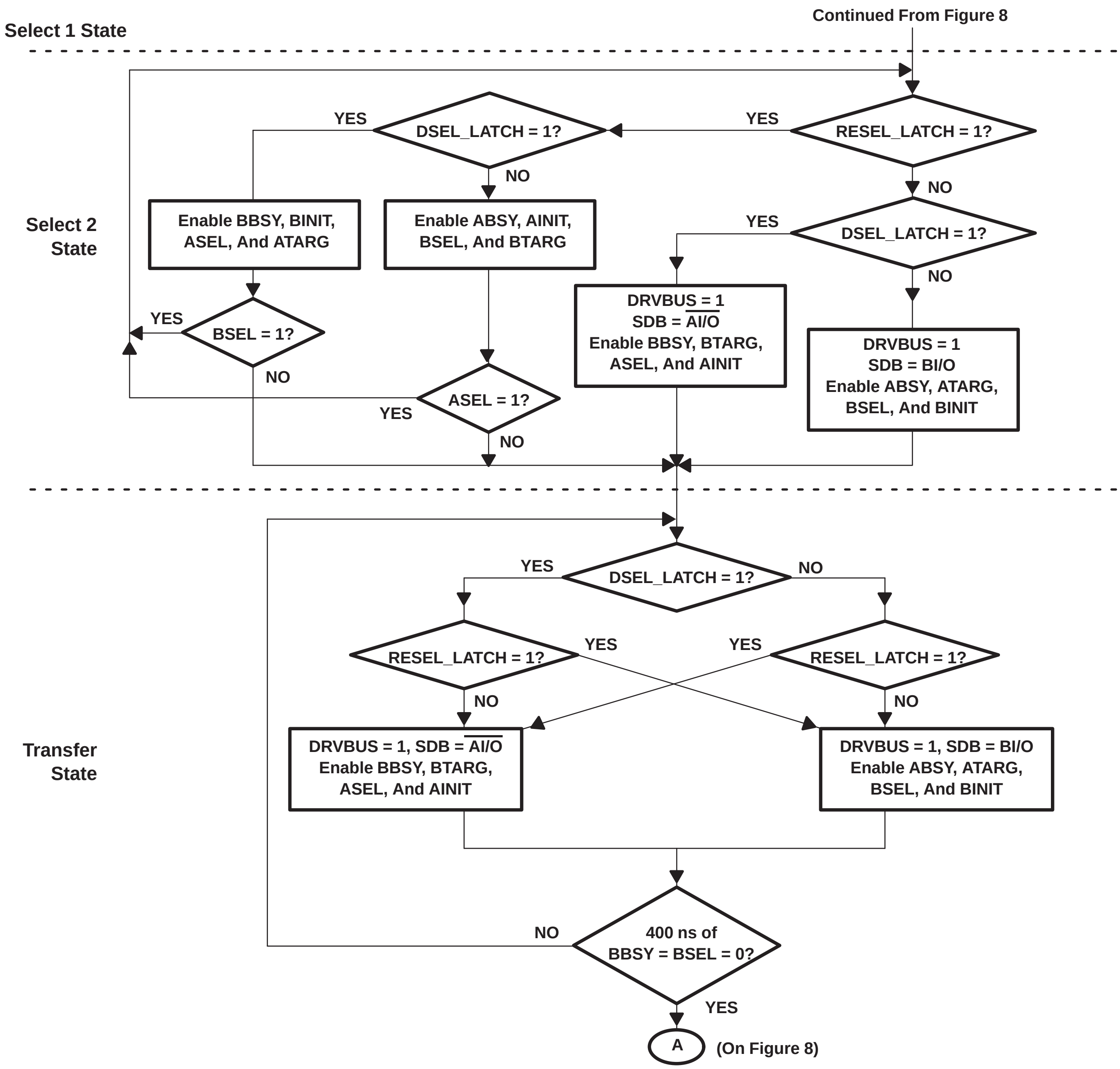
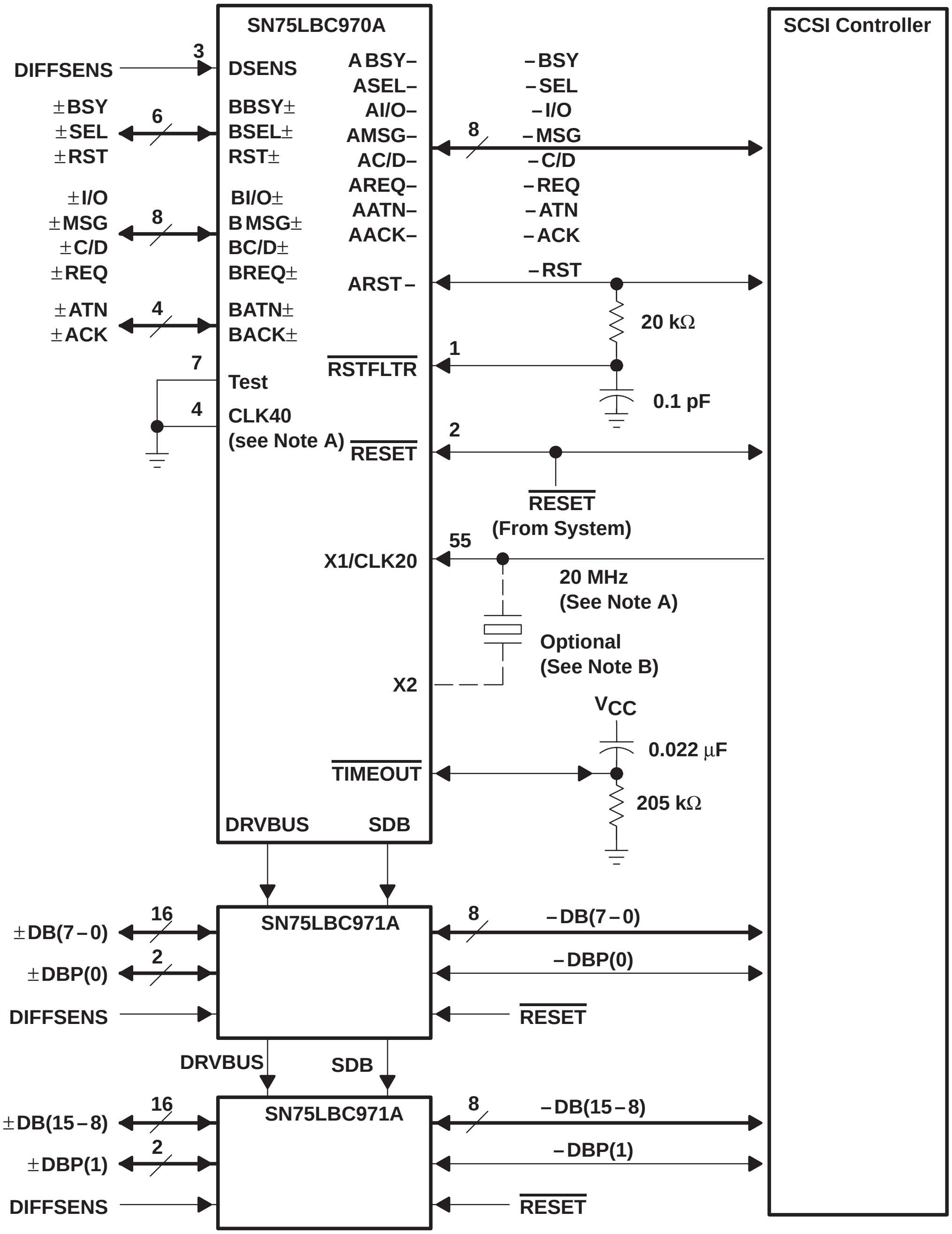


Figure 9. SCSI Select 1, Select 2, and Transfer State Flow Chart

APPLICATION INFORMATION

The SCSI bus signal RST does not directly clear SDCC internal logic. Instead, the RSTFLTR terminal can be connected as ARST– so that a bus reset clears SDCC. RSTFLTR clears the internal controller but does not clear the RST bidirectional latch. By connecting these terminals externally through a RC filter as shown in Figure 8, noise pulses on the bus may be filtered as recommended by the SCSI-2 specification.



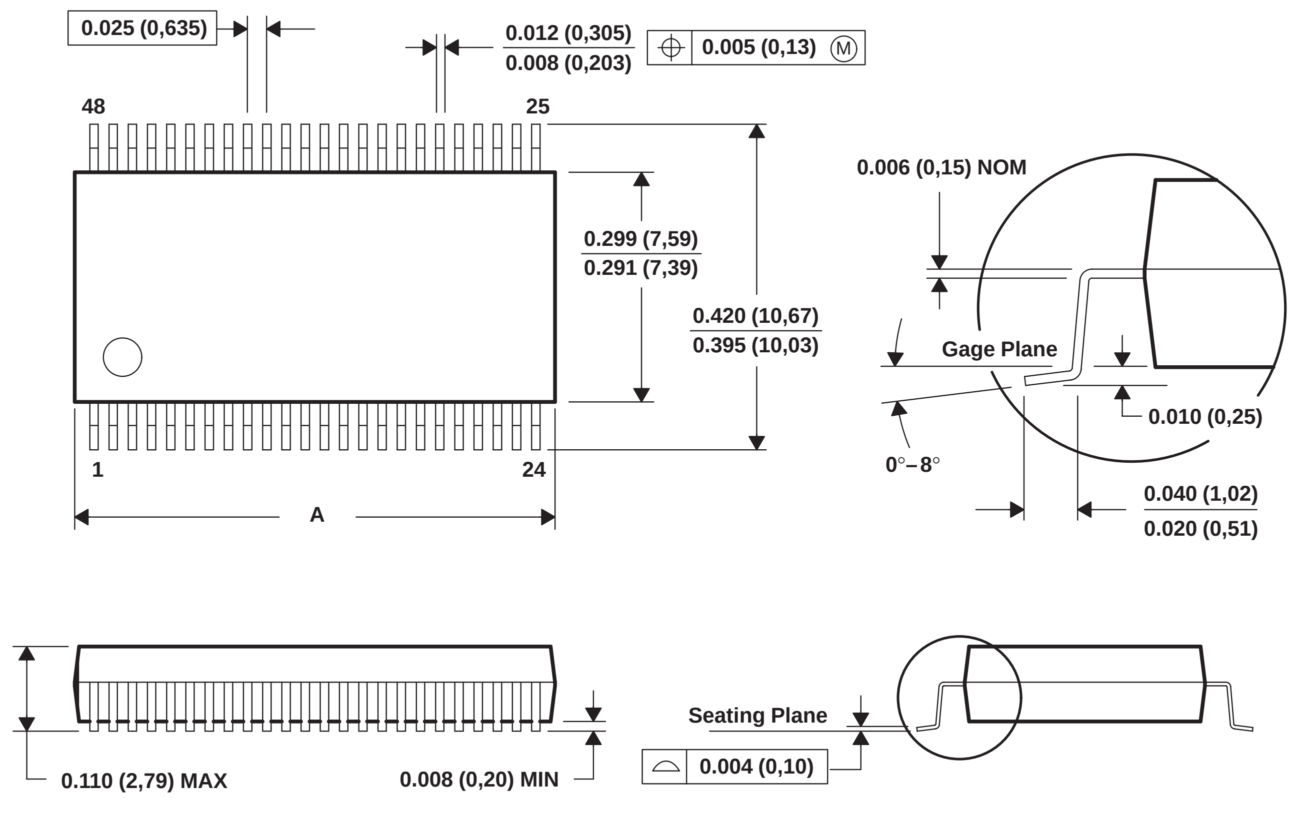
NOTES: A. When using the 40 MHz clock input, X1 must be connected to V_{CC}.
B. The oscillator cell of the SN75LBC970A is for a series-resonant crystal and needs approximately 10 pF (including fixture capacitance) from X1 and X2 to ground in order to function.

Figure 10. Typical Application of the SN75LBC970A and SN75LBC971A

MECHANICAL INFORMATION

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48-PIN SHOWN



DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/D 08/97

NOTES: D. All linear dimensions are in inches (millimeters).
E. This drawing is subject to change without notice.
F. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
G. Falls within JEDEC MO-118