- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation**

- **$I_{off}$ and Power-Up 3-State Support Hot Insertion**

- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**

- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V $V_{CC}$)**

- **Support Unregulated Battery Operation Down to 2.7 V**

- **Typical $V_{OLP}$ (Output Ground Bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**

- **Latch-Up Performance Exceeds 500 mA Per JESD 17**

- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**

- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Thin Very Small-Outline (DGV) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (JT) DIPs**

**SN54LVTH646 . . . JT OR W PACKAGE**
**SN74LVTH646 . . . DB, DGV, DW, OR PW PACKAGE**
**(TOP VIEW)**

| | | |
|---|---|---|
| CLKAB | 1 | 24 | $V_{CC}$ |
| SAB | 2 | 23 | CLKBA |
| DIR | 3 | 22 | SBA |
| A1 | 4 | 21 | $\overline{OE}$ |
| A2 | 5 | 20 | B1 |
| A3 | 6 | 19 | B2 |
| A4 | 7 | 18 | B3 |
| A5 | 8 | 17 | B4 |
| A6 | 9 | 16 | B5 |
| A7 | 10 | 15 | B6 |
| A8 | 11 | 14 | B7 |
| GND | 12 | 13 | B8 |

**SN54LVTH646 . . . FK PACKAGE**
**(TOP VIEW)**

Top pins (left to right): DIR (4), SAB (3), CLKAB (2), NC (1), $V_{CC}$ (28), CLKBA (27), SBA (26)

Left pins: A1 (5), A2 (6), A3 (7), NC (8), A4 (9), A5 (10), A6 (11)

Right pins: $\overline{OE}$ (25), B1 (24), B2 (23), NC (22), B3 (21), B4 (20), B5 (19)

Bottom pins (left to right): A7 (12), A8 (13), GND (14), NC (15), B8 (16), B7 (17), B6 (18)

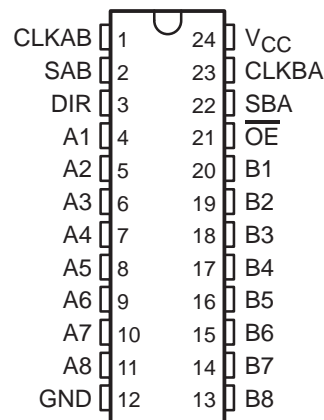NC – No internal connection

## description

These bus transceivers and registers are designed specifically for low-voltage (3.3-V) $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH646 devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH646.
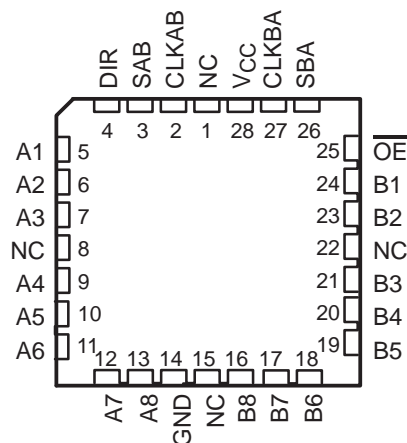
Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data can be stored in one register and/or B data can be stored in the other register.

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**TEXAS INSTRUMENTS**

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## description (continued)

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When $V_{CC}$ is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using $I_{off}$ and power-up 3-state. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54LVTH646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH646 is characterized for operation from –40°C to 85°C.
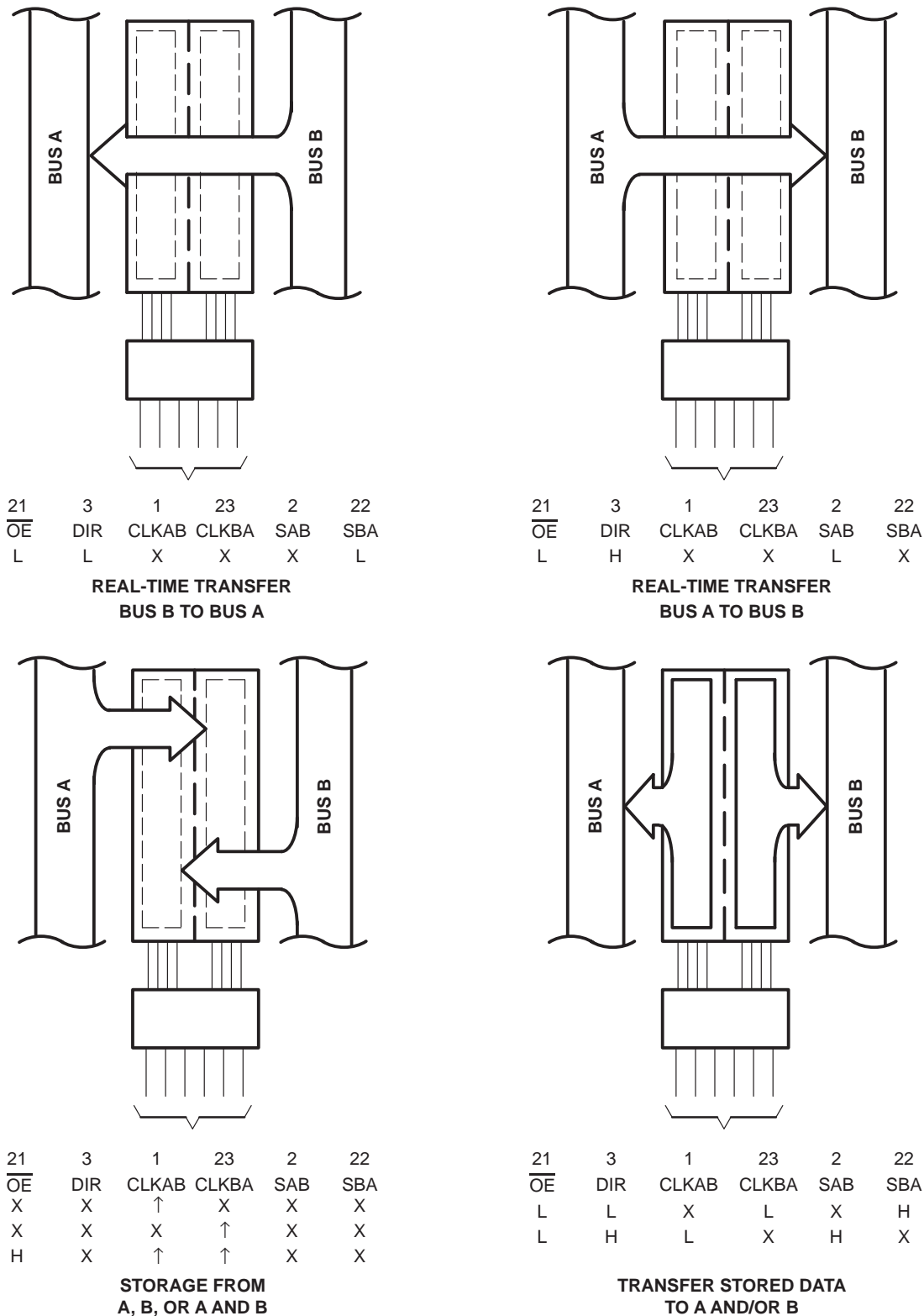
**FUNCTION TABLE**

| INPUTS | | | | | | DATA I/Os | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA | A1–A8 | B1–B8 | |
| X | X | ↑ | X | X | X | Input | Unspecified† | Store A, B unspecified† |
| X | X | X | ↑ | X | X | Unspecified† | Input | Store B, A unspecified† |
| H | X | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| H | X | H or L | H or L | X | X | Input disabled | Input disabled | Isolation, hold storage |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B data to A bus |
| L | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| L | H | H or L | X | H | X | Input | Output | Stored A data to B bus |

† The data-output functions can be enabled or disabled by various signals at $\overline{OE}$ and DIR. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

| 21 | 3 | 1 | 23 | 2 | 22 |
|----|----|----|----|----|----|
| $\overline{\text{OE}}$ | DIR | CLKAB | CLKBA | SAB | SBA |
| L | L | X | X | X | L |

**REAL-TIME TRANSFER**
**BUS B TO BUS A**

| 21 | 3 | 1 | 23 | 2 | 22 |
|----|----|----|----|----|----|
| $\overline{\text{OE}}$ | DIR | CLKAB | CLKBA | SAB | SBA |
| L | H | X | X | L | X |

**REAL-TIME TRANSFER**
**BUS A TO BUS B**

| 21 | 3 | 1 | 23 | 2 | 22 |
|----|----|----|----|----|----|
| $\overline{\text{OE}}$ | DIR | CLKAB | CLKBA | SAB | SBA |
| X | X | ↑ | X | X | X |
| X | X | X | ↑ | X | X |
| H | X | ↑ | ↑ | X | X |

**STORAGE FROM**
**A, B, OR A AND B**

| 21 | 3 | 1 | 23 | 2 | 22 |
|----|----|----|----|----|----|
| $\overline{\text{OE}}$ | DIR | CLKAB | CLKBA | SAB | SBA |
| L | L | X | L | X | H |
| L | H | L | X | H | X |

**TRANSFER STORED DATA**
**TO A AND/OR B**

Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

**Figure 1. Bus-Management Functions**
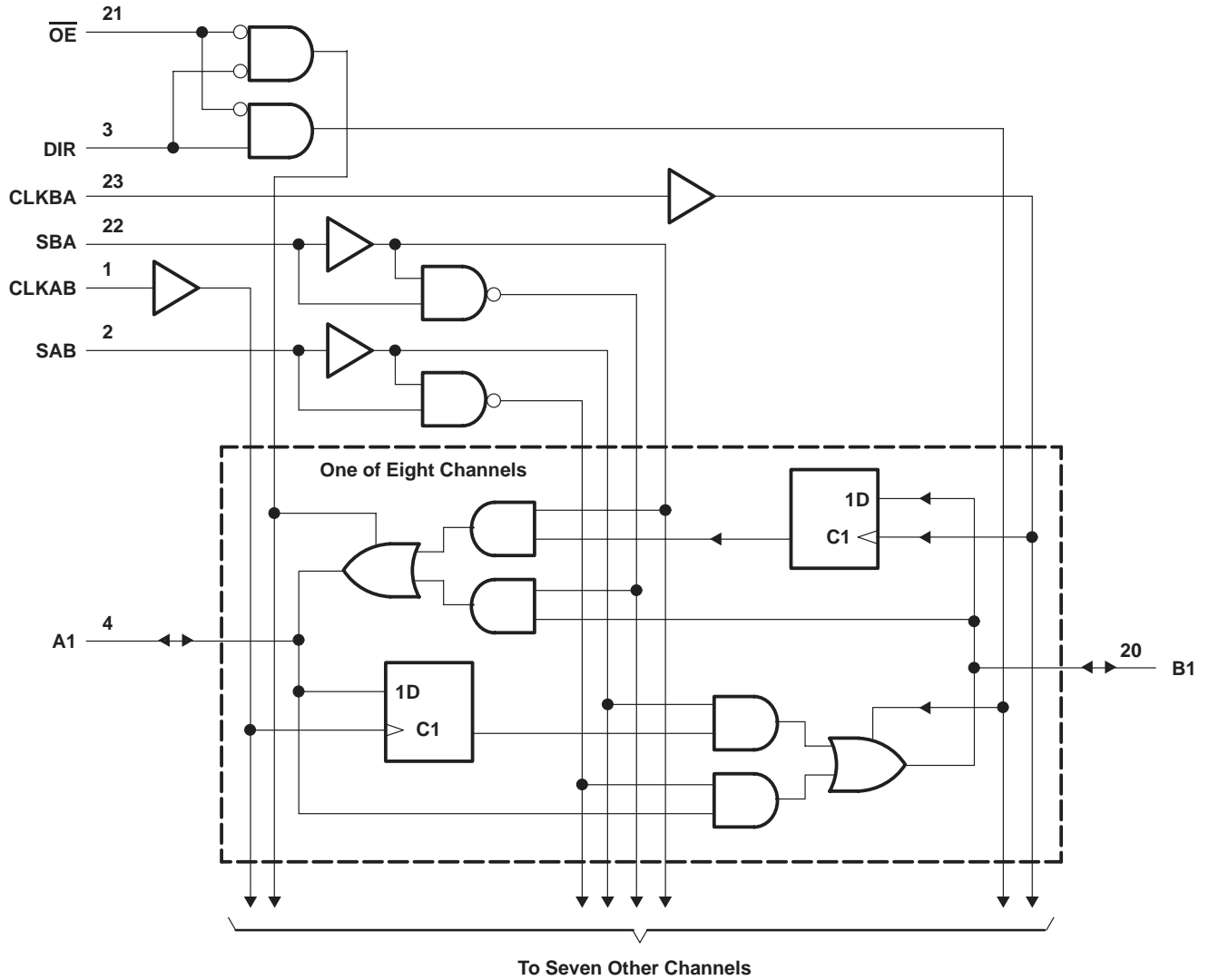
## logic symbol†
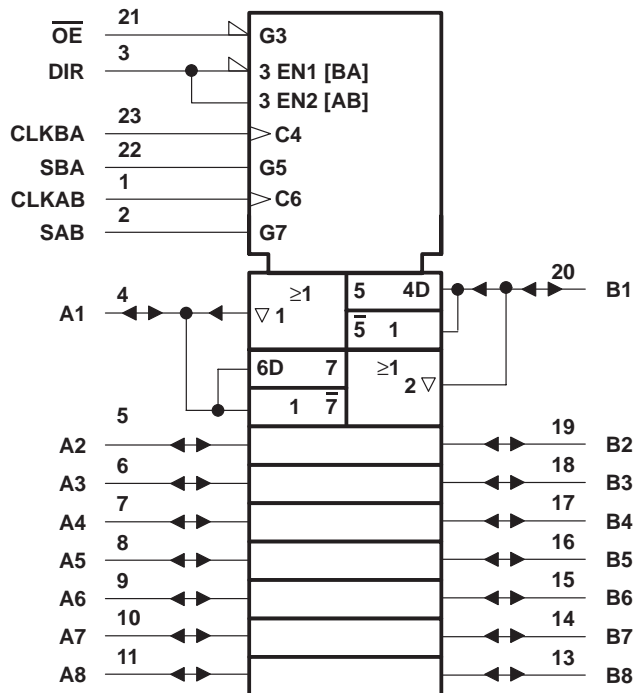


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

## logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ............................................................... –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) ..................................................... –0.5 V to 7 V
Voltage range applied to any output in the high-impedance
   or power-off state, $V_O$ (see Note 1) .................................................. –0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1) ............. –0.5 V to $V_{CC}$ + 0.5 V
Current into any output in the low state, $I_O$:  SN54LVTH646 ..................................... 96 mA
                                               SN74LVTH646 ..................................... 128 mA
Current into any output in the high state, $I_O$ (see Note 2):  SN54LVTH646 ....................... 48 mA
                                                              SN74LVTH646 ....................... 64 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) ......................................................... –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) ....................................................... –50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3):  DB package ................................ 104°C/W
                                                       DGV package ............................... 139°C/W
                                                       DW package ................................ 81°C/W
                                                       PW package ................................ 120°C/W
Storage temperature range, $T_{stg}$ ............................................................ –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:  1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
        2. This current flows only when the output is in the high state and $V_O$ > $V_{CC}$.
        3. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 4)

|          |                                 |                 | SN54LVTH646 | | SN74LVTH646 | | UNIT |
|----------|---------------------------------|-----------------|-----|-----|-----|-----|------|
|          |                                 |                 | MIN | MAX | MIN | MAX |      |
| $V_{CC}$ | Supply voltage                  |                 | 2.7 | 3.6 | 2.7 | 3.6 | V    |
| $V_{IH}$ | High-level input voltage        |                 | 2   |     | 2   |     | V    |
| $V_{IL}$ | Low-level input voltage         |                 |     | 0.8 |     | 0.8 | V    |
| $V_I$    | Input voltage                   |                 |     | 5.5 |     | 5.5 | V    |
| $I_{OH}$ | High-level output current       |                 |     | –24 |     | –32 | mA   |
| $I_{OL}$ | Low-level output current        |                 |     | 48  |     | 64  | mA   |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled |     | 10  |     | 10  | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate     |                 | 200 |     | 200 |     | μs/V |
| $T_A$    | Operating free-air temperature  |                 | –55 | 125 | –40 | 85  | °C   |

NOTE 4:  All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54LVTH646 MIN | TYP† | MAX | SN74LVTH646 MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 2.7 V to 3.6 V, | $I_{OH}$ = −100 µA | $V_{CC}$−0.2 | | | $V_{CC}$−0.2 | | | V |
| | | $V_{CC}$ = 2.7 V, | $I_{OH}$ = −8 mA | 2.4 | | | 2.4 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = −24 mA | 2 | | | | | | |
| | | | $I_{OH}$ = −32 mA | | | | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | V |
| | | | $I_{OL}$ = 24 mA | | | 0.5 | | | 0.5 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | |
| | | | $I_{OL}$ = 32 mA | | | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 48 mA | | | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.55 | |
| $I_I$ | Control inputs | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | µA |
| | | $V_{CC}$ = 0 or 3.6 V, | $V_I$ = 5.5 V | | | 10 | | | 10 | |
| | A or B ports‡ | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 20 | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | | | −5 | | | −5 | |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | ±100 | µA |
| $I_{I(hold)}$ | A or B ports | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | 75 | | | 75 | | | µA |
| | | | $V_I$ = 2 V | −75 | | | −75 | | | |
| | | $V_{CC}$ = 3.6 V§, | $V_I$ = 0 to 3.6 V | | | | | | ±500 | |
| $I_{OZPU}$ | | $V_{CC}$ = 0 to 1.5 V, $V_O$ = 0.5 V to 3 V, $\overline{OE}$ = don't care | | | | ±100 | | | ±100 | µA |
| $I_{OZPD}$ | | $V_{CC}$ = 1.5 V to 0, $V_O$ = 0.5 V to 3 V, $\overline{OE}$ = don't care | | | | ±100 | | | ±100 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | | 0.19 | | | 0.19 | mA |
| | | | Outputs low | | | 5 | | | 5 | |
| | | | Outputs disabled | | | 0.19 | | | 0.19 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ − 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.2 | | | 0.2 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | 4 | | | 4 | | pF |
| $C_{io}$ | | $V_O$ = 3 V or 0 | | | 9 | | | 9 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ Unused terminals at $V_{CC}$ or GND
§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| | | | SN54LVTH646 | | | | SN74LVTH646 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | 150 | | 150 | | 150 | | 150 | MHz |
| $t_w$ | Pulse duration, CLK high or low | | 3.3 | | 3.3 | | 3.3 | | 3.3 | | ns |
| $t_{su}$ | Setup time, A or B before CLKAB↑ or CLKBA↑ | Data high | 1.3 | | 1.6 | | 1.2 | | 1.5 | | ns |
| | | Data low | 1.9 | | 2.6 | | 1.6 | | 2.2 | | |
| $t_h$ | Hold time, A or B after CLKAB↑ or CLKBA↑ | | 1.2 | | 1.2 | | 0.8 | | 0.8 | | ns |

## switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH646 | | | | SN74LVTH646 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | TYP† | MAX | MIN | MAX | |
| $f_{max}$ | | | 150 | | 150 | | 150 | | | 150 | | MHz |
| $t_{PLH}$ | CLKBA or CLKAB | A or B | 1 | 5.3 | | 5.9 | 1.8 | 3.1 | 4.7 | | 5.6 | ns |
| $t_{PHL}$ | | | 1.5 | 5 | | 5.9 | 1.8 | 3.1 | 4.7 | | 5.6 | |
| $t_{PLH}$ | A or B | B or A | 1 | 4.9 | | 5.6 | 1.3 | 2.3 | 3.5 | | 4.1 | ns |
| $t_{PHL}$ | | | 1.2 | 4.8 | | 5 | 1.3 | 2.4 | 3.5 | | 4.1 | |
| $t_{PLH}$ | SBA or SAB‡ | A or B | 1 | 5.3 | | 6.3 | 1.5 | 3 | 4.9 | | 6 | ns |
| $t_{PHL}$ | | | 1.3 | 5.3 | | 6.3 | 1.5 | 3.3 | 4.9 | | 6 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | 1 | 5.4 | | 6.7 | 1.1 | 3.1 | 5.2 | | 6.5 | ns |
| $t_{PZL}$ | | | 1 | 5.6 | | 6.7 | 1.1 | 3.4 | 5.2 | | 6.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | 1.7 | 6.3 | | 6.5 | 2.3 | 3.9 | 5.5 | | 6.1 | ns |
| $t_{PLZ}$ | | | 2.2 | 6.3 | | 6.5 | 2.3 | 4 | 5.5 | | 5.9 | |
| $t_{PZH}$ | DIR | A or B | 1.2 | 5.6 | | 6.8 | 1.3 | 3.4 | 5.2 | | 6.6 | ns |
| $t_{PZL}$ | | | 1.2 | 6.7 | | 6.8 | 1.3 | 3.6 | 5.2 | | 6.6 | |
| $t_{PHZ}$ | DIR | A or B | 1.1 | 7.2 | | 8.1 | 1.5 | 3.2 | 5.6 | | 6.7 | ns |
| $t_{PLZ}$ | | | 1.4 | 6.1 | | 6.6 | 1.5 | 3.8 | 5.6 | | 6.3 | |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

## PARAMETER MEASUREMENT INFORMATION
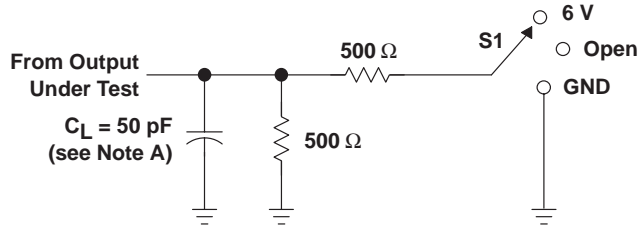


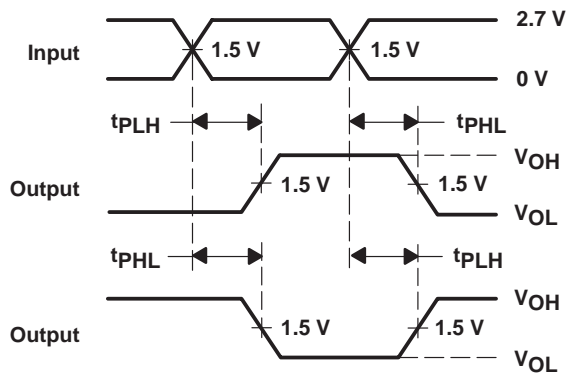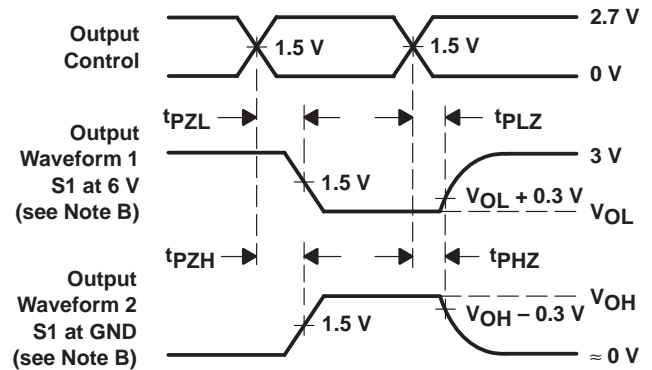| TEST | S1 |
|------|-----|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

**LOAD CIRCUIT**
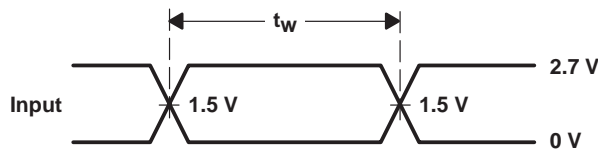
**VOLTAGE WAVEFORMS**
**PULSE DURATION**
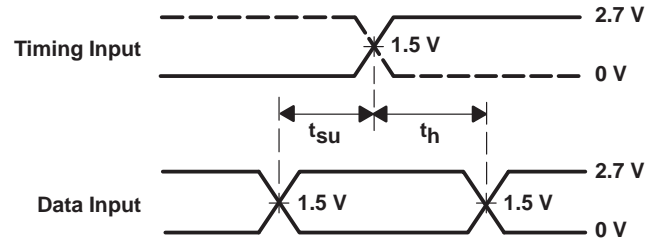
**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**
**INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES**
**LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, $t_r ≤ 2.5$ ns, $t_f ≤ 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

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