- **Member of the Texas Instruments Widebus™ Family**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Make-Before-Break Feature**
- **Internal 500-Ω Pulldown Resistors to Ground**
- **Input/Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**

description/ordering information

The SN74CBTLVR16292 is a 12-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1, and R_{INT} is connected to port B2. When S is high, port A is connected to port B2, and R_{INT} is connected to port B1.

The input/output ports include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)

S	1	56	NC
1A	2	55	NC
NC	3	54	1B1
2A	4	53	1B2
NC	5	52	2B1
3A	6	51	2B2
NC	7	50	3B1
GND	8	49	GND
4A	9	48	3B2
NC	10	47	4B1
5A	11	46	4B2
NC	12	45	5B1
6A	13	44	5B2
NC	14	43	6B1
7A	15	42	6B2
NC	16	41	7B1
V_{CC}	17	40	7B2
8A	18	39	8B1
GND	19	38	GND
NC	20	37	8B2
9A	21	36	9B1
NC	22	35	9B2
10A	23	34	10B1
NC	24	33	10B2
11A	25	32	11B1
NC	26	31	11B2
12A	27	30	12B1
NC	28	29	12B2

NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DL	Tube	SN74CBTLVR16292L	CBTLVR16292
		Tape and reel	SN74CBTLVR16292LR	
	TSSOP – DGG	Tape and reel	SN74CBTLVR16292GR	CBTLVR16292
	TVSOP – DGV	Tape and reel	SN74CBTLVR16292VR	CE292

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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TEXAS INSTRUMENTS

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FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port R_{INT} = B2 port
H	A port = B2 port R_{INT} = B1 port

logic diagram (positive logic)
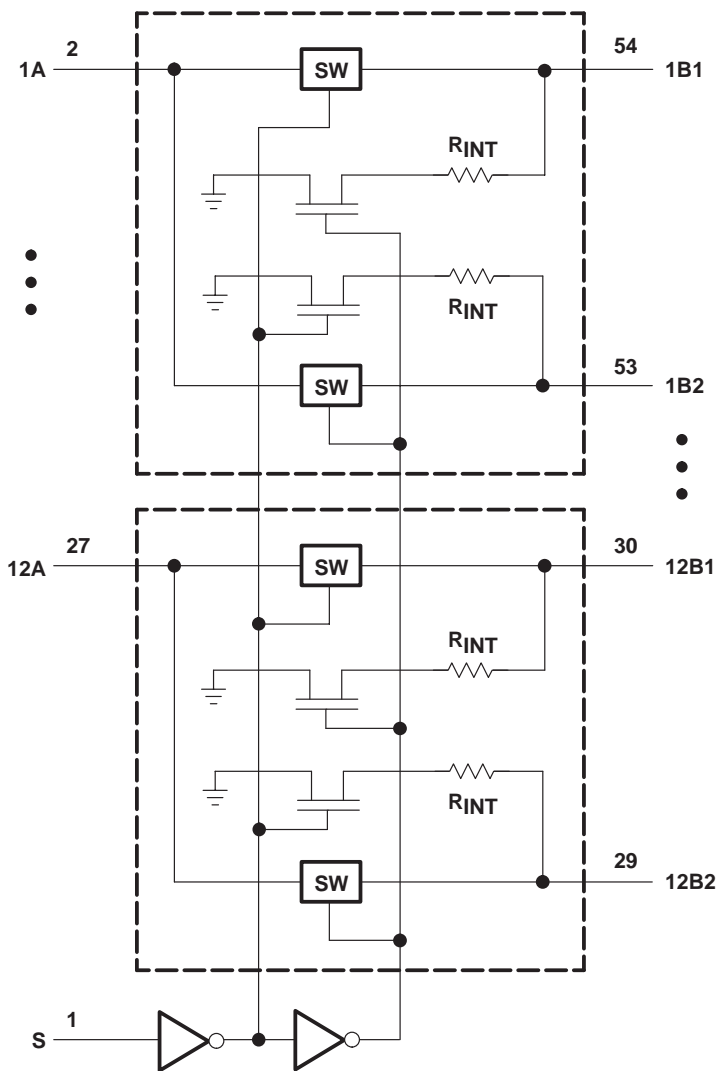
simplified schematic, each FET switch

(OE)
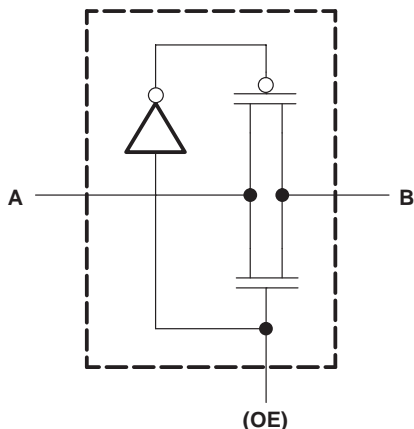
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 4.6 V
Continuous channel current .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package .... 64°C/W
DGV package .... 48°C/W
DL package .... 56°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1.   The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
             2.   The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3:   All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				10	µA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			10	µA
ΔI_{CC}[‡]	Control input	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	µA
C_i	Control input	V_I = 3.3 V or 0				3.5		pF
C_{io}	A or B port	V_O = 3.3 V or 0				23		pF
r_{on}[§]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		30	47	Ω
				I_I = 24 mA		30	47	
			V_I = 1.7 V,	I_I = 15 mA		36	80	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		30	42	
				I_I = 24 mA		30	42	
			V_I = 2.4 V,	I_I = 15 mA		32	47	

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A		0.15		0.25	ns
t_{pd}[#]	S	A	3.2	8.5	3.2	8	ns
t_{en}	S	B	1	6.5	1	5.8	ns
t_{dis}	S	B	1	5.3	1	4.6	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
# This propagation delay was measured by observing the change of voltage on the A output introduced by static levels equal to 3-V or 0 for 3.3 V ± 0.3 V or V_{CC} or 0 for 2.5 V ± 0.2 V on B1 and B2 to achieve the desired transition.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	DESCRIPTION	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_{mbb}[‖]	Make-before-break time	0	2	0	2	ns

‖ The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.
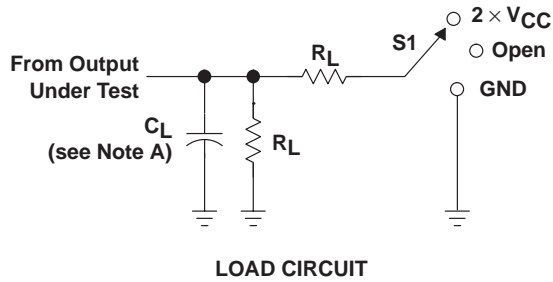
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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_Δ
2.5 V $\pm$0.2 V	30 pF	500 Ω	0.15 V
3.3 V $\pm$0.3 V	50 pF	500 Ω	0.3 V

LOAD CIRCUIT

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING
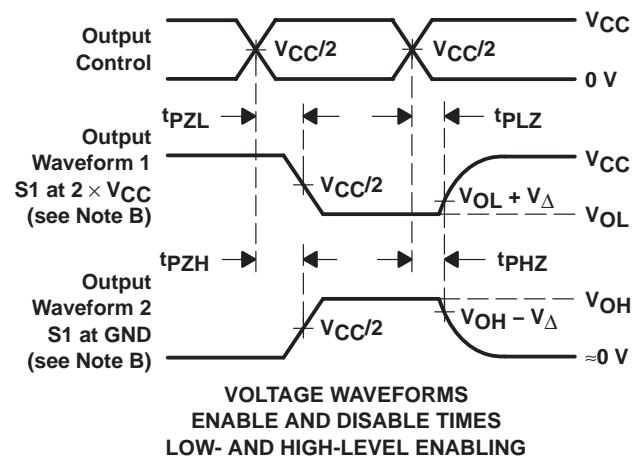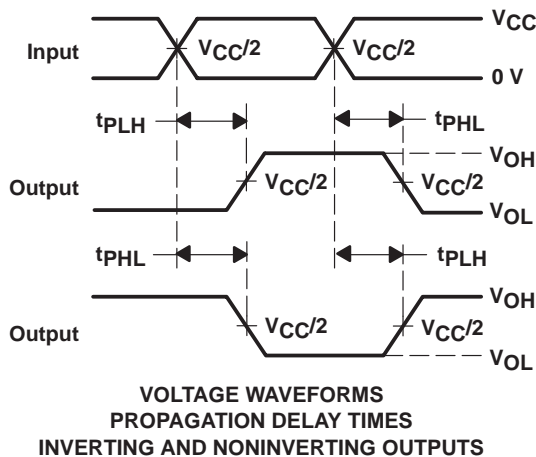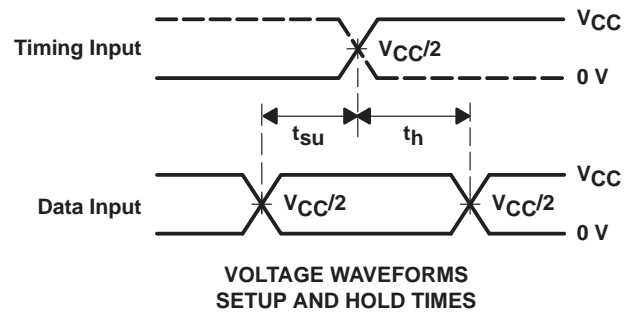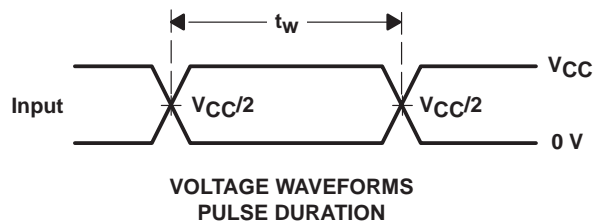
NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2 ns, $t_f \leq$ 2 ns.
   D. The outputs are measured one at a time with one transition per measurement.
   E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
   F. t_{PZL} and t_{PZH} are the same as t_{en}.
   G. t_{PLH} and t_{PHL} are the same as t_{pd}.
   H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

TEXAS INSTRUMENTS

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
           B. This drawing is subject to change without notice.
           C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
           D. Falls within JEDEC: 24/48 Pins – MO-153
                                    14/16/20/56 Pins – MO-194

DL (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

0.025 (0,635)

$\frac{0.0135\ (0,343)}{0.008\ (0,203)}$

⊕ 0.005 (0,13) Ⓜ

48   25

$\frac{0.010\ (0,25)}{0.005\ (0,13)}$

$\frac{0.299\ (7,59)}{0.291\ (7,39)}$

$\frac{0.420\ (10,67)}{0.395\ (10,03)}$

Gage Plane

0.010 (0,25)

1   24

0°–8°

A

$\frac{0.040\ (1,02)}{0.020\ (0,51)}$

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

PINS ** DIM	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
           B. This drawing is subject to change without notice.
           C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
           D. Falls within JEDEC MO-118

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DGG (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS **	48	56	64
DIM			
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold protrusion not to exceed 0,15.
   D. Falls within JEDEC MO-153

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