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● Member of the Texas Instruments <i>Widebus™</i> Family	DGG OR DL PACKAGI (TOP VIEW)				
 EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process 			1LE		
 ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0) 	1Q1 2 1Q2 3 GND 4	54 53	1D1 1D2 GND		
 Latch-Up Performance Exceeds 250 mA Per JESD 17 	1Q3 5 1Q4 6 V _{CC} 7	51	1D3 1D4 V _{CC}		
 Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown 	1Q5 [8 1Q6] 9	49	1D5 1D6		
ResistorsPackage Options Include Plastic 300-mil	1Q7 [10 GND [11	46	1D7 GND		
Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages	1Q8 12 1Q9 13	3 44	1D8 1D9		
description	1Q10 14 2Q1 15	5 42	1D10 2D1		
This 20-bit bus-interface D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.	2Q2 16 2Q3 17 GND 18	7 40	2D2 2D3 GND		
The SN74ALVCH16841 features 3-state outputs designed specifically for driving highly capacitive	2Q4 [19 2Q5 [20	9 38 0 37	2D4 2D5		
or relatively low-impedance loads. This device is particularly suitable for implementing buffer	2Q6 [21 V _{CC} [22	2 35	2D6 V _{CC}		
registers, unidirectional bus drivers, and working registers.	2Q7 23 2Q8 24	4 33	2D7 2D8		
The SN74ALVCH16841 can be used as two 10-bit latches or one 20-bit latch. The 20 latches are	GND 25 2Q9 26	5 31	GND 2D9		

A buffered output-enable $(1\overline{OE} \text{ or } 2\overline{OE})$ input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

OE does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16841 is characterized for operation from -40°C to 85°C.



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transparent D-type latches. The device has

noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched

at the levels set up at the D inputs.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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30 🛛 2D10

2LE

29

2Q10 🛿 27

28

20E

FUNC	TION	TABL	E
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	(each 10-bit latch)								
	INPUTS	OUTPUT							
OE	LE	D	Q						
L	Н	Н	Н						
L	Н	L	L						
L	L	Х	Q ₀						
Н	Х	Х	z						

logic symbol[†]

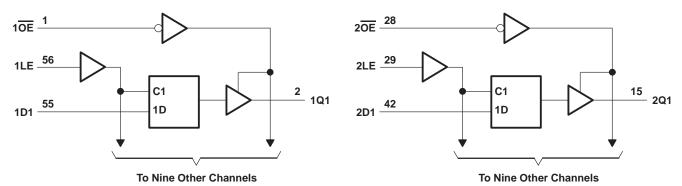
	4				
1 <mark>0E</mark>	1	EN2			
1LE	56	C1			
2 <mark>0E</mark>	28	EN4			
2LE	29	C3			
ZLC		Ľ	لے _		
1D1	55	1D	2 ▽	2	1Q1
1D2	54			3	1Q2
1D3	52			5	1Q3
1D4	51	J		6	1Q4
	49	<u> </u>		8	
1D5	48	1		9	1Q5
1D6	47	1		10	1Q6
1D7	45	·		12	1Q7
1D8	44	L		13	1Q8
1D9	43	-			1Q9
1D10		-		14	1Q10
2D1	42	3D	4 ▽	15	2Q1
2D2	41			16	2Q2
2D3	40			17	2Q3
2D4	38	J		19	2Q4
	37	L		20	
2D5	36	1		21	2Q5
2D6	34	ļ		23	2Q6
2D7	33	1		24	2Q7
2D8	31			26	2Q8
2D9					2Q9
2D10	30	-		27	2Q10
			_	l i i i i i i i i i i i i i i i i i i i	

 † This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1) Output voltage range, V _O (see Notes 1 and 2)	–0.5 V to 4.6 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, Io	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 V \text{ to } 3.6 V$	2		
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
VIL	IL Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 V \text{ to } 3.6 V$		0.8	
VI	Input voltage		0	VCC	V
VO	Output voltage		0	VCC	V
	High-level output current	V _{CC} = 1.65 V		-4	
1		$V_{CC} = 2.3 V$		-12	A
ЮН		$V_{CC} = 2.7 V$		-12	mA
		$V_{CC} = 3 V$		-24	
		V _{CC} = 1.65 V		4	
1		V _{CC} = 2.3 V		12	A
IOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		$V_{CC} = 3 V$		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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PA	RAMETER	TEST CC	ONDITIONS	Vcc	MIN	TYP†	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2			
	I _{OH} = -4 mA	1.65 V	1.2						
		I _{OH} = -6 mA		2.3 V	2				
Vон				2.3 V	1.7			V	
		I _{OH} = -12 mA		2.7 V	2.2				
				3 V	2.4				
		I _{OH} = -24 mA		3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		I _{OL} = 4 mA		1.65 V			0.45		
M		I _{OL} = 6 mA		2.3 V			0.4		
VOL				2.3 V			0.7	V	
	I _{OL} = 12 mA	2.7 V			0.4				
		I _{OL} = 24 mA		3 V			0.55		
Ι		V _I = V _{CC} or GND		3.6 V			±5	μΑ	
		V _I = 0.58 V		1.65 V	25				
		VI = 1.07 V	1.65 V	-25					
		V _I = 0.7 V	2.3 V	45					
II(hold)		V _I = 1.7 V		2.3 V	-45			μA	
、 ,		V _I = 0.8 V		3 V	75				
		V _I = 2 V		3 V	-75				
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500		
IOZ		V _O = V _{CC} or GND		3.6 V			±10	μA	
ICC		$V_{I} = V_{CC} \text{ or GND},$	IO = 0	3.6 V			40	μA	
∆lcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μA	
	Control inputs					4.5			
Ci	Data inputs	$V_{I} = V_{CC} \text{ or } GND$		3.3 V		6.5		рF	
Co	Outputs	$V_{O} = V_{CC}$ or GND		3.3 V		7		pF	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. [‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V		$V_{CC} = 1.8 V$ $V_{CC} = 2.5 V$ $\pm 0.2 V$		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tw	Pulse duration, LE high or low	§		3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE↑	§		0.9		0.7		1.1		ns
th	Hold time, data after LE↑	§		1.2		1.5		1.1		ns

§ This information was not available at time of publication.



switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} = ± 0.2	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} = ± 0.3	3.3 V 3 V	UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	
+ .	D	Q	†	1	5		4.7	1.2	3.9	00
^t pd	LE		†	1	5.6		5.1	1	4.3	ns
ten	OE	Q	†	1	6.2		6	1	4.9	ns
^t dis	OE	Q	†	1.1	5.3		4.3	1.3	4.1	ns

[†] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
		TEST CONDITIONS	TYP	TYP	TYP		
	Power dissipation	Outputs enabled	C _I = 50 pF. f = 10 MHz	†	12	20	рF
C _{pd}	capacitance	Outputs disabled	$C_{L} = 50 \text{ pF}, \text{ f} = 10 \text{ MHz}$	†	1	3	рг

[†] This information was not available at the time of publication.



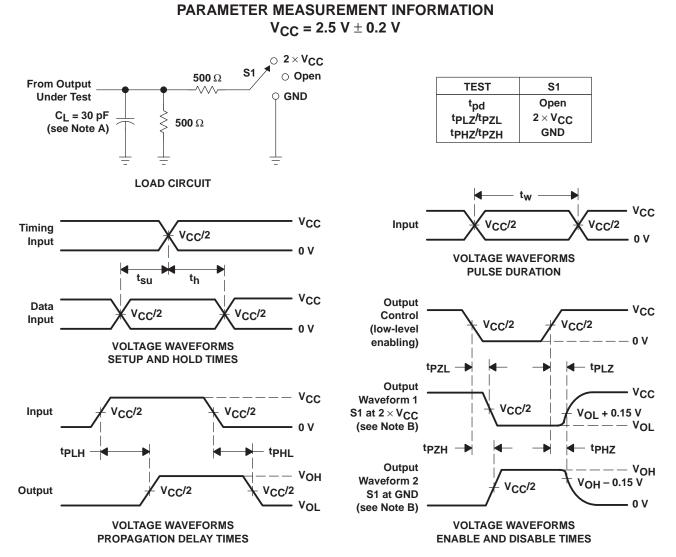
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$ $\odot 2 \times V_{CC}$ **S1** O Open **1 k**Ω From Output TEST **S1 Under Test** O GND Open ^tpd C_L = 30 pF 2×VCC tPLZ/tPZL **1 k**Ω (see Note A) tPHZ/tPZH GND LOAD CIRCUIT tw Vcc VCC V_{CC}/2 Input V_{CC}/2 Timing V_{CC}/2 0 V Input 0 V **VOLTAGE WAVEFORMS** PULSE DURATION t_{su} th Vcc Output Data VCC V_{CC}/2 Vcc/2 Control Input V_{CC}/2 V_{CC}/2 0 V (low-level 0 V enabling) **VOLTAGE WAVEFORMS** SETUP AND HOLD TIMES - t_{PLZ} ^tPZL Output Vcc Vcc Waveform 1 V_{CC}/2 V_{CC}/2 Input V_{CC}/2 S1 at $2 \times V_{CC}$ V_{OL} + 0.15 V - V_{OL} (see Note B) 0 V tPZH -- tphz ^tPLH **t**PHL Output - VOH Vон Waveform 2 VOH - 0.15 V V_{CC}/2 V_{CC}/2 Output Vcc/2 S1 at GND VOL - 0 V (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES ENABLE AND DISABLE TIMES**

- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tPLZ and tPHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2 ns, t_f \leq 2 ns.

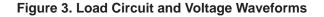
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tPLZ and tPHZ are the same as tdis.
 - F. tp71 and tp7H are the same as ten.
 - G. tpi H and tpHi are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$ O 6 V **S**1 TEST **S1** O Open **500** Ω From Output Open tpd O GND Under Test tPLZ/tPZL 6 V $C_L = 50 \text{ pF}$ tPHZ/tPZH GND **500** Ω (see Note A) -LOAD CIRCUIT 2.7 V 1.5 V Input 1.5 V 2.7 V Timing 1.5 V 0 V Input 0 V **VOLTAGE WAVEFORMS** PULSE DURATION t_{su} th 2.7 V Data 1.5 V 1.5 V Output 2.7 V Input 0 V Control 1.5 V 1.5 V (low-level **VOLTAGE WAVEFORMS** enabling) 0 V SETUP AND HOLD TIMES tPZL -^tPLZ Output 3 V 2.7 V Waveform 1 1.5 V 1.5 V 1.5 V Input S1 at 6 V V_{OL} + 0.3 V (see Note B) VOL 0 V ^tPHL ^tPLH tPZH -- ^tPHZ Output VOH V_{OH} – 0.3 V Vон Waveform 2 1.5 V 1.5 V Output 1.5 V S1 at GND 0 V (see Note B) VOL **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES ENABLE AND DISABLE TIMES**

- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .





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