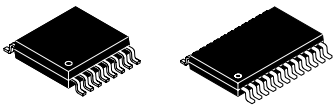


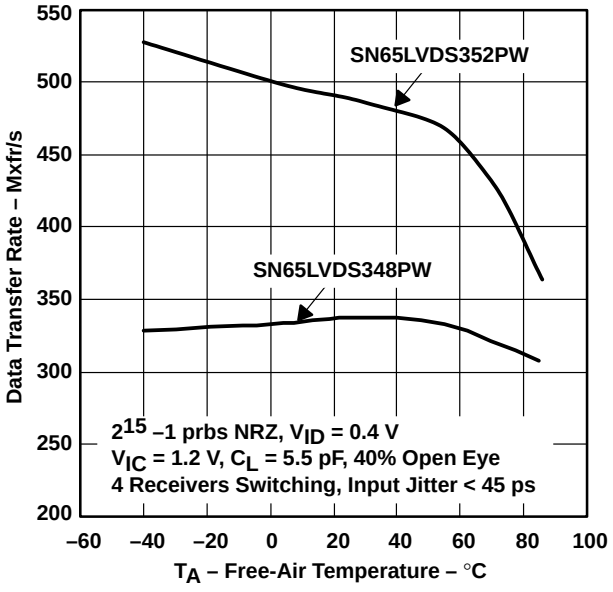
SLLS523D – FEBRUARY 2002 – REVISED FEBRUATY 2003

QUAD HIGH-SPEED DIFFERENTIAL RECEIVERS

FEATURES

- **Meets or Exceeds the Requirements of ANSI TIA/EIA-644A Standard**
- **Single-Channel Signaling Rates[1] up to 560 Mbps**
- **–4 V to 5 V Common-Mode Input Voltage Range**
- **Flow-Through Architecture**
- **Active Failsafe Assures a High-level Output When an Input Signal Is not Present**
- **SN65LVDS348 Provides a Wide Common-Mode Range Replacement for the SN65LVDS048A or the DS90LV048A**

DATA TRANSFER RATE vs FREE-AIR TEMPERATURE

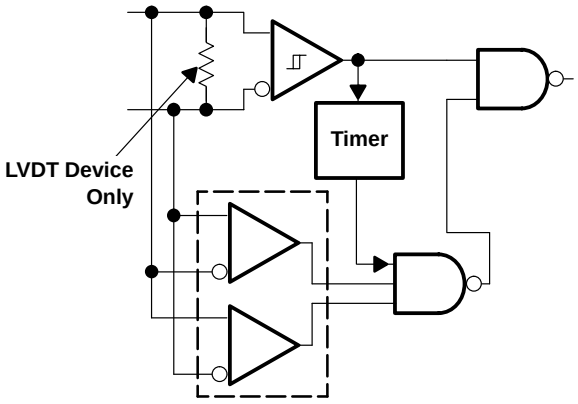


APPLICATIONS

- **Logic Level Translator**
- **Point-to-Point Baseband Data Transmission Over 100-Ω Media**
- **ECL/PECL-to-LVTTL Conversion**
- **Wireless Base Stations**
- **Central Office or PABX Switches**

DESCRIPTION

The SN65LVDS348, SN65LVDT348, SN65LVDS352, and SN65LVDT352 are high-speed, quadruple differential receivers with a wide common-mode input voltage range. This allows receipt of TIA/EIA-644 signals with up to 3-V of ground noise or a variety of differential and single-ended logic levels. The ‘348 is in a 16-pin package to match the industry-standard footprint of the DS90LV048. The ‘352 adds two additional V_{CC} and GND pins in a 24-pin package to provide higher data transfer rates with multiple receivers in operation. All offer a flow-through architecture with all inputs on one side and outputs on the other to ease board layout and reduce crosstalk between receivers. LVDT versions of both integrate a 110-Ω line termination resistor.



(One of Four Shown)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[1] The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

description (continued)

These receivers also provide 3x the standard's minimum common-mode noise voltage tolerance. The –4 V to 5 V common-mode range allows usage in harsh operating environments or accepts LVPECL, PECL, LVECL, ECL, CMOS, and LVCMOS levels without level shifting circuitry. See the Application Information Section for more details on the ECL/PECL to LVDS interface.

Precise control of the differential input voltage thresholds allows for inclusion of 50 mV of input-voltage hysteresis to improve noise rejection. The differential input thresholds are still no more than ±50 mV over the full input common-mode voltage range.

The receiver inputs can withstand ±15 kV human-body model (HBM), with respect to ground, without damage. This provides reliability in cabled and other connections where potentially damaging noise is always a threat.

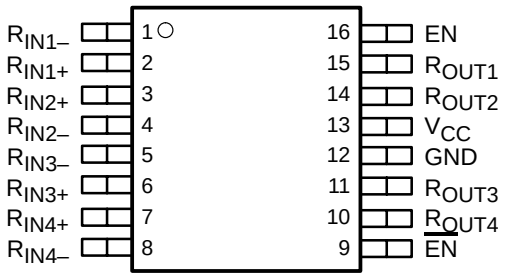
The receivers also include a (patent-pending) failsafe circuit that provides a high-level output approximately 600 ns after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or powered-down transmitters. This prevents noise from being received as valid data under these fault conditions. This feature may also be used for Wired-Or bus signaling.

The SN65LVDT348 and SN65LVDT352 include an integrated termination resistor. This reduces board space requirements and parts count by eliminating the need for a separate termination resistor. This can also improve signal integrity at the receiver by reducing the stub length from the line termination to the receiver.

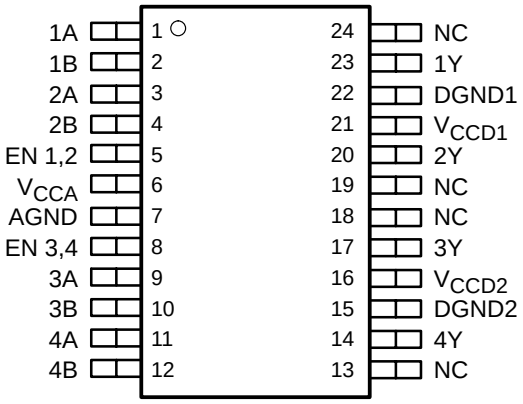
The intended application of these devices and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS348, SN65LVDT348, SN65LVDS352 and SN65LVDT352 are characterized for operation from –40°C to 85°C.

SN65LVDS348, SN65LVDT348
D or PW PACKAGE
(TOP VIEW)

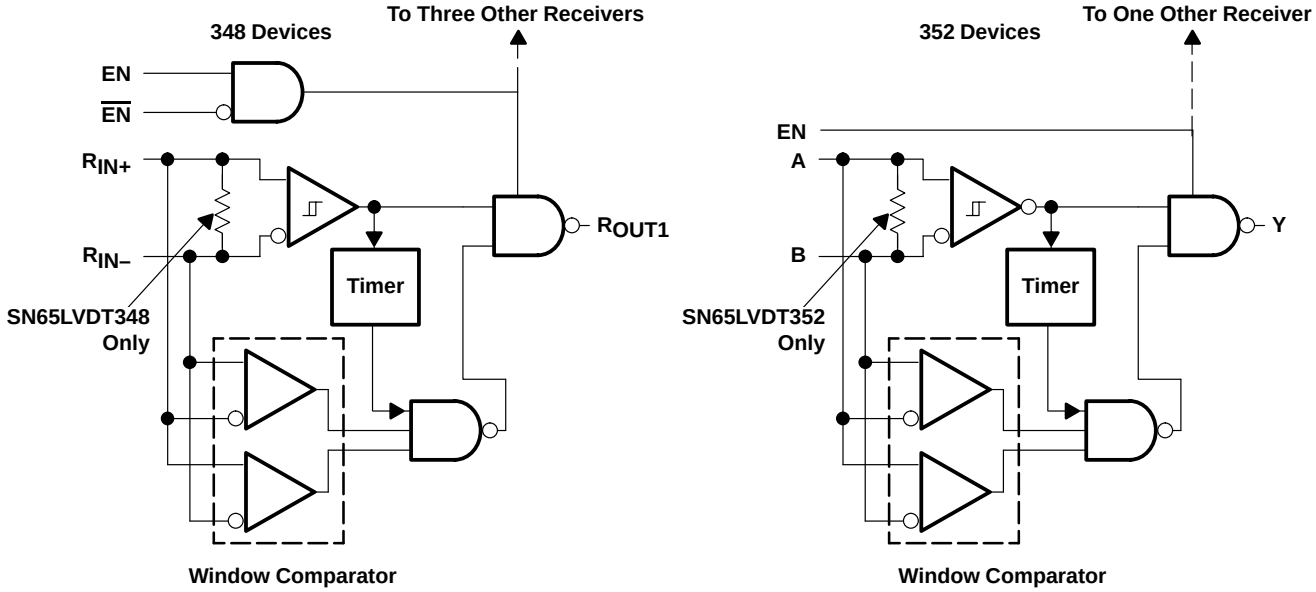


SN65LVDS352, SN65LVDT352
PW PACKAGE
(TOP VIEW)



NC – No internal connection

functional block diagrams (one of four receivers shown)



AVAILABLE OPTIONS

PART NUMBER†	INTEGRATED TERMINATION	PACKAGE TYPE	PACKAGE MARKING
SN65LVDS348D		SOIC	LVDS348
SN65LVDT348D	✓	SOIC	LVDT348
SN65LVDS348PW		TSSOP	DL348
SN65LVDT348PW	✓	TSSOP	DE348
SN65LVDS352PW		TSSOP	DL352
SN65LVDT352PW	✓	TSSOP	DE352

† Add the R suffix to the device type (e.g., SN65LVDS348DR) for taped and reeled carrier.

Function Tables

348 DEVICES

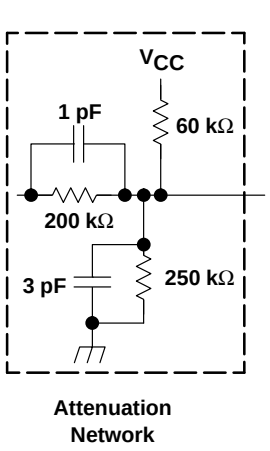
INPUTS			OUTPUTS
$V_{ID} = V_{RIN+} - V_{RIN-}$	EN	$\overline{EN}$	R_{OUT}
$V_{ID} \geq -32$ mV	H	L or OPEN	H
-100 mV < $V_{ID} < -32$ mV	H	L or OPEN	?
$V_{ID} \leq -100$ mV	H	L or OPEN	L
Open	H	L or OPEN	H
X	L or OPEN	X	Z
	X	H	Z

352 DEVICES

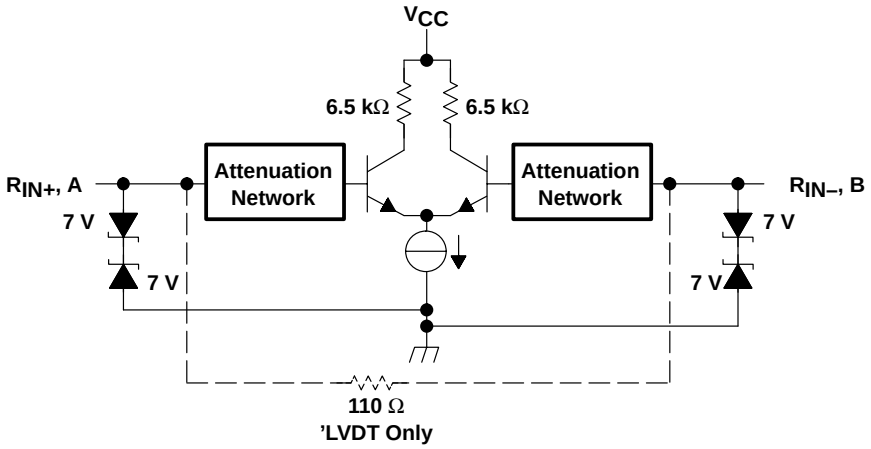
INPUTS		OUTPUTS
$V_{ID} = V_{IA} - V_{IB}$	EN	Y
$V_{ID} \geq -32$ mV	H	H
-100 mV < $V_{ID} < -32$ mV	H	?
$V_{ID} \leq -100$ mV	H	L
X	L or OPEN	Z
Open	H	H

H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

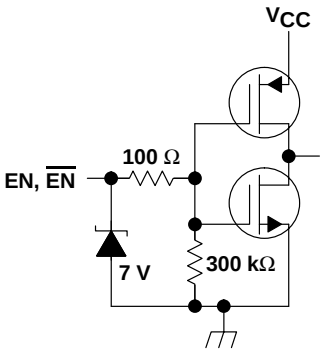
equivalent input and output schematic diagrams

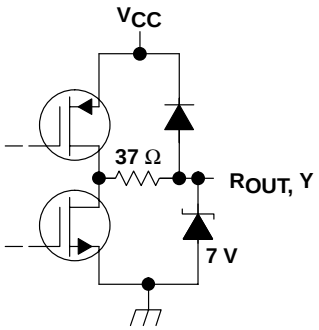


Attenuation Network



'LVDT Only





absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range (see Note 1), V_{CC}, V_{CCA}, V_{CCD1}, and V_{CCD2} . . . . . –0.5 V to 4 V
Voltage range: Enables, R_{OUT}, or Y . . . . . –0.5 V to 6 V
Differential input magnitude $|V_{ID}|$ (LVDT only) . . . . . 1 V
R_{IN+}, $R_{IN–}$, A or B . . . . . –5 V to 6 V
Electrostatic discharge: Human body model (see Note 2): A, B, R_{IN+}, $R_{IN–}$ and GND . . . . . ±15 kV
All pins . . . . . ±7 kV
Charged-device model (see Note 3): All pins . . . . . ±500 V
Continuous power dissipation . . . . . See Dissipation Rating Table
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal (GND, AGND).
2. Tested in accordance with JEDEC Standard 22, Test Method A114-A.
3. Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D16	950 mW	7.6 mW/°C	494 mW
PW16	774 mW	6.2 mW/°C	402 mW
PW24	1087 mW	8.7 mW/°C	565 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}, V_{CCA}, V_{CCD1}, and V_{CCD2}		3	3.3	3.6	V
High-level input voltage, V_{IH}	Enables	2		5	V
Low-level input voltage, V_{IL}	Enables	0		0.8	V
Magnitude of differential input voltage	$\|V_{ID}\|$ (LVDT348, 352)	0.1		0.8	V
	$\|V_{ID}\|$ (LVDS348, 352)	0.1		3	
Input voltage (any combination of common mode or input signals)		–4		5	V
Operating free-air temperature, T_A		–40		85	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{ITH1}	Positive-going differential input voltage threshold		See Figure 1 and Figure 2				50	mV
V_{ITH2}	Negative-going differential input voltage threshold				–50			
V_{ITH3}	Differential input failsafe voltage threshold		See Figure 1 and Table 1		–32		–100	mV
$V_{ID(HYS)}$	Differential input voltage hysteresis, $V_{ITH1} - V_{ITH2}$					50		mV
V_{OH}	High-level output voltage		I_{OH} = –4 mA		2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 4 mA				0.4	V
I_{CC}	Supply current	LVDS348, LVDT348	Enabled, EN at V_{CC},	$\overline{EN}$ at 0 V, No load		16	20	mA
			Disabled, EN at 0 or $\overline{EN}$ at V_{CC}			1.1	4	
		LVDS352, LVDT352	Enabled, EN at V_{CC},	No load		16	20	mA
			Disabled, EN at 0			1.1	4	
I_I	Input current (RIN+, RIN–, A or B inputs)	LVDS348, LVDS352	V_I = –4 V,	Other input open	–75		0	µA
			0 V ≤ V_I ≤ 2.4 V,	Other input 1.2 V	–20		0	
			V_I = 5 V,	Other input open	0		40	
		LVDT348, LVDT352	V_I = –4 V,	Other input open	–150		0	µA
			0 V ≤ V_I ≤ 2.4 V,	Other input open	–40		0	
			V_I = 5 V,	Other input open	0		80	
$I_{I(OFF)}$	Power–off input current (RIN+, RIN–, A or B inputs)	LVDS348, LVDS352	V_{CC} = 1.5 V, Other input open	V_I = –4 V or 5 V,	–50		50	µA
			V_{CC} = 1.5 V, Other input at 1.2 V	0 V ≤ V_I ≤ 2.4 V,	–20		20	
		LVDT348, LVDT352	V_{CC} = 1.5 V, Other input open	V_I = –4 V or 5 V,	–100		100	µA
			V_{CC} = 1.5 V, Other input open	V_I = 0 V or 2.4 V,	–40		40	
I_{ID}	Differential input current ($I_{RIN+} - I_{RIN-}$, or $I_{IA} - I_{IB}$)	LVDS348, LVDS352	V_{ID} = 100 mV,	V_{IC} = –3.9 V or 4.9 V	–4		4	µA
R_T	Differential input resistance	LVDT348, LVDT352	V_{CC} = 0 V, V_I = 0 V to 2.4 V	V_{ID} = 250 mV,	90	111	132	Ω
I_{IH}	High-level input current	Enables	V_{IH} = 2 V		0		10	µA
I_{IL}	Low-level input current	Enables	V_{IL} = 0.8 V		0		10	µA
I_{OZ}	High-impedance output current		V_O = 0 V		–10		10	µA
C_{IN}	Input capacitance, R_{IN+}, R_{IN-} input to GND or A or B input to AGND		V_I = 0.4 sin (4E6πft) + 0.5 V			5		pF

† All typical values are at 25°C and with a 3.3-V supply.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 3	2.5	4	6	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2.5	4	6	ns
t_{d1}	Delay time, failsafe disable time				9	ns
t_{d2}	Delay time, failsafe enable time		0.3		1.5	µs
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL1} - t_{pLH1} \rvert$)			200		ps
$t_{sk(o)}$	Output skew‡			150		ps
$t_{sk(pp)}$	Part-to-part skew§				1	ns
t_r	Output signal rise time			1.2		ns
t_f	Output signal fall time			1		ns
t_r	Output signal rise time	C_L = 1 pF, See Figure 3		650		ps
t_f	Output signal fall time			400		ps
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 4 and Figure 5		5	9	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			5	9	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output			8	12	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			8	12	ns

† All typical values are at 25°C and with a 3.3-V supply.
‡ $t_{sk(o)}$ is the magnitude of the time difference between the t_{PHL} or t_{PLH} of all receivers of a single device with all of their inputs connected together.
§ $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

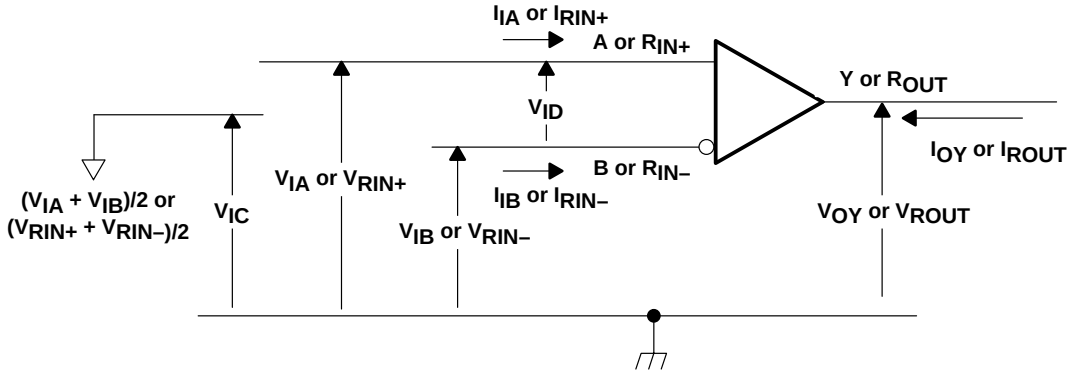
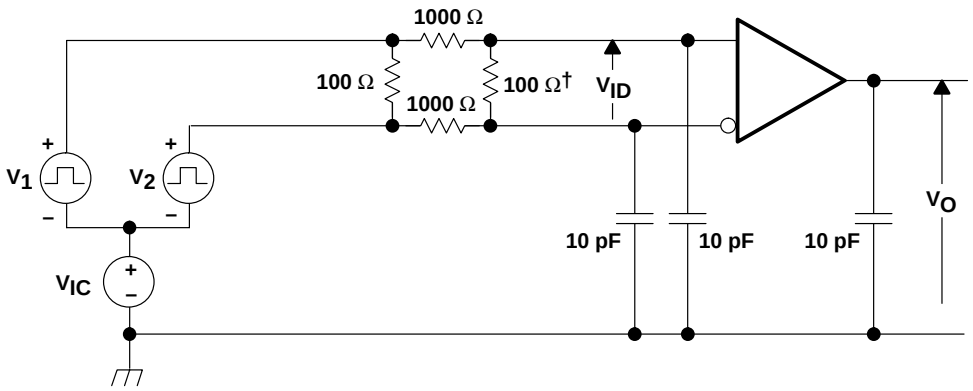


Figure 1. Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION



† Remove for testing LVDT device.

NOTES: A. Input signal of 3 MHz, duty cycle of 50±0.2%, and transition time of < 1ns.
B. Fixture capacitance ±20%.
C. Resistors are metal film, 1% tolerance, and surface mount

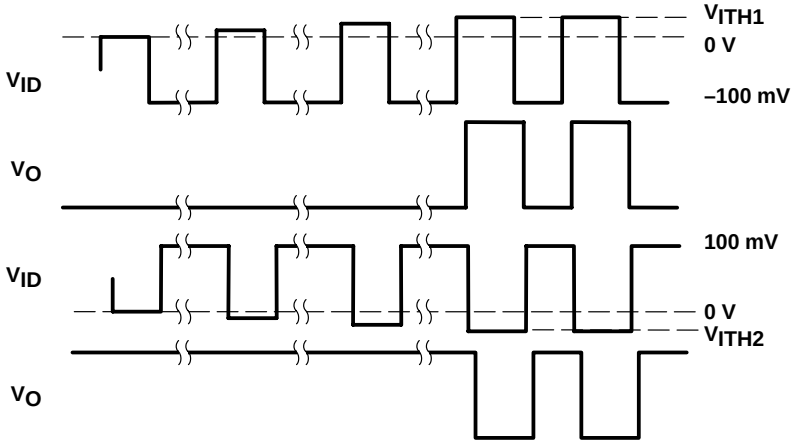


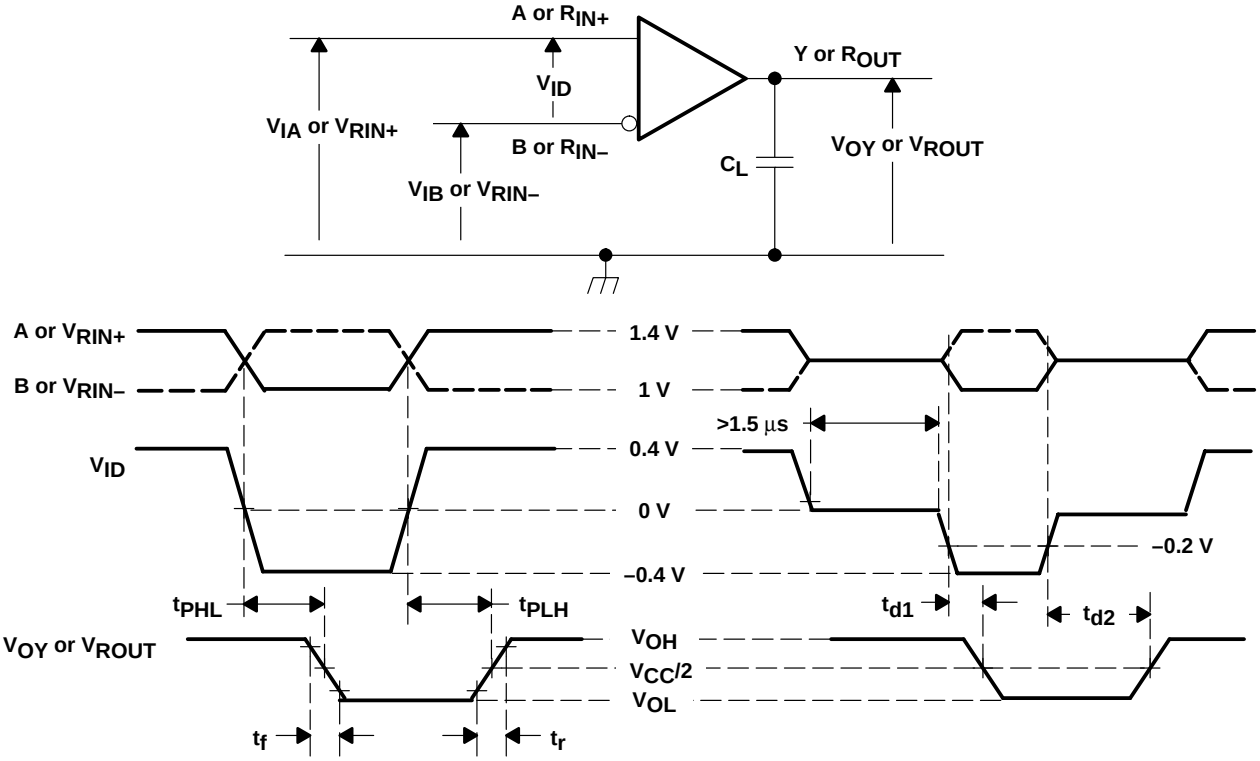
Figure 2. V_{ITH1} and V_{ITH2}, Input Voltage Threshold Test Circuit and Definitions

Table 1. Receiver Minimum and Maximum Failsafe Input Voltage

FAILSAFE THRESHOLD TEST VOLTAGES				
APPLIED VOLTAGES†		RESULTANT INPUTS		Output
V_{IA} (mV)	V_{IB} (mV)	V_{ID} (mV)	V_{IC} (mV)	
–4000	–3900	–100	–3950	L
–4000	–3968	–32	–3984	H
4900	5000	–100	4950	L
4968	5000	–32	4984	H

† Voltage applied for greater than 1.5 μs.

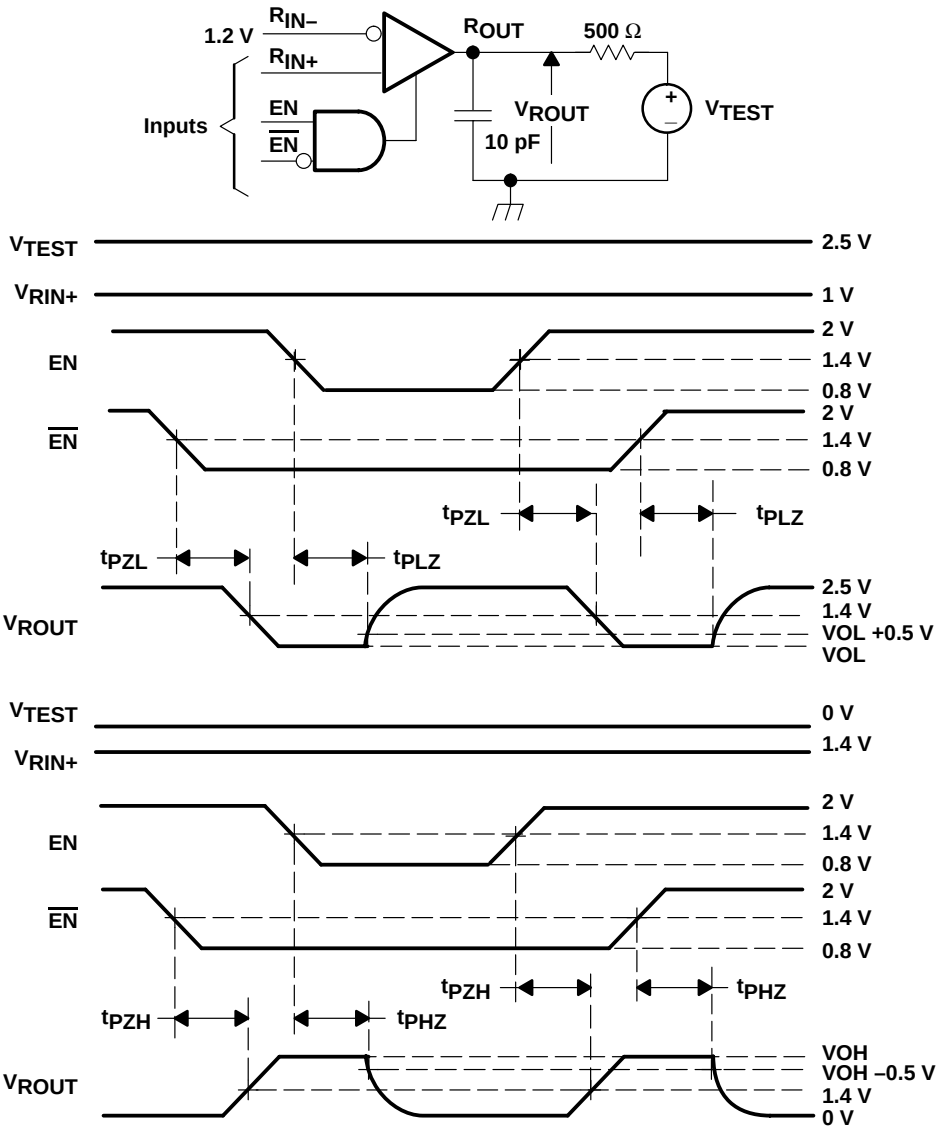
PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, signaling rate = 250 kHz, duty cycle = 50 ±2%, C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T and is ±20%.

Figure 3. Timing Test Circuit and Waveforms

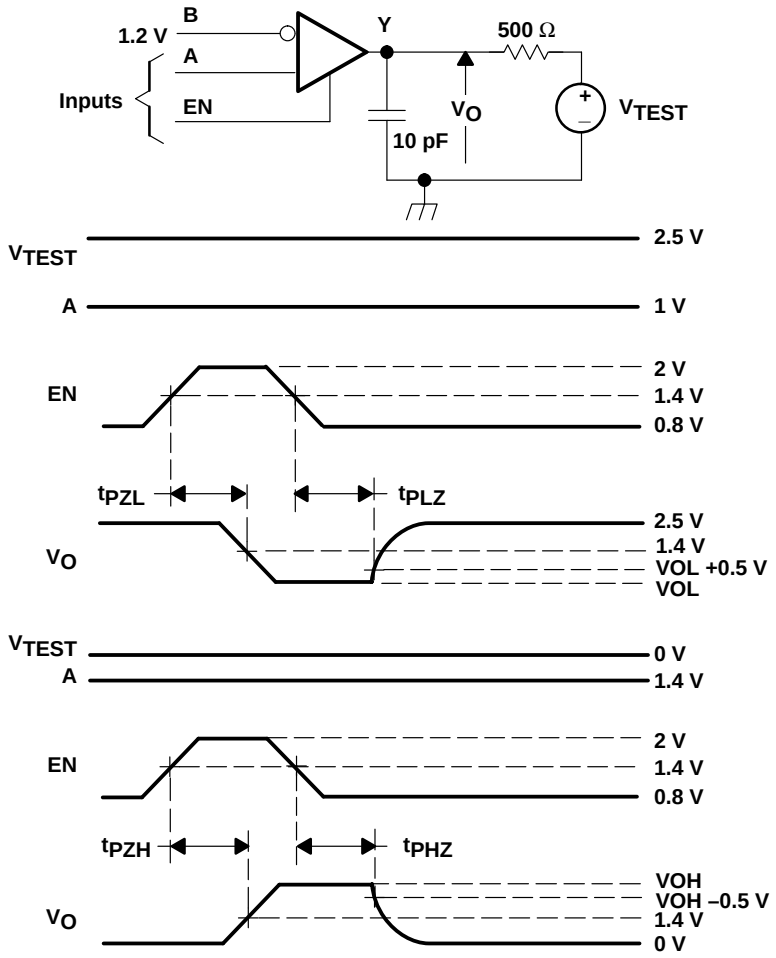
PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, signaling rate = 500 kHz, duty cycle = 50 ±2%, C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T and is ±20%.

Figure 4. 348 Enable/Disable Time Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, signaling rate = 500 kHz, duty cycle = 50 ±2 %, C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T and is ±20%.

Figure 5. 352 Enable/Disable Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

LOW-TO-HIGH PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

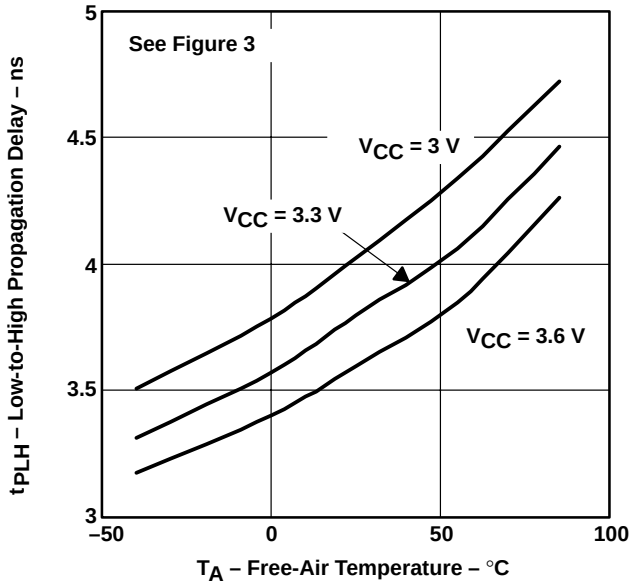


Figure 6

HIGH-TO-LOW PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

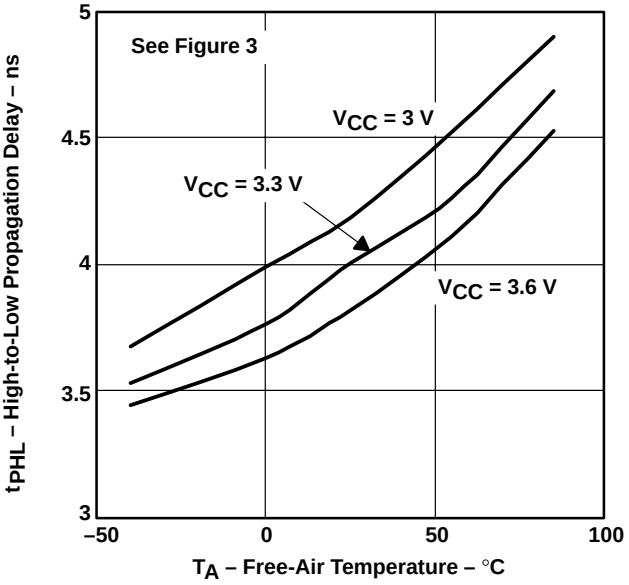


Figure 7

LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

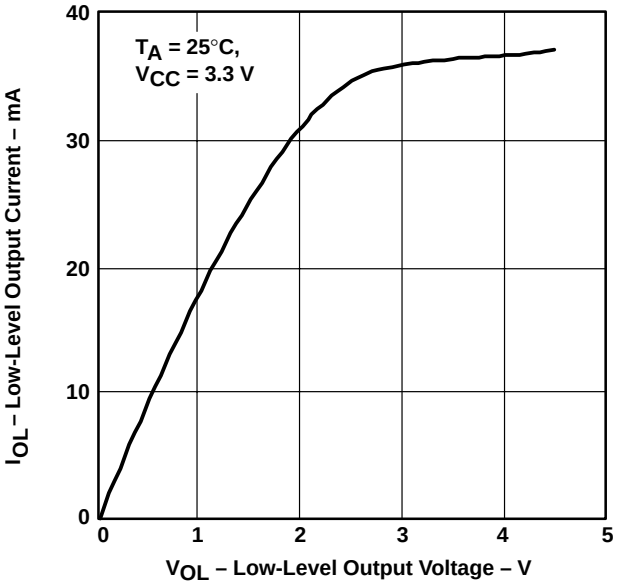


Figure 8

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

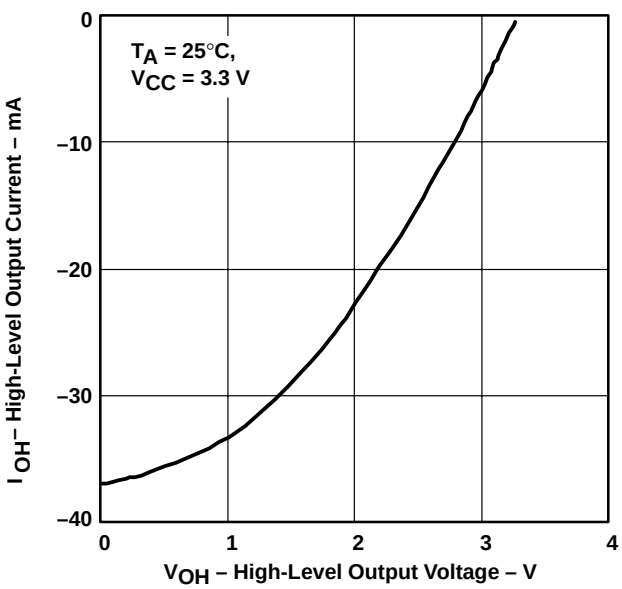


Figure 9

TYPICAL CHARACTERISTICS

DATA TRANSFER RATE vs FREE-AIR TEMPERATURE

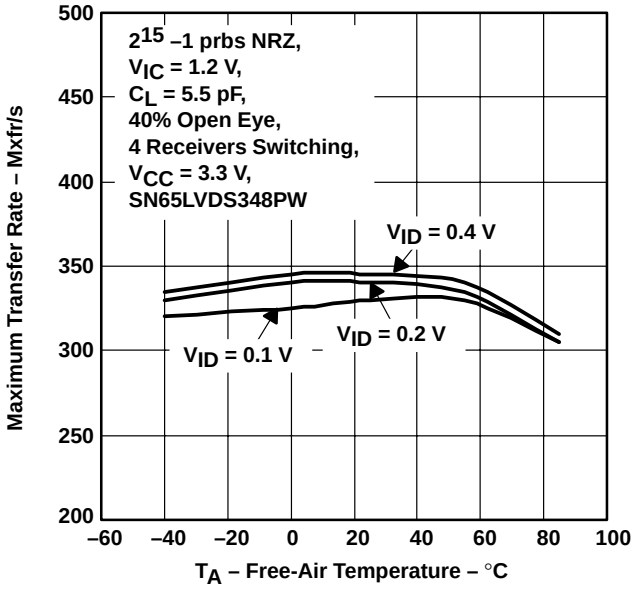


Figure 10

RMS SUPPLY CURRENT vs SWITCHING FREQUENCY

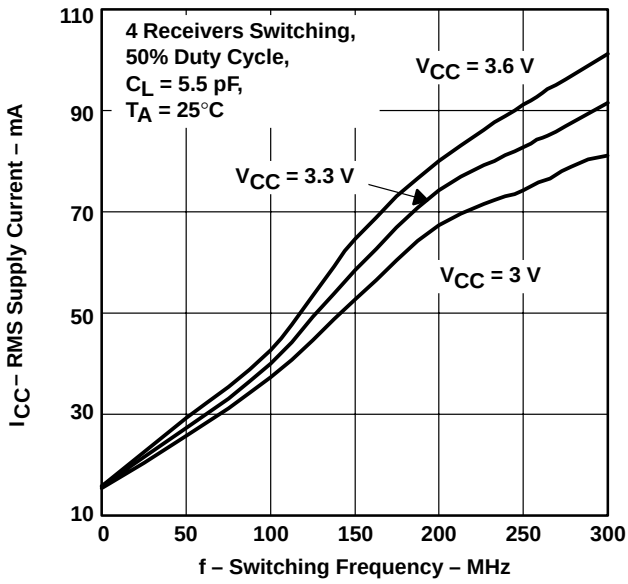


Figure 11

2^{23} –1 prbs NRZ, T_A = 25°C, C_L = 5.5 pF,
4 Receivers Switching, V_{CC} = 3.3 V

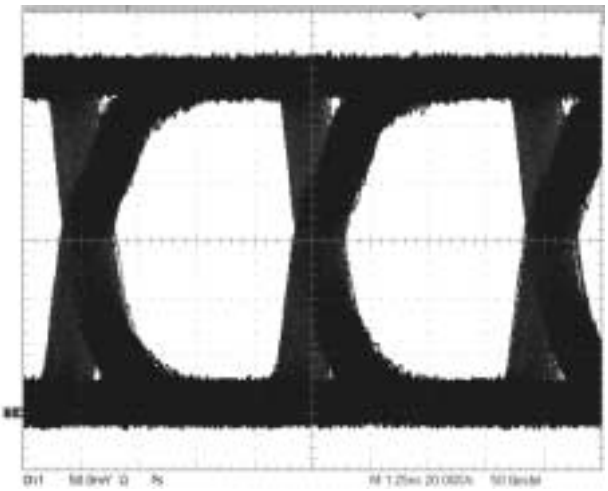


Figure 12. SN65LVDS348 Eye Pattern Running at 200 Mxfr/s

2^{23} –1 prbs NRZ, T_A = 25°C, C_L = 5.5 pF,
4 Receivers Switching, V_{CC} = 3.3 V

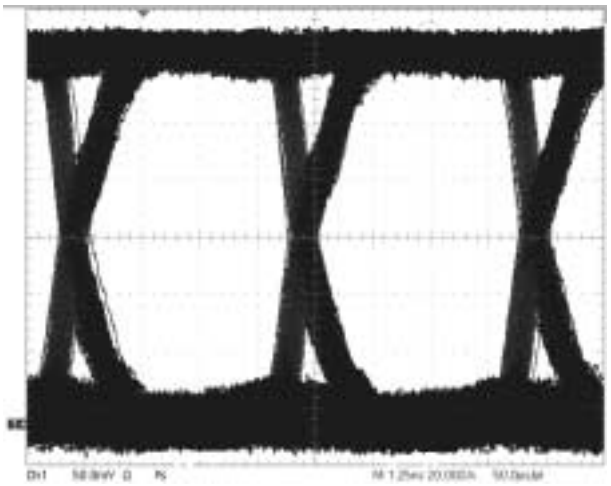


Figure 13. SN65LVDS352 Eye Pattern Running at 200 Mxfr/s

APPLICATION INFORMATION

impedance matching and reflections

A termination mismatch can result in reflections that degrade the signal at the load. A low source impedance causes the signal to alternate polarity at the load (oscillates) as shown in Figure 14. High source impedance results in the signal accumulating monotonically to the final value (stair step) as shown in Figure 15. Both of these modes result in a delay in valid signal and reduce the opening in the eye pattern. A 10% termination mismatch results in a 5% reflection ($\rho = Z_L - Z_O/Z_L + Z_O$), even a 1:3 mismatch absorbs half of the incoming signal. This shows that termination is important in the more critical cases, however, in a general sense, a rather large termination mismatch is not as critical when the differential output signal is much greater than the receiver sensitivity.

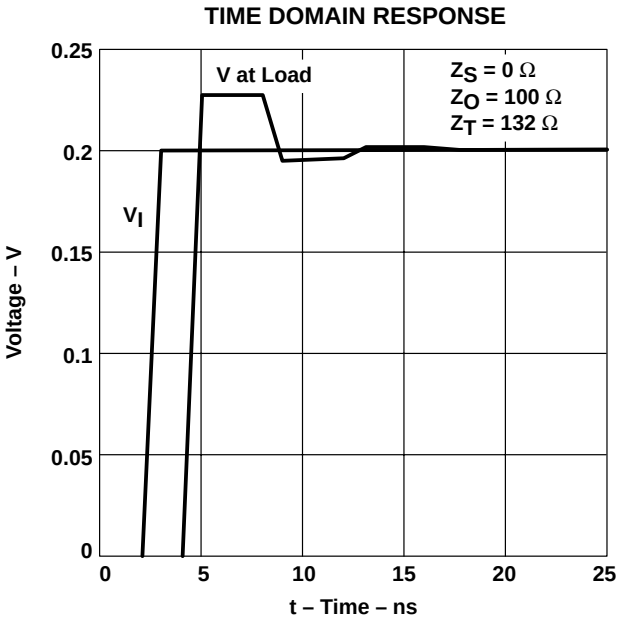


Figure 14. Low-Source Impedance

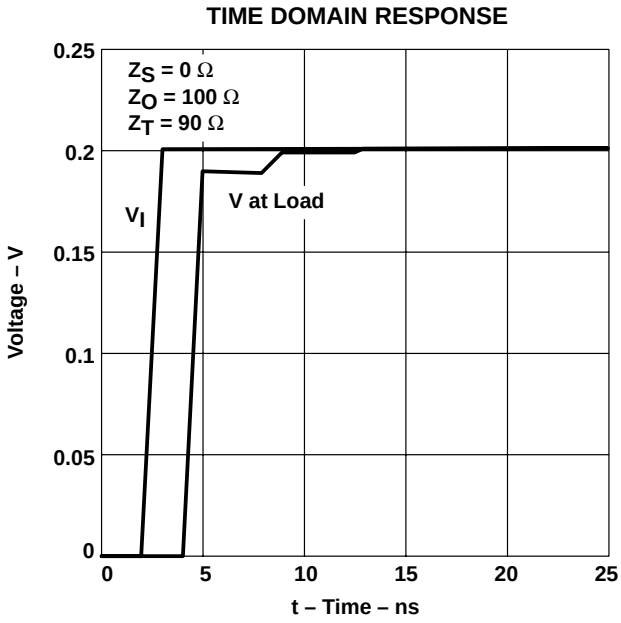


Figure 15. High-Source Impedance

For example a 200-mV drive signal into a 100-Ω lossless transmission media with a termination resistor of 90 Ω to 132 Ω results in ~227 mV to 189 mV into the receiver. This would typically be more than enough signal into a receiver with a sensitivity of ±50 mV assuming no other disturbance or attenuation on the line. The other factors, which reduce the signal margin, do affect this and therefore it is important to match the impedance as closely as possible to allow more noise immunity at the receiver.

APPLICATION INFORMATION

active failsafe feature

A differential line receiver commonly has a failsafe circuit to prevent it from switching on input noise. Current LVDS failsafe solutions require either external components with subsequent reductions in signal quality or integrated solutions with limited application. This family of receivers has a new integrated failsafe that solves the limitations seen in present solutions. A detailed theory of operation is presented in application note *The Active Fail-Safe in TI's LVDS Receivers,* literature number SLLA082B.

The following figure shows one receiver channel with active failsafe. It consists of a main receiver that can respond to a high-speed input differential signal. Also connected to the input pair are two failsafe receivers that form a window comparator. The window comparator has a much slower response than the main receiver and it detects when the input differential falls below 80 mV. A 600-ns failsafe timer filters the window comparator outputs. When failsafe is asserted, the failsafe logic drives the main receiver output to logic high.

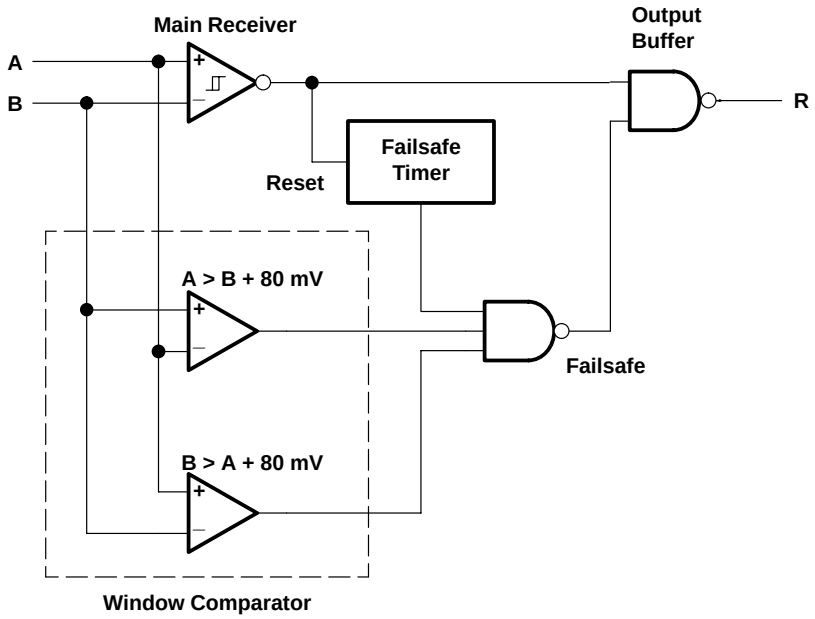


Figure 16. Receiver With Active Failsafe

APPLICATION INFORMATION

ECL/PECL-to-LVTTL conversion with TI's LVDS receiver

The various versions of emitter-coupled logic (i.e., ECL, PECL and LVPECL) are often the physical layer of choice for system designers. Designers know that established technology is capable of high-speed data transmission. In the past, system requirements often forced the selection of ECL. Now technologies like LVDS provide designers with another alternative. While the total exchange of ECL for LVDS may not be a design option, designers have been able to take advantage of LVDS by implementing a small resistor divider network at the input of the LVDS receiver. TI has taken the next step by introducing a wide common-mode LVDS receiver (no divider network required) which can be connected directly to an ECL driver with only the termination bias voltage required for ECL termination (V_{CC} – 2 V).

Figure 17 shows the use of an LV/PECL driver driving 5 meters of CAT–5 cable and being received by TI's wide common-mode receiver and the resulting eye-pattern. The values for R3 are required in order to provide a resistor path to ground for the LV/PECL driver. With no resistor divider, R1 simply needs to match the characteristic load impedance of 50 Ω. The R2 resistor is a small value intended to minimize common-mode reflections.

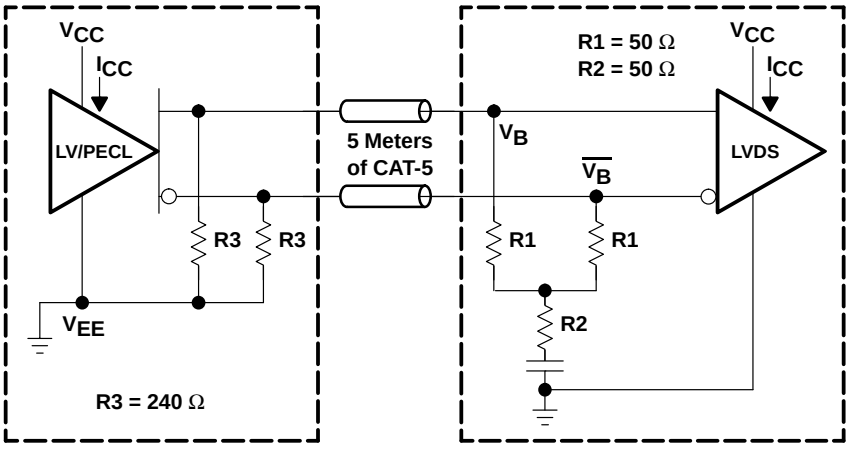


Figure 17. LVPECL or PECL to Remote Wide Common-Mode LVDS Receiver

APPLICATION INFORMATION

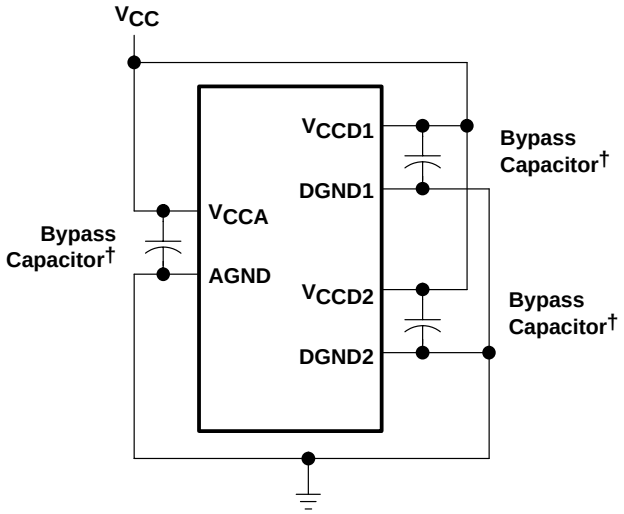
device power and grounding

The SN65LVDS352 device provides separate power and ground pins for the analog input section and the two digital output sections. All of the power pins and all of the ground pins of the device must be tied together at some point in the system. Figure 18 shows one recommended scheme for power and ground to the device. This point will be determined by the power and grounding distribution design, which can greatly affect system performance.

Key points to remember when routing power and grounds in your system are:

- The grounding system must provide a low impedance path back to the power source.
- The signal return must be close to the signal path.
- Ground noise occurs due to ground loops and common-mode noise pick-up.
- Closely spaced power and ground planes reduce inductance and increase capacitance.

A good rule to remember when doing your power distribution and board layout is that the current always flows in the lowest impedance path. At dc the lowest resistance is the lowest impedance, but at high frequencies the lowest impedance is the lowest inductance path.



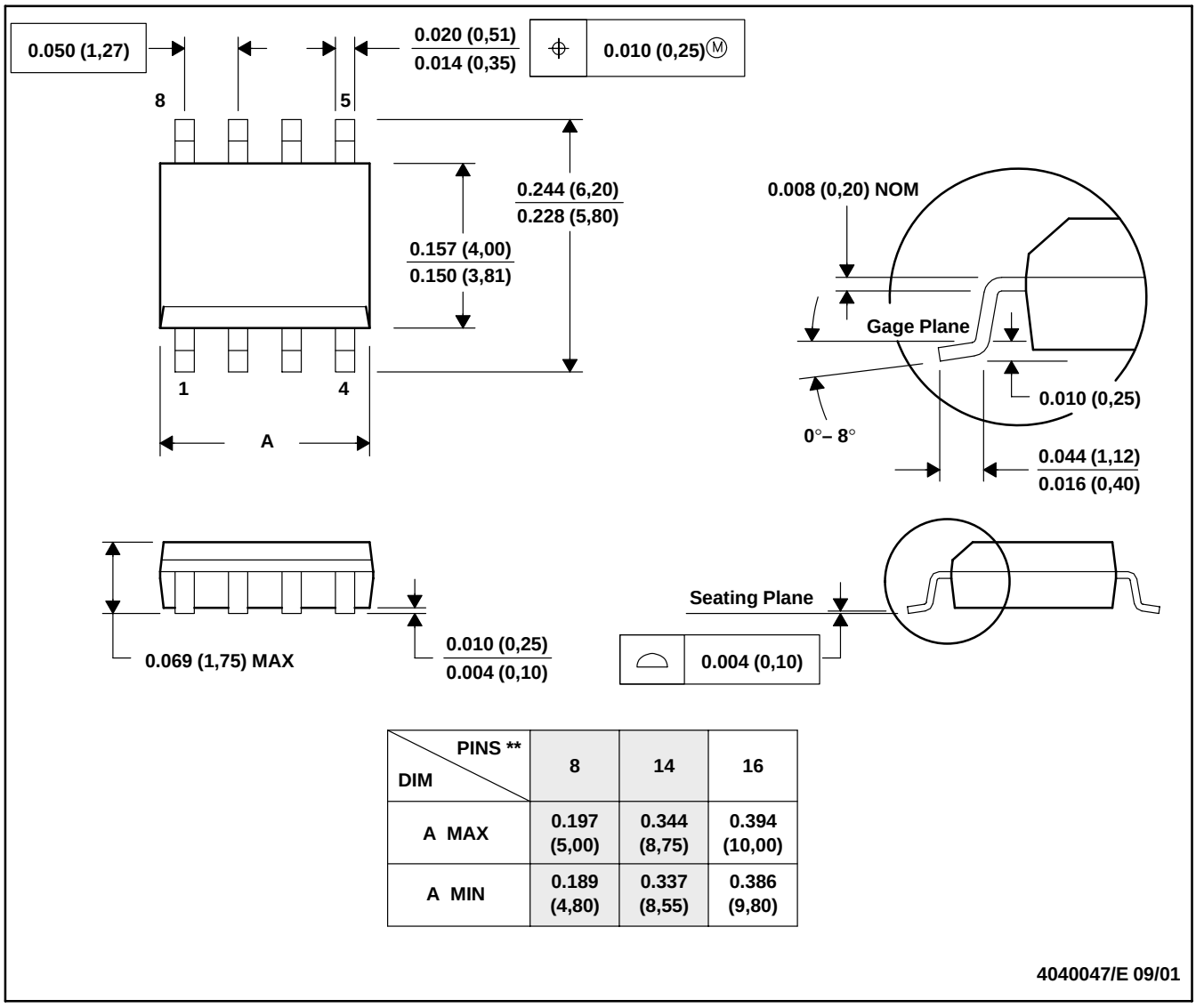
† Bypass capacitors used for data sheet electrical testing were low ESR ceramic, surface mount, 0.01 μF ±10%. For a more accurate determination of these values refer to the application note, *The Bypass Capacitor in High-Speed Environments*, literature number SCBA007A.

Figure 18. Recommended Power and Ground Connection

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

8 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

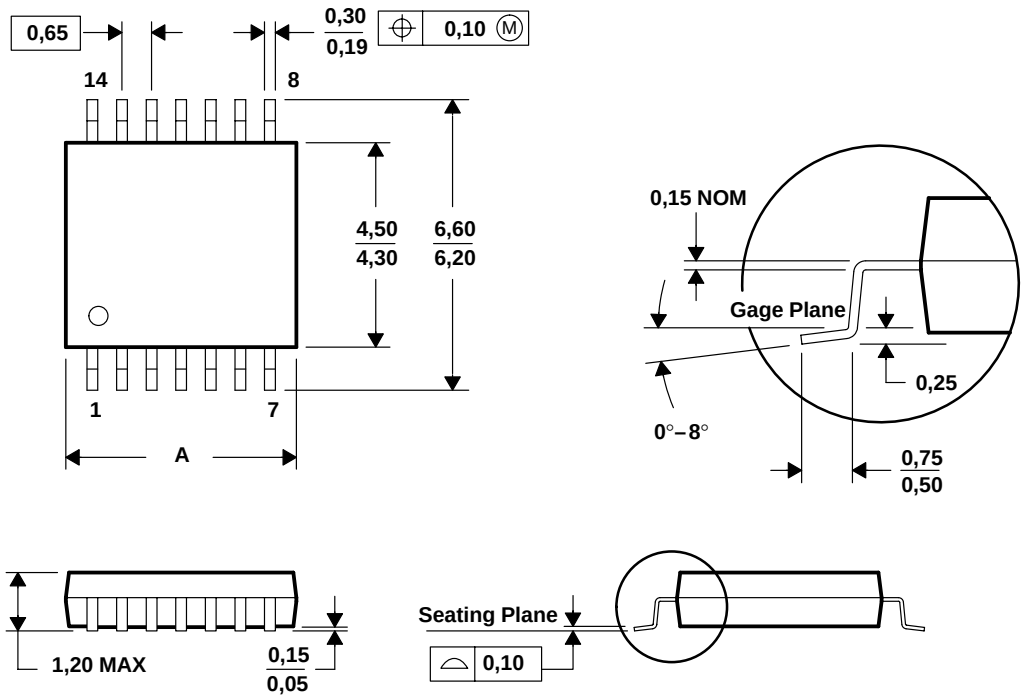
4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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