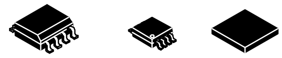


DIFFERENTIAL TRANSLATOR/REPEATER

FEATURES

- **Designed for Signaling Rates (1) ≥ 2 Gbps**
- **Total Jitter < 65 ps**
- **Low-Power Alternative for the MC100EP16**
- **Low 100 ps (Max) Part-To-Part Skew**
- **25 mV of Receiver Input Threshold Hysteresis Over 0-V to 4-V Common-Mode Range**
- **Inputs Electrically Compatible With LVPECL, CML, and LVDS Signal Levels**
- **3.3-V Supply Operation**
- **LVDT Integrates 110-Ω Terminating Resistor**
- **Offered in SOIC and MSOP**

APPLICATIONS

- **622 MHz Central Office Clock Distribution**
- **High-Speed Network Routing**
- **Wireless Basestations**
- **Low Jitter Clock Repeater**
- **Serdes LVPECL Output to FPGA LVDS Input Translator**

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

DESCRIPTION

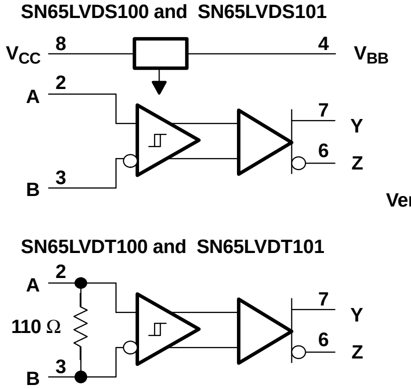
The SN65LVDS100, SN65LVDT100, SN65LVDS101, and SN65LVDT101 are a high-speed differential receiver and driver connected as a repeater. The receiver accepts low-voltage differential signaling (LVDS), positive-emitter-coupled logic (PECL), or current-mode logic (CML) input signals at rates up to 2 Gbps and repeats it as either an LVDS or PECL output signal. The signal path through the device is differential for low radiated emissions and minimal added jitter.

The outputs of the SN65LVDS100 and SN65LVDT100 are LVDS levels as defined by TIA/EIA-644-A. The outputs of the SN65LVDS101 and SN65LVDT101 are compatible with 3.3-V PECL levels. Both drive differential transmission lines with nominally 100-Ω characteristic impedance.

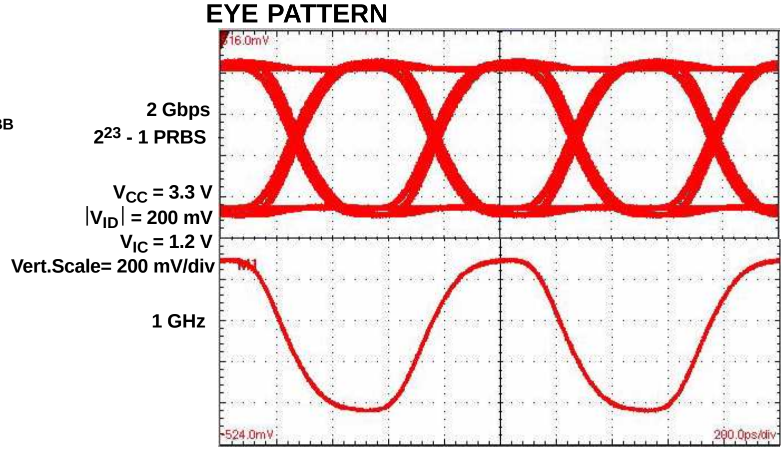
The SN65LVDT100 and SN65LVDT101 include a 110-Ω differential line termination resistor for less board space, fewer components, and the shortest stub length possible. They do not include the V_{BB} voltage reference found in the SN65LVDS100 and SN65LVDS101. V_{BB} provides a voltage reference of typically 1.35 V below V_{CC} for use in receiving single-ended input signals and is particularly useful with single-ended 3.3-V PECL inputs. When not used, V_{BB} should be unconnected or open.

All devices are characterized for operation from –40°C to 85°C.

FUNCTIONAL DIAGRAM



EYE PATTERN



Horizontal Scale= 200 ps/div

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

OUTPUT	TERMINATION RESISTOR	V_{BB}	PART NUMBER(1)	PART MARKING	PACKAGE
LVDS	No	Yes	SN65LVDS100D	DL100	SOIC
LVDS	No	Yes	SN65LVDS100DGK	AZK	MSOP
LVDS	Yes	No	SN65LVDT100D	DE100	SOIC
LVDS	Yes	No	SN65LVDT100DGK	AZL	MSOP
LVPECL	No	Yes	SN65LVDS101D	DL101	SOIC
LVPECL	No	Yes	SN65LVDS101DGK	AZM	MSOP
LVPECL	Yes	No	SN65LVDT101D	DE101	SOIC
LVPECL	Yes	No	SN65LVDT101DGK	BAF	MSOP

(1) Add the suffix R for taped and reeled carrier (i.e. SN65LVDS100DR).

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range unless otherwise noted

				UNIT
V_{CC}	Supply voltage range(2)			–0.5 V to 4 V
I_{BB}	V_{BB} Output current			±0.5 mA
V_I	Voltage range, (A, B, Y, Z)			0 V to 4.3 V
V_O				
V_{ID}	Differential voltage, $\|V_A – V_B\|$ ('LVDT100 and 'LVDT101 only)			1 V
ESD		Human Body Model(3)	A, B, Y, Z, and GND	±5 kV
			All pins	±2 kV
		Charged-Device Model(4)	All pins	±1500 V
P_D	Continuous power dissipation			See Dissipation Rating Table

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.7.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

POWER DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
DGK	377 mW	3.8 mW/°C	151 mW
D	481 mW	4.8 mW/°C	192 mW

(1) This is the inverse of the junction-to-ambient thermal resistance with no air flow installed on the JESD51-3 low effective thermal conductivity test board for leadless surface mount packages.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Magnitude of differential input voltage $\|V_{ID}\|$	'LVDS100 or 'LVDS101	0.1		1	V
	'LVDT100 or 'LVDT101	0.1		0.8	
Input voltage (any combination of common-mode or input signals), V_I		0		4	V
V_{BB} output current, $I_{O(VBB)}$		–400 (1)		12	µA
Operating free-air temperature, T_A		–40		85	°C

(1) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
I_{CC}	Supply current, 'LVDx100	No load or input		25	30	mA
	Supply current, 'LVDx101	R_L = 50 Ω to 1 V, No input		50	61	
P_D	Device power dissipation, 'LVDx100	R_L = 100 Ω, No input			110	mW
	Device power dissipation, 'LVDx101	Y and Z to V_{CC} - 2 V through 50 Ω, No input		116	142	
V_{BB}	Reference voltage output, 'LVDS100 or 'LVDS101	I_O = –400 µA or 12 µA	V_{CC}–1.4	V_{CC}–1.35	V_{CC}–1.3	mV
SN65LVDS100 and SN65LVDS101 INPUT CHARACTERISTICS (see Figure 1)						
V_{IT+}	Positive-going differential input voltage threshold	See Figure 1 and Table 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold		–100			
I_I	Input current	V_I = 0 V or 2.4 V, Second input at 1.2 V	–20		20	µA
		V_I = 4 V, Second input at 1.2 V			33	µA
$I_{I(OFF)}$	Power off input current	V_{CC} = 1.5 V, V_I = 0 V or 2.4 V, Second input at 1.2 V	–20		20	µA
		V_{CC}= 1.5 V, V_I = 4 V, Second input at 1.2 V			33	
I_{IO}	Input offset current ($\|I_{IA} - I_{IB}\|$)	$V_{IA} = V_{IB,}$ $0 \le V_{IA} \le 4$ V	–6		6	µA
C_i	Small-signall input capacitance to GND	V_I = 1.2 V		0.6		pF
SN65LVDT100 and SN65LVDT101 INPUT CHARACTERISTICS (see Figure 1)						
V_{IT+}	Positive-going differential input voltage threshold	See Figure 1 and Table 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold		–100			
I_I	Input current	V_I = 0 V or 2.4 V, Other input open	–40		40	µA
		V_I = 4 V, Other input open			66	
$I_{I(OFF)}$	Power off input current	V_{CC} = 1.5 V, V_I = 0 V or 2.4 V, Other input open	–40		40	µA
		V_{CC}= 1.5 V, V_I = 4 V, Other input open			66	
$R_{(T)}$	Differential input resistance	V_{ID} = 300 mV or 500 mV, V_{IC} = 0 V or 2.4 V	90	110	132	Ω
		V_{CC}= 0 V, V_{ID} = 300 mV or 500 mV, V_{IC} = 0 V or 2.4 V	90	110	132	
C_i	Small-signall differential input capacitance	V_I = 1.2 V		0.6		pF

(1) Typical values are with a 3.3-V supply voltage and room temperature

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
SN65LVDS100 and SN65LVDT100 OUTPUT CHARACTERISTICS (see Figure 1)						
$\|V_{OD}\|$	Differential output voltage magnitude	See Figure 2	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states		–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	150	mV
I_{OS}	Short-circuit output current	$V_{O(Y)}$ or $V_{O(Z)}$ = 0 V	–24		24	mA
$I_{OS(D)}$	Differential short-circuit output current	V_{OD} = 0 V	–12		12	mA
SN65LVDS101 and SN65LVDT101 OUTPUT CHARACTERISTICS (see Figure 1)						
V_{OH}	High-level output voltage	50 Ω to V_{CC}– 2 V, See Figure 4	V_{CC}–1.25	V_{CC}–1.02	V_{CC}–0.9	V
		V_{CC} = 3.3 V, 50-Ω load to 2.3 V	2055	2280	2405	mV
V_{OL}	Low-level output voltage	50 Ω to V_{CC} - 2 V, See Figure 4	V_{CC}–1.83	V_{CC}–1.61	V_{CC}–1.53	V
		V_{CC} = 3.3 V, 50-Ω load to 2.3 V	1475	1690	1775	mV
$\|V_{OD}\|$	Differential output voltage magnitude	50-Ω load to V_{CC}– 2 V, SeeFigure 4	475	575	750	mV

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	'LVDx100	See Figure 5	300	470	800	ps
		'LVDx101		400	630	900	
t_{PHL}	Propagation delay time, high-to-low-level output	'LVDx100		300	470	800	ps
		'LVDx100		400	630	900	
t_r	Differential output signal rise time (20%–80%)					220	ps
t_f	Differential output signal fall time (20%–80%)					220	ps
$t_{sk(p)}$	Pulse skew ($\|t_{PHL}$– $t_{PLH}\|$) (2)				5	50	ps
$t_{sk(pp)}$	Part-to-part skew(3)		V_{ID} = 0.2 V, See Figure 5			100	ps
$t_{jit(per)}$	RMS period jitter(4)		1 GHz 50% duty cycle square wave input, V_{ID} = 200 mV, V_{IC} = 1.2 V, See Figure 6		1	3.7	ps
$t_{jit(cc)}$	Peak cycle-to-cycle jitter(5)				6	23	ps
$t_{jit(pp)}$	Peak-to-peak jitter		2 GHz PRBS, 2^{23}–1 run length, V_{ID} = 200 mV, V_{IC} = 1.2 V, See Figure 6		28	65	ps
$t_{jit(det)}$	Peak-to-peak deterministic jitter(6)		2 GHz PRBS, 2^{7}–1 run length, V_{ID} = 200 mV, V_{IC} = 1.2 V, See Figure 6		17	48	ps

(1) All typical values are at 25°C and with a 3.3 V supply.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.
(3) $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay time between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) Period jitter is the deviation in cycle time of a signal with respect to the ideal period over a random sample of 1000,000 cycles.
(5) Cycle-to-cycle jitter is the variation in cycle time of a signal between adjacent cycles, over a random sample of 1,000 adjacent cycle pairs.
(6) Deterministic jitter is the sum of pattern-dependent jitter and pulse-width distortion.

PARAMETER MEASUREMENT INFORMATION

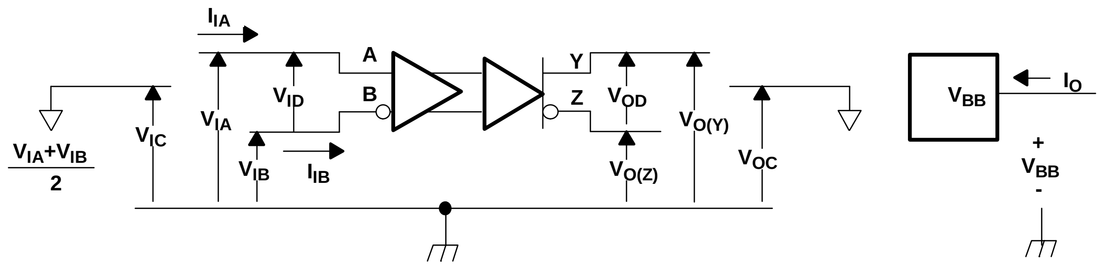


Figure 1. Voltage and Current Definitions

Table 1. Receiver Input Voltage Threshold Test

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	OUTPUT(1)
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
1.25 V	1.15 V	100 mV	1.2 V	H
1.15 V	1.25 V	–100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	H
3.9 V	4. 0 V	–100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.05 V	H
0.0 V	0.1 V	–100 mV	0.05 V	L
1.7 V	0.7 V	1000 mV	1.2 V	H
0.7 V	1.7 V	–1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	H
3.0 V	4.0 V	–1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	H
0.0 V	1.0 V	–1000 mV	0.5 V	L

(1) H = high level, L = low level

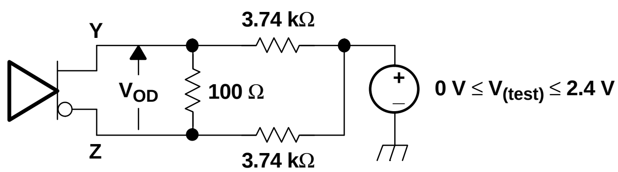
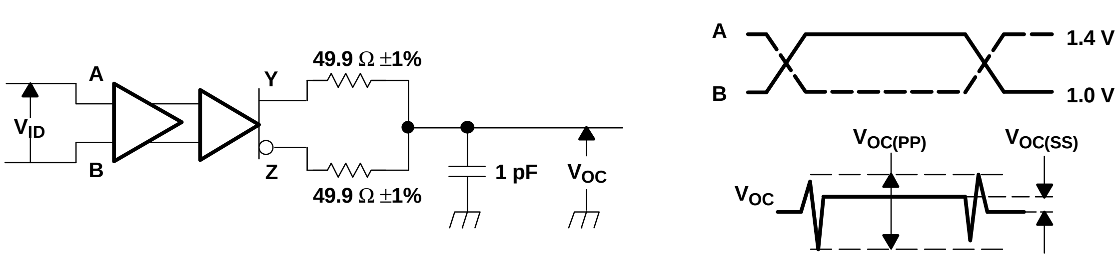


Figure 2. SN65LVDx100 Differential Output Voltage (V_{OD}) Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 0.25 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the SN65LVDx100 Driver Common-Mode Output Voltage

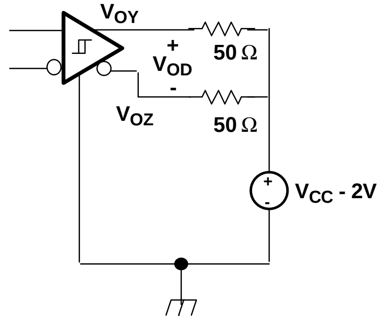
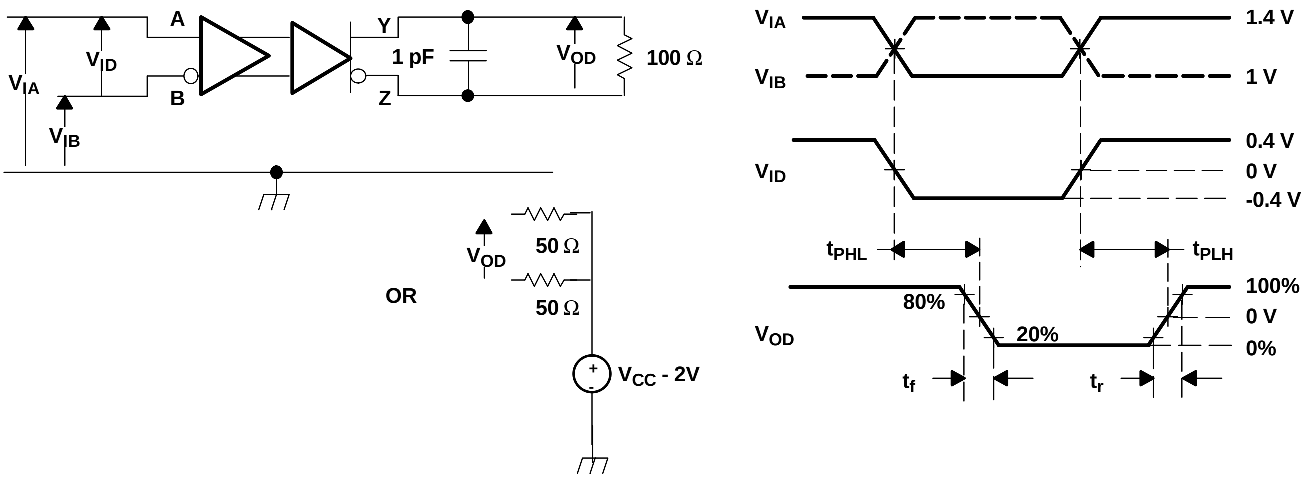


Figure 4. Typical Termination for LVPECL Output Driver (65LVDx101)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 0.25$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. Measurement equipment provides a bandwidth of 5 GHz minimum.

Figure 5. Timing Test Circuit and Waveforms

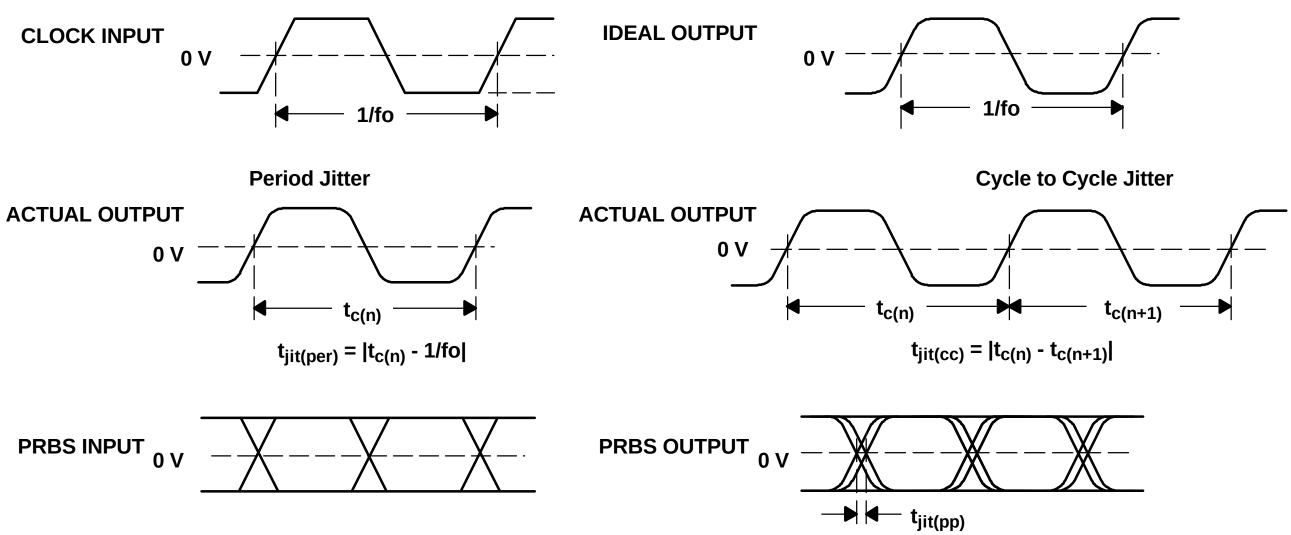
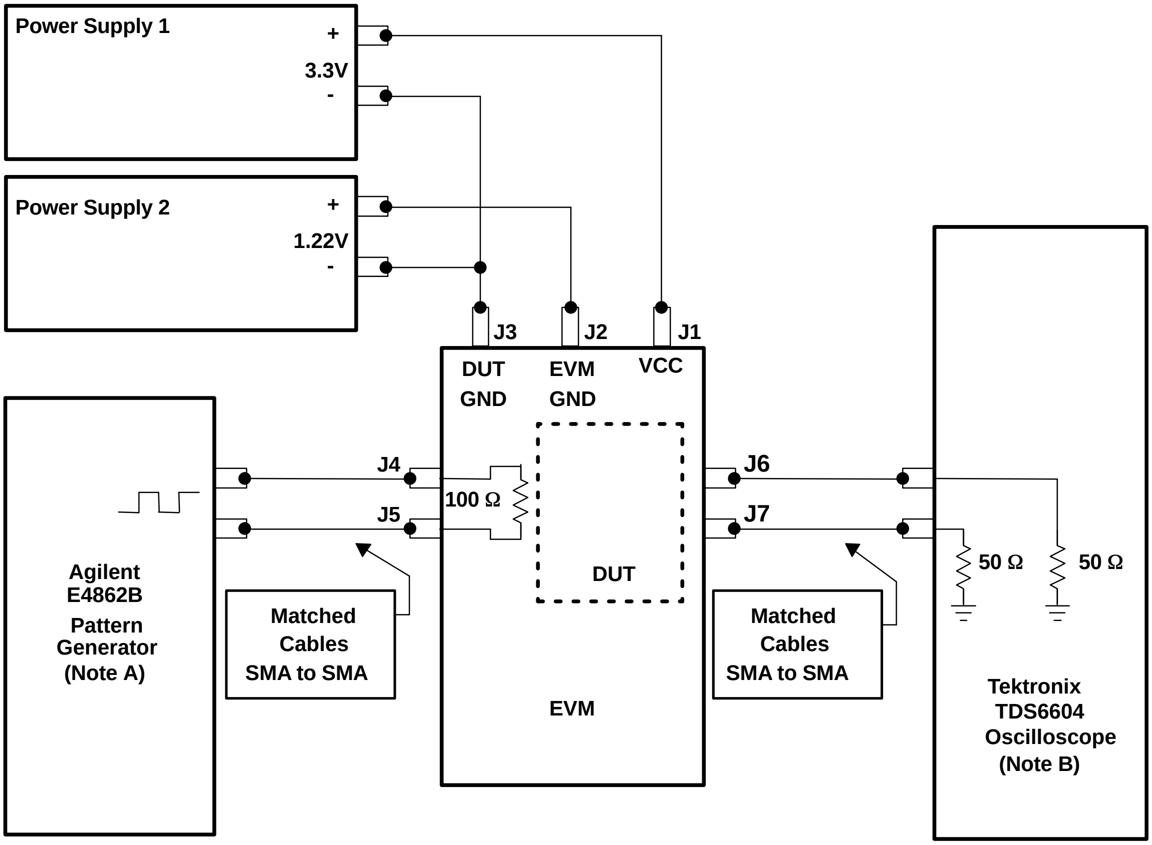


Figure 6. Driver Jitter Measurement Waveforms



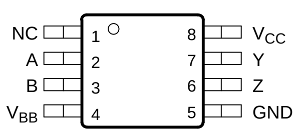
A. Source jitter is subtracted from the measured values.

B. TDS JIT3 jitter analysis software installed

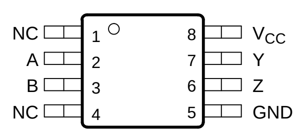
Figure 7. Jitter Setup Connections for SN65LVDS100 and SN65LVDS101

PIN ASSIGNMENTS

SN65LVDS100 and SN65LVDS101
D AND DGK PACKAGE
(TOP VIEW)



SN65LVDT100 and SN65LVDT101
D AND DGK PACKAGE
(TOP VIEW)



NC = Not Connected

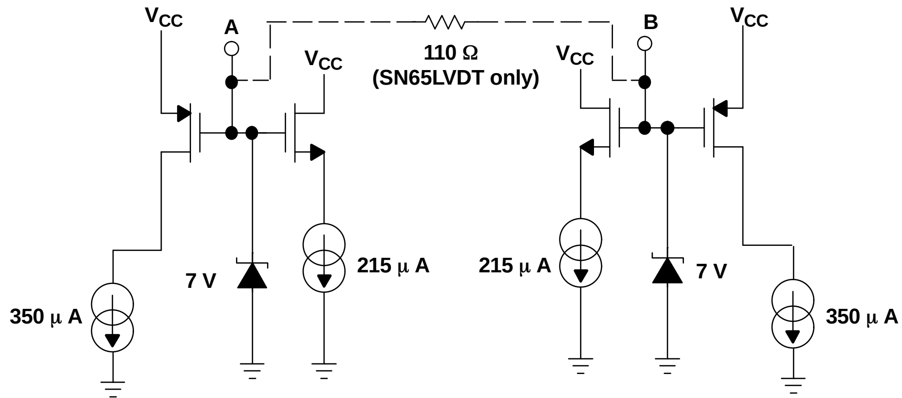
FUNCTION TABLE

DIFFERENTIAL INPUT	OUTPUTS(1)	
$V_{ID} = V_A - V_B$	Y	Z
$V_{ID} \geq 100$ mV	H	L
–100 mV < V_{ID} < 100 mV	?	?
$V_{ID} \leq -100$ mV	L	H
Open	?	?

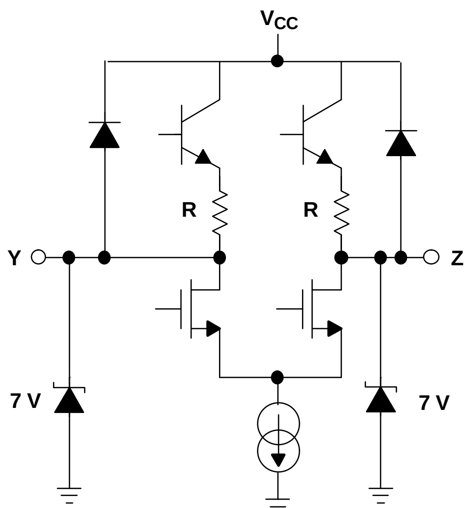
(1) H = high level, L = low level, ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

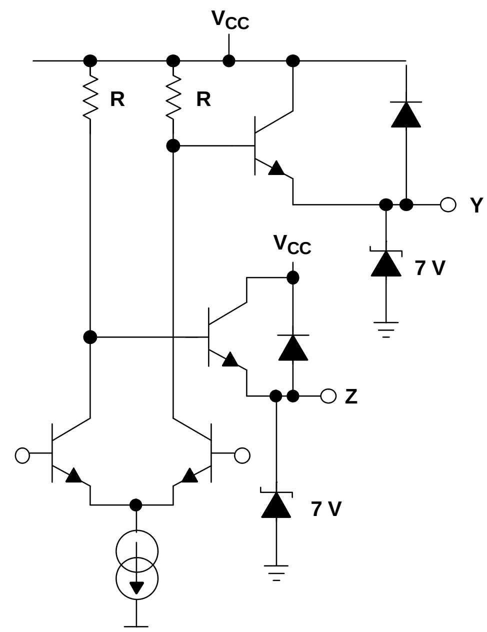
INPUT



OUTPUT
(SN65LVDS100 and SN65LVDT100)



OUTPUT
(SN65LVDS101 and SN65LVDT101)



TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

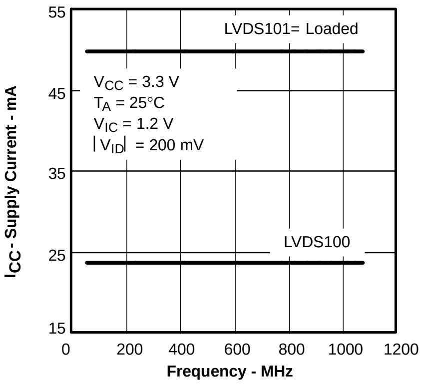


Figure 8.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

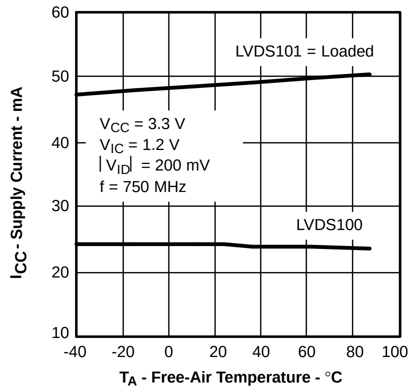


Figure 9.

DIFFERENTIAL OUTPUT VOLTAGE vs FREQUENCY

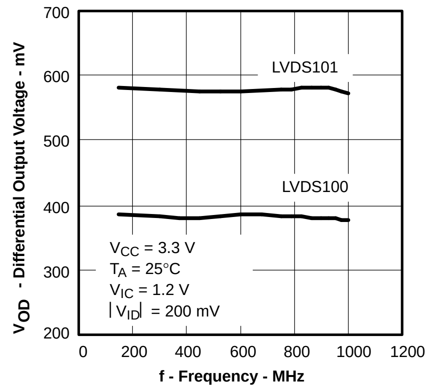


Figure 10.

SN65LVDS100 PROPAGATION DELAY TIME vs COMMON-MODE INPUT VOLTAGE

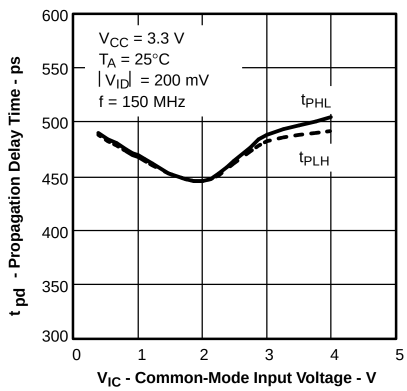


Figure 11.

SN65LVDS101 PROPAGATION DELAY TIME vs COMMON-MODE INPUT VOLTAGE

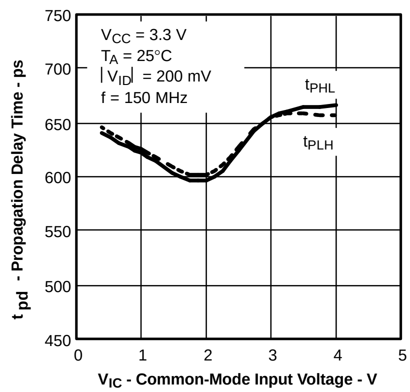


Figure 12.

SN65LVDS100 PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

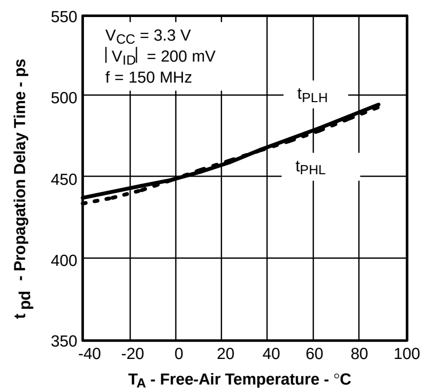


Figure 13.

SN65LVDS101 PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

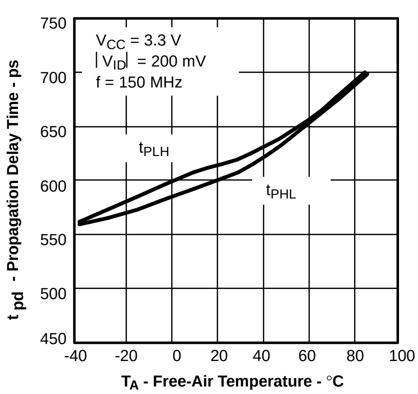


Figure 14.

SN65LVDS100 PEAK-TO-PEAK JITTER vs FREQUENCY

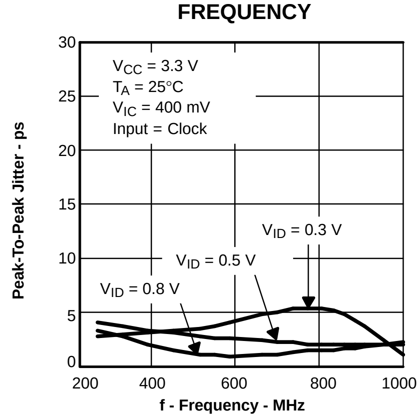


Figure 15.

SN65LVDS100 PEAK-TO-PEAK JITTER vs DATA RATE

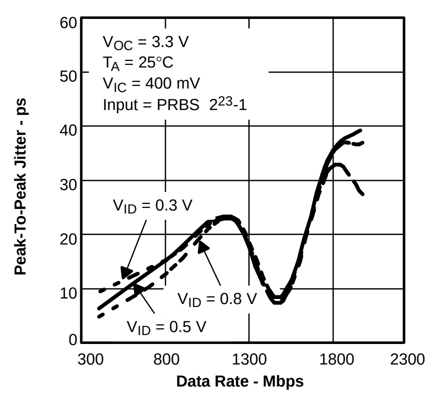


Figure 16.

TYPICAL CHARACTERISTICS (continued)

SN65LVDS101 PEAK-TO-PEAK JITTER vs FREQUENCY

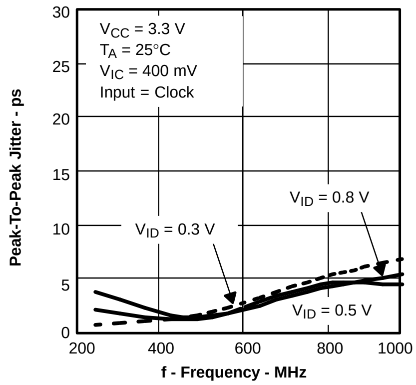


Figure 17.

SN65LVDS101 PEAK-TO-PEAK JITTER vs DATA RATE

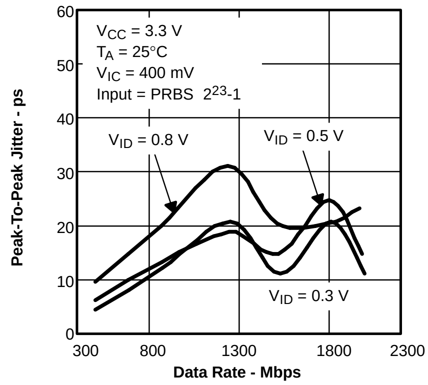


Figure 18.

SN65LVDS100 PEAK-TO-PEAK JITTER vs FREQUENCY

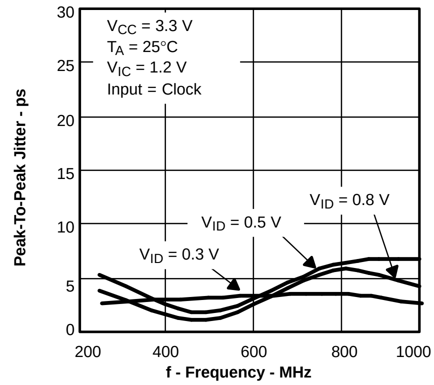


Figure 19.

SN65LVDS100 PEAK-TO-PEAK JITTER vs DATA RATE

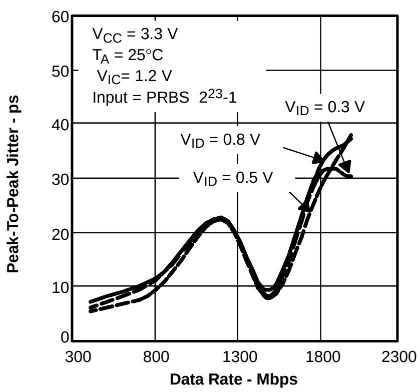


Figure 20.

SN65LVDS101 PEAK-TO-PEAK JITTER vs FREQUENCY

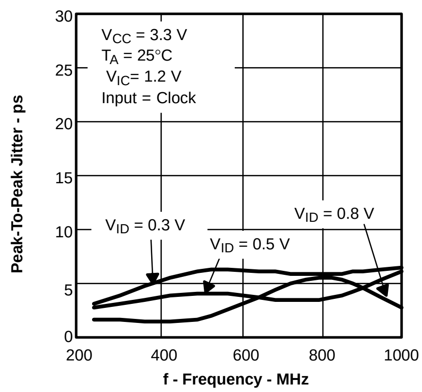


Figure 21.

SN65LVDS101 PEAK-TO-PEAK JITTER vs DATA RATE

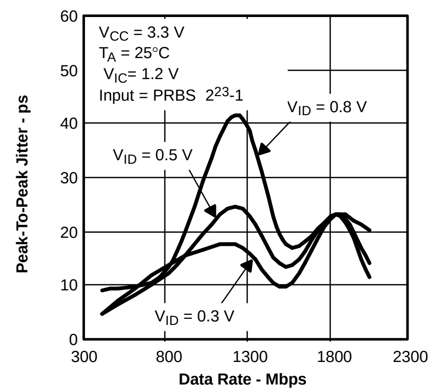


Figure 22.

SN65LVDS100 PEAK-TO-PEAK JITTER vs FREQUENCY

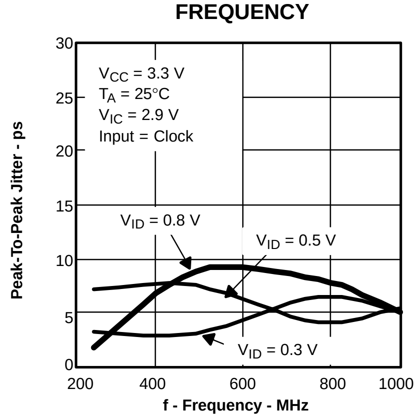


Figure 23.

SN65LVDS100 PEAK-TO-PEAK JITTER vs DATA RATE

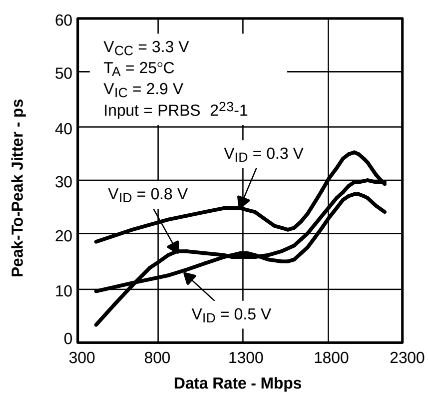


Figure 24.

SN65LVDS101 PEAK-TO-PEAK JITTER vs FREQUENCY

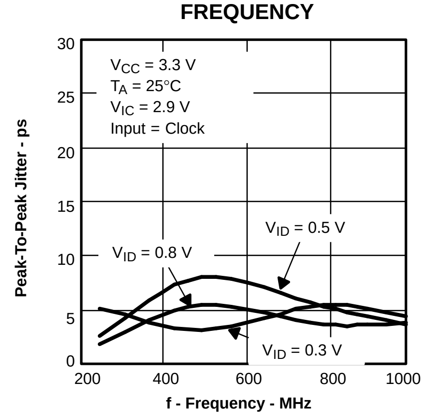


Figure 25.

TYPICAL CHARACTERISTICS (continued)

**SN65LVDS101
PEAK-TO-PEAK JITTER
vs
DATA RATE**

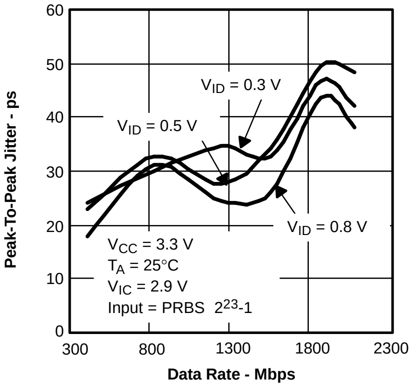


Figure 26.

**SN65LVDS100
PEAK-TO-PEAK JITTER
vs
FREE-AIR TEMPERATURE**

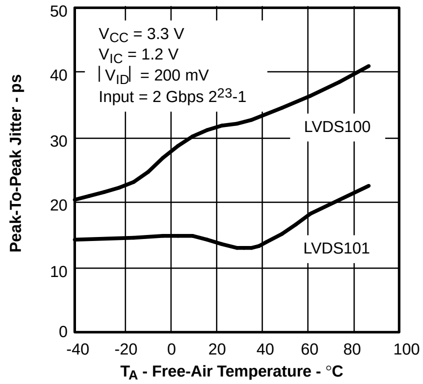


Figure 27.

**SN65LVDS100
DIFFERENTIAL OUTPUT VOLTAGE
vs
FREQUENCY**

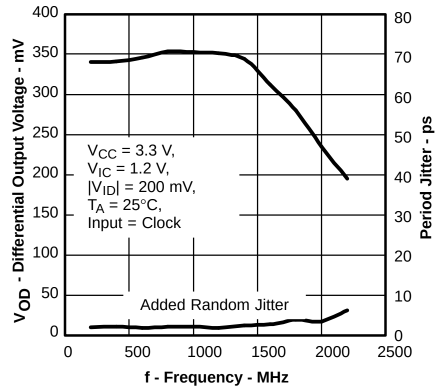


Figure 28.

**SN65LVDS100
PEAK-TO-PEAK JITTER
vs
DATA RATE**

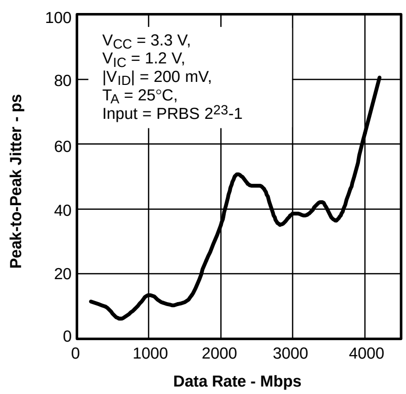


Figure 29.

**SN65LVDS101
DIFFERENTIAL OUTPUT VOLTAGE
vs
FREQUENCY**

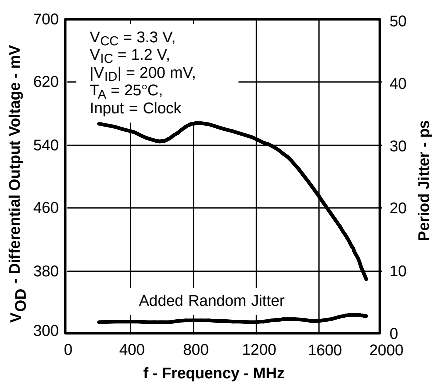


Figure 30.

**SN65LVDS101
PEAK-TO-PEAK JITTER
vs
DATA RATE**

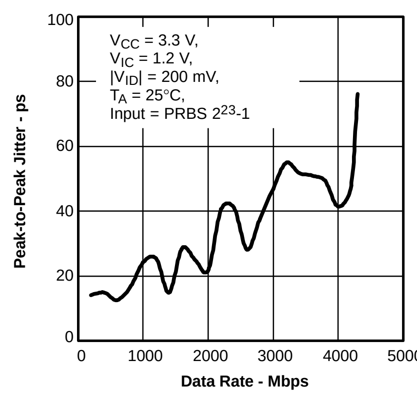
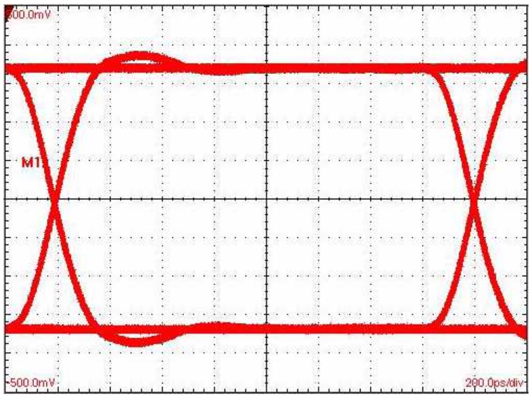


Figure 31.

TYPICAL CHARACTERISTICS (continued)

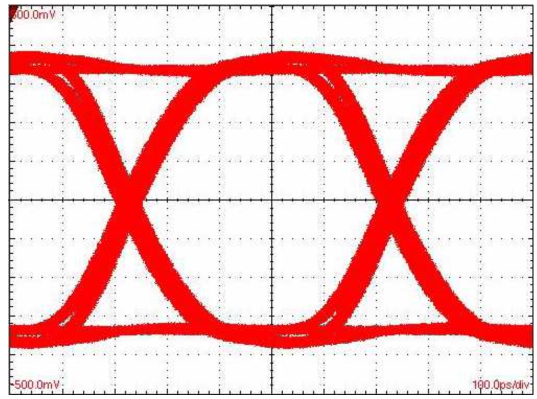
SN65LVDS100
622 Mbps, 2^{23}– 1 PRBS



Horizontal Scale= 200 ps/div
LVPECL-to-LVDS

Figure 32.

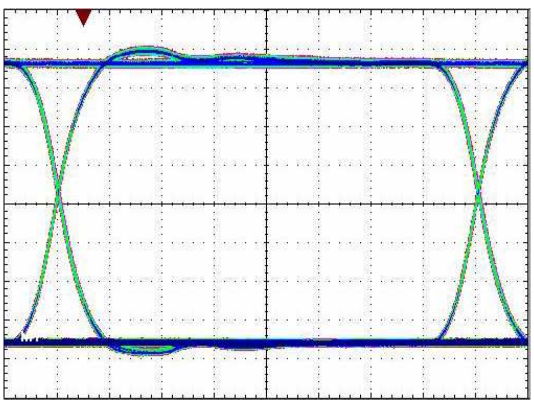
SN65LVDS100
2 Gbps, 2^{23}– 1 PRBS



Horizontal Scale= 100 ps/div
LVPECL-to-LVDS

Figure 33.

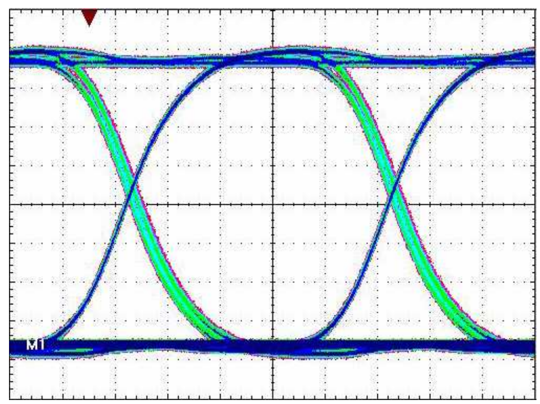
SN65LVDS101
622 Mbps, 2^{23}– 1 PRBS



Horizontal Scale= 200 ps/div
LVDS-to-LVPECL

Figure 34.

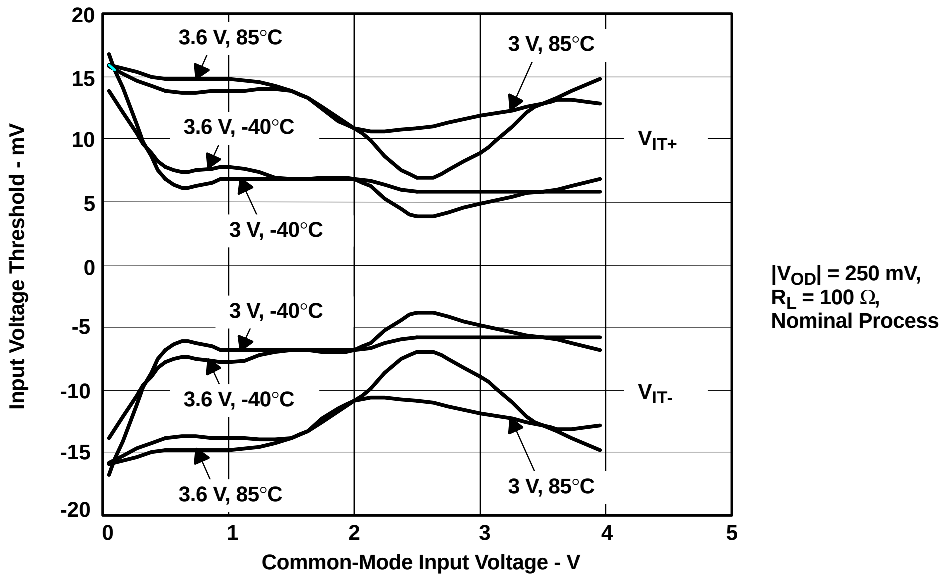
SN65LVDS101
2 Gbps, 2^{23}– 1 PRBS



Horizontal Scale= 100 ps/div
LVDS-to-LVPECL

Figure 35.

TYPICAL CHARACTERISTICS (continued)



NOTE: V_{IT} is a steady-state parameter. The switching time is influenced by the input overdrive above this steady-state threshold up to a differential input voltage magnitude of 100 mV.

Figure 36. SN65LVDS100 Simulated Input Voltage Threshold vs Common-Mode Input Voltage, Supply Voltage, and Temperature

APPLICATION INFORMATION

The SN65LVDS100, SN65LVDT100, SN65LVDS101, and SN65LVDT101 inputs will detect a 100-mV difference between any two signals between 0 V and 4 V, This range will allow receipt of many different single-ended and differential signals. Following are some of the more common connections.

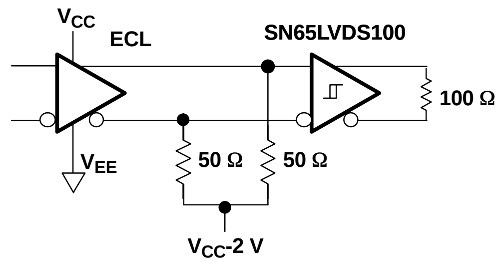


Figure 37. PECL-to-LVDS Translation

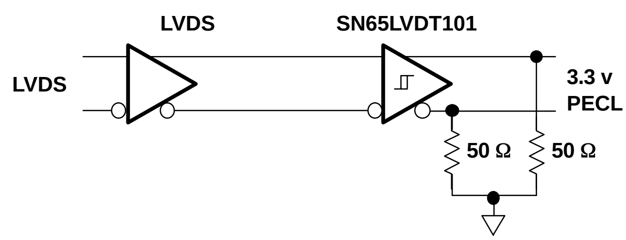


Figure 38. LVDS-to-3.3 V PECL Translation

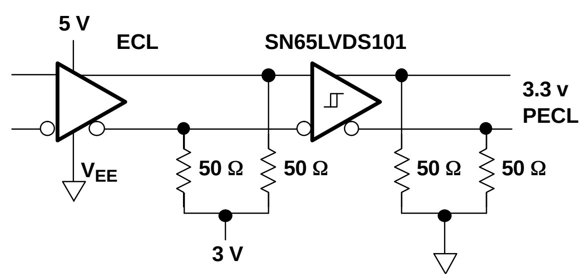


Figure 39. 5-V PECL to 3.3-V PECL Translation

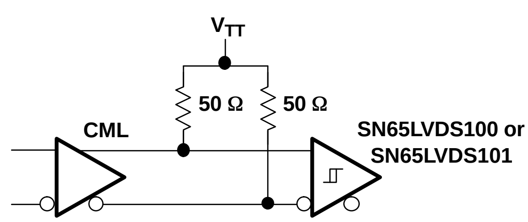


Figure 40. CML-to-LVDS or 3.3-V PECL Translation

APPLICATION INFORMATION (continued)

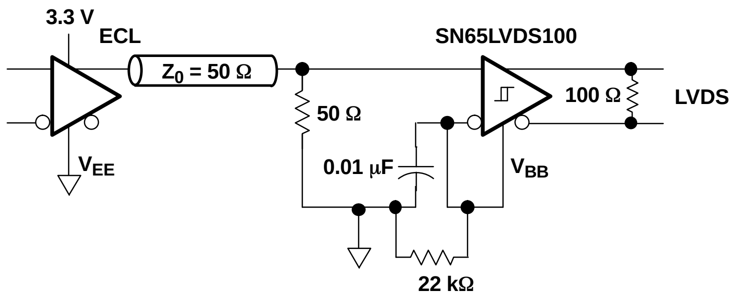


Figure 41. Single-Ended 3.3-V PECL-to-LVDS Translation

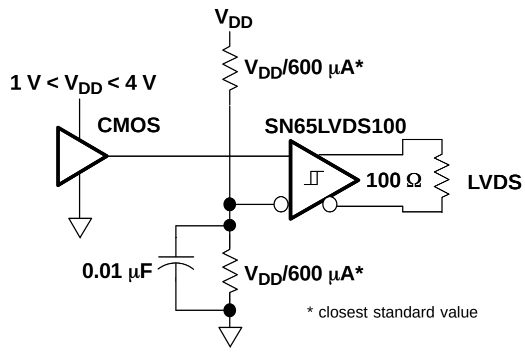


Figure 42. Single-Ended CMOS-to-LVDS Translation

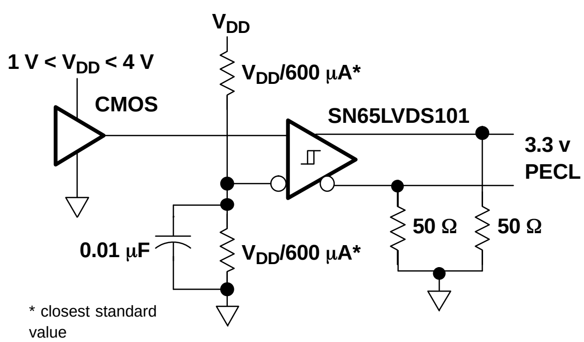


Figure 43. Single-Ended CMOS-to-3.3-V PECL Translation

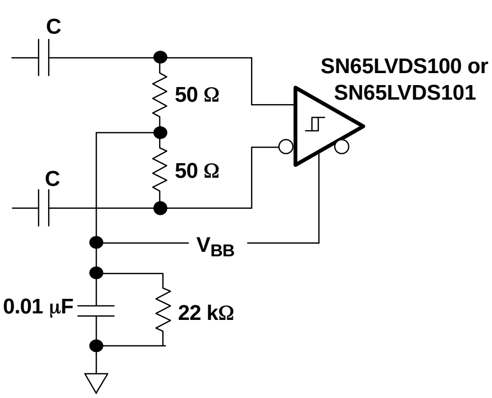


Figure 44. Receipt of AC-Coupled Signals

APPLICATION INFORMATION (continued)

FAILSAFE CONSIDERATIONS

Failsafe, in regard to a line receiver, usually means that the output goes to a defined logical state with no input signal. To keep added jitter to an absolute minimum, the SN65LVDS100 does not include this feature. It does exhibit 25 mV of input voltage hysteresis to prevent oscillation and keep the output in the last state prior to input-signal loss (assuming the differential noise in the system is less than the hysteresis).

Should failsafe be required, it may be added externally with a 1.6-kΩ pull-up resistor to the 3.3-V supply and a 1.6-kΩ pull-down resistor to ground as shown in Figure 45 The default output state is determined by which line is pulled up or down and is the user's choice. The location of the 1.6-kΩ resistors is not critical. However the 100-Ω resistor should be located at the end of the transmission line.

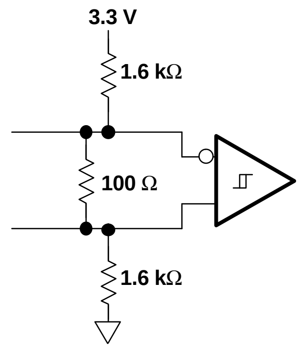


Figure 45. External Failsafe Circuit

Addition of this external failsafe will reduce the differential noise margin and add jitter to the output signal. The roughly 100-mV steady-state voltage generated across the 100-Ω resistor adds (or subtracts) from the signal generated by the upstream line driver. If the line driver's differential output is symmetrical about zero volts, then the input at the receiver will appear asymmetrical with the external failsafe. Perhaps more important, is the extra time it takes for the input signal to overcome the added failsafe offset voltage.

In Figure 46 and using an external failsafe, the high-level differential voltage at the input of the SN65LVDS100 reaches 340 mV and the low-level –400 mV indicating a 60-mV differential offset induced by the external failsafe circuitry. The figure also reveals that the lowest peak-to-peak time jitter does not occur at zero-volt differential (the nominal input threshold of the receiver) but at –60 mV, the failsafe offset.

The added jitter from external failsafe increases as the signal transition times are slowed by cable effects. When a ten-meter CAT-5 UTP cable is introduced between the driver and receiver, the zero-crossing peak-to-peak jitter at the receiver output adds 250 ps when the external failsafe is added with this specific test set up. If external failsafe is used in conjunction with the SN65LVDS100, the noise margin and jitter effects should be budgeted.

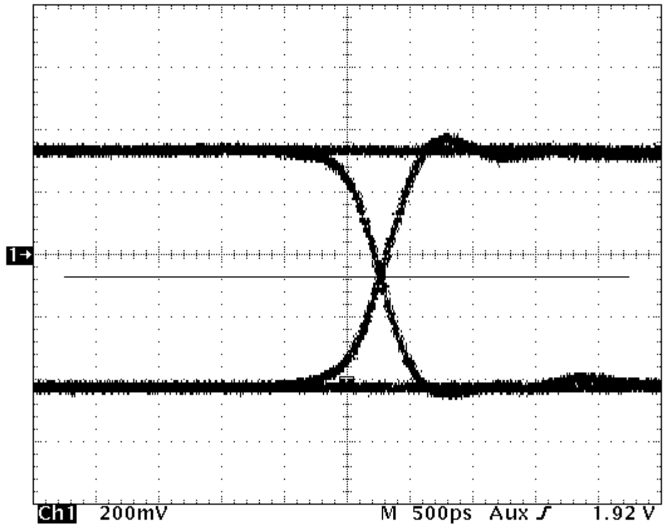
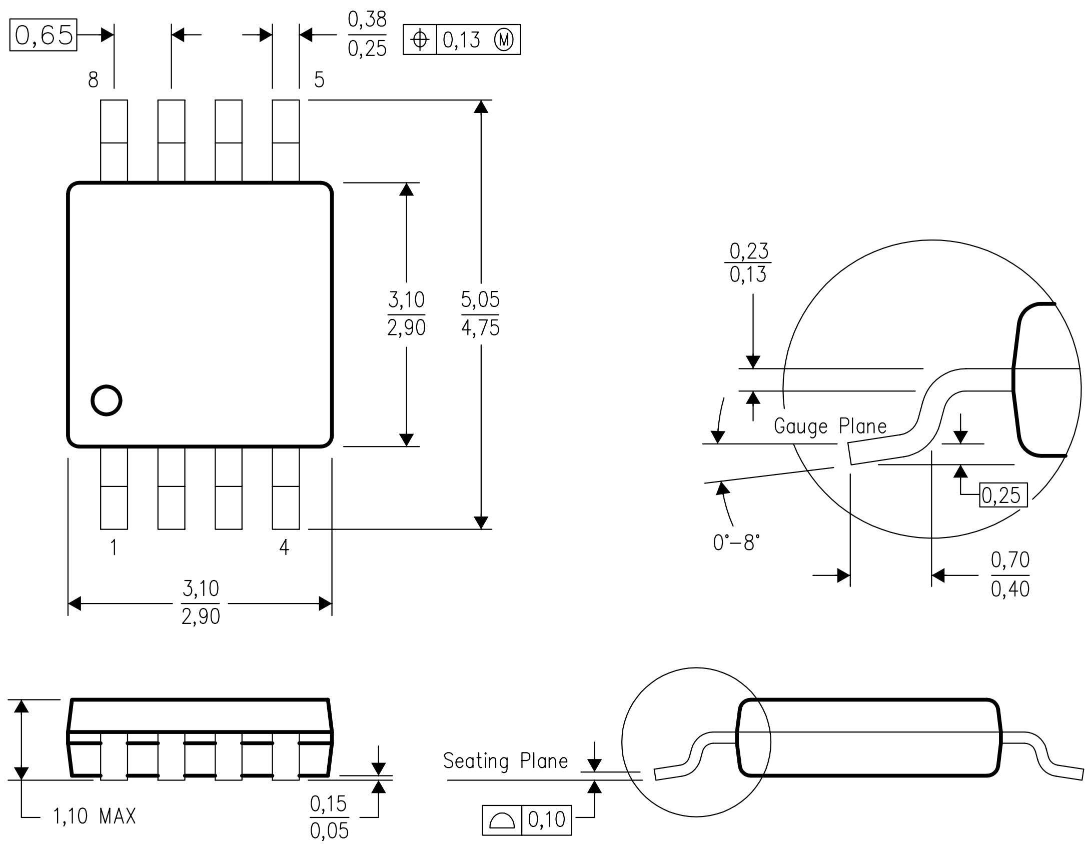


Figure 46. Receiver Input Eye Pattern With External Failsafe

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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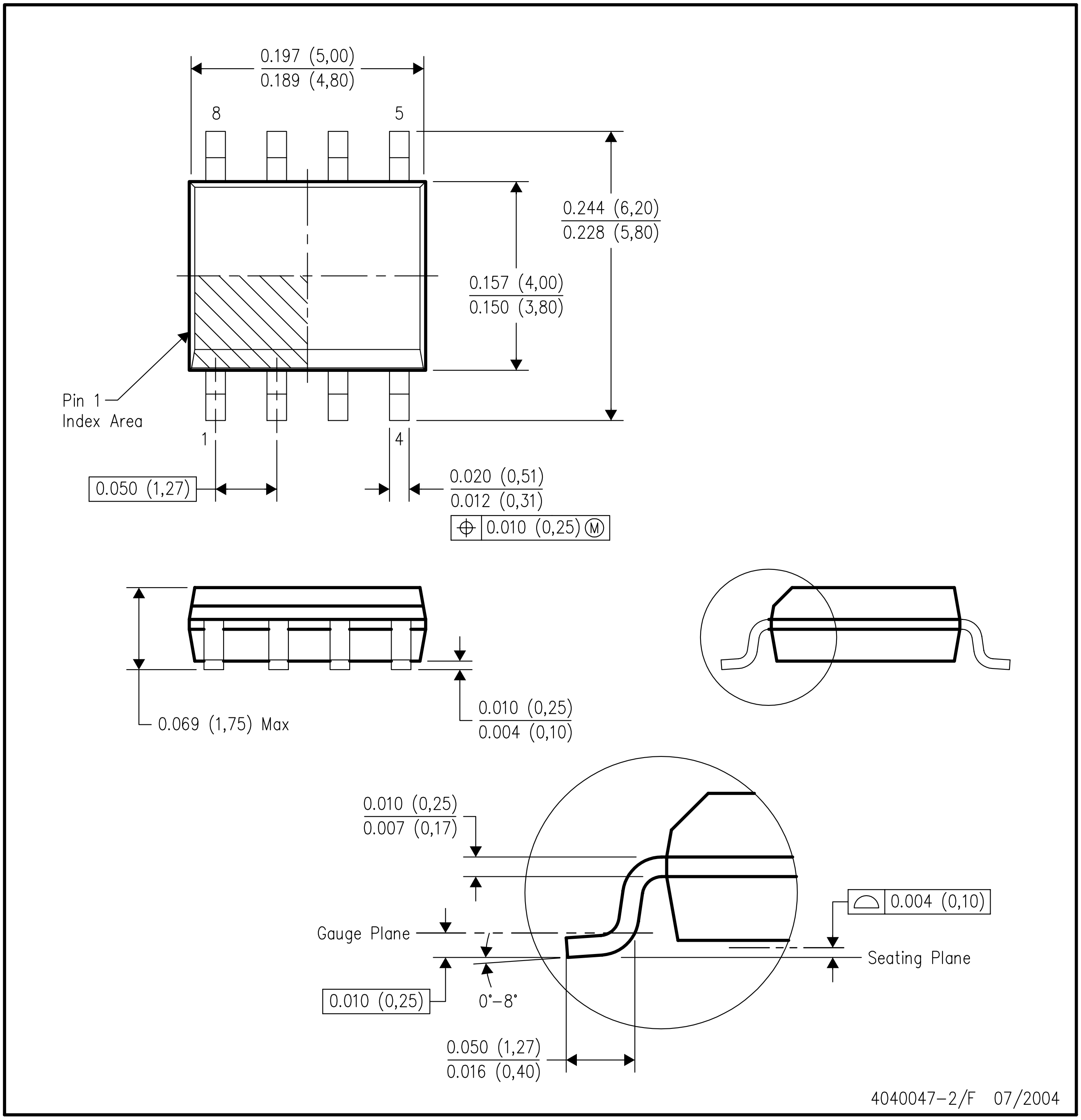
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation AA.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–012 variation AA.

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