- **Meets or Exceeds the Requirements of ANSI EIA/TIA-644 Standard for Signaling Rates† Up to 400 Mbps**
- **Operates With a Single 3.3 V Supply**
- **–2 V to 4.4 V Common-Mode Input Voltage Range**
- **Differential Input Thresholds <50 mV With 50 mV of Hysteresis Over Entire Common-Mode Input Voltage Range**
- **Integrated 110Ω Line Termination Resistors Offered With the LVDT Series**
- **Propagation Delay Times 4 ns (typ)**
- **Open-Circuit and Terminated Fail Safe Assures a High-Level Output With No Input**
- **Bus-Pin ESD Protection Exceeds 15 kV HBM**
- **Outputs High-Impedance With V_{CC} < 1.5 V**
- **Power Dissipation <400 mW With Four Receivers Switching at 200 MHz**
- **Available in Small-Outline Package With 1,27 mm Terminal Pitch**
- **Pin-Compatible With the AM26LS32, MC3486, or uA9637**

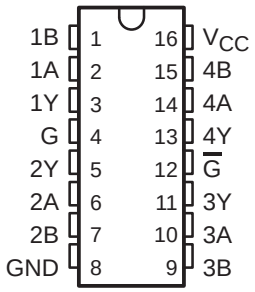
description

This family of differential line receivers offer improved performance and features that implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS is defined in the TIA/EIA-644 standard. This improved performance represents the second generation of receiver products for this standard providing a better overall solution for the cabled environment. The next generation family of products is an extension to TI's overall product portfolio and is not necessarily a replacement for older LVDS receivers.

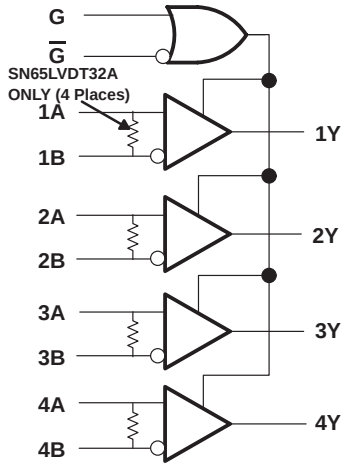
Improved features include an input common-mode voltage range 2 V wider than the minimum required by the standard. This will allow longer cable lengths by tripling the allowable ground noise tolerance to 3 V between a driver and receiver.

SN65LVDS32A
SN65LVDT32A

D PACKAGE
(TOP VIEW)

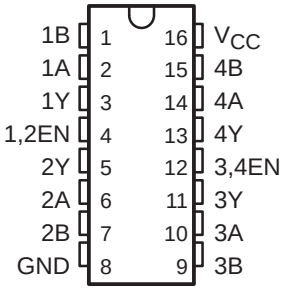


Logic Diagram
(positive logic)

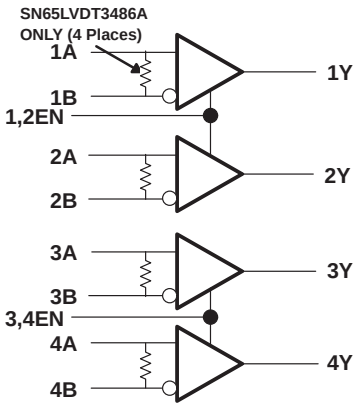


SN65LVDS3486A
SN65LVDT3486A

D PACKAGE
(TOP VIEW)

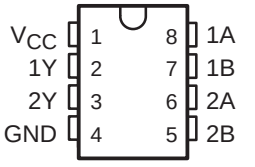


Logic Diagram
(positive logic)

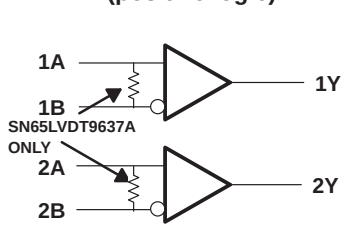


SN65LVDS9637A
SN65LVDT9637A

D PACKAGE
(TOP VIEW)



Logic Diagram
(positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† Signaling rate, 1/t, where t is the minimum unit interval and is expressed in the units bits/s (bits per second)

description (continued)

Precise control of the differential input voltage thresholds now allows for inclusion of 50 mV of input voltage hysteresis to improve noise rejection on slowly changing input signals. The input thresholds are still no more than ±50 mV over the full input common-mode voltage range. See *Application Information* for more details on this feature.

The high-speed switching of LVDS signals almost always necessitates the use of a line impedance matching resistor at the receiving-end of the cable or transmission media. The SN65LVDT series of receivers eliminates this external resistor by integrating it with the receiver. The nonterminated SN65LVDS series is also available for multidrop or other termination circuits.

The receivers can withstand ±15 kV human-body model (HBM) and ±600 V machine model (MM) electrostatic discharges to the receiver input pins with respect to ground without damage. This provides reliability in cabled and other connections where potentially damaging noise is always a threat.

The receivers also include a (patent pending) fail-safe circuit that will provide a high-level output within 500 ns after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or powered-down transmitters. This prevents noise from being received as valid data under these fault conditions. This feature may also be used for wired-OR bus signaling.

The intended application of these devices and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS32A, SN65LVDT32A, SN65LVDS3486A, SN65LVDT3486A, SN65LVDS9637A, and SN65LVDT9637A are characterized for operation from -40°C to 85°C.

Function Tables

SN65LVDS32A and SN65LVDT32A

DIFFERENTIAL INPUT	ENABLES		OUTPUT
A-B	G	$\overline{G}$	Y
$V_{ID} \geq$ -70 mV	H X	X L	H H
-100 mV < $V_{ID} \leq$ -70 mV	H X	X L	? ?
$V_{ID} \leq$ -100 mV	H X	X L	L L
X	L	H	Z
Open	H X	X L	H H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

SN65LVDS3486A and SN65LVDT3486A

DIFFERENTIAL INPUT	ENABLES	OUTPUT
A-B	EN	Y
$V_{ID} \geq$ -70 mV	H	H
-100 mV < $V_{ID} \leq$ -70 mV	H	?
$V_{ID} \leq$ -100 mV	H	L
X	L	Z
Open	H	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

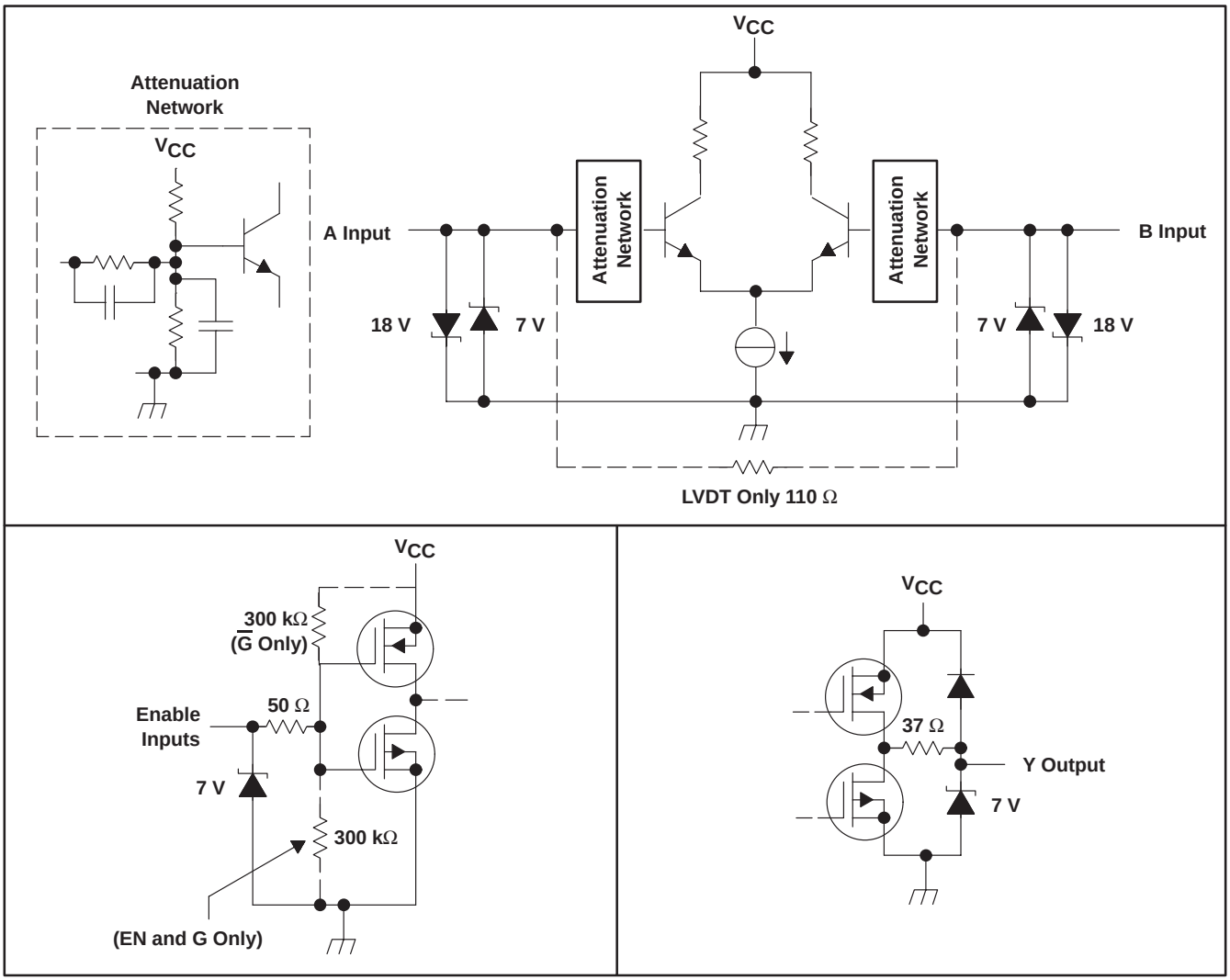
Function Tables (Continued)

SN65LVDS9637A and SN65LVDT9637A

DIFFERENTIAL INPUT	OUTPUT
A-B	Y
$V_{ID} \geq$ -70 mV	H
-100 mV < $V_{ID} \leq$ -70 mV	?
$V_{ID} \leq$ -100 mV	L
Open	H

H = high level, L = low level, ? = indeterminate

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 4 V
Voltage range: Enables or Y . . . . . –0.5 V to V_{CC} + 3 V
A or B . . . . . –4 V to 6 V
Electrostatic discharge: A, B, and GND (see Note 2) . . . . . Class 3, A: 15 kV, B: 600 V
All pins . . . . . Class 3, A: 7 kV, B: 500 V
Continuous power dissipation . . . . . See Dissipation Rating Table
Storage Temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D8	725 mW	5.8 mW/°C	377 mW
D16	950 mW	7.6 mW/°C	494 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}	Enables	2			V
Low-level input voltage, V_{IL}	Enables			0.8	V
Magnitude of differential input voltage, $\lvert V_{ID} \rvert$		0.1		3	V
Common-mode input voltage, V_{IC}		–2		4.4	V
Operating free-air temperature, T_A		–40		85	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{ITH1}	Positive-going differential input voltage threshold		V_{IB} =-2 V or 4.4 V,	See Figure 1			50	mV
V_{ITH2}	Negative-going differential input voltage threshold				–50			
V_{ITH3}	Differential input fail-safe voltage threshold		See Figure 2 and Table 1		–70		–100	mV
$V_{ID(HYS)}$	Differential input voltage hysteresis, V_{ITH1} - V_{ITH2}					50		mV
V_{OH}	High-level output voltage		I_{OH} = –8 mA		2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 8 mA				0.4	V
I_{CC}	Supply current	‘32A or ‘3486A	G or EN at V_{CC}, Steady-state	No load,		16	23	mA
			G or EN at GND			1.1	5	
		‘9637A	No load,	Steady-state		8	12	
I_I	Input current (A or B inputs)	SN65LVDS	V_I = 0 V,	Other input open			±20	µA
			V_I =2.4 V,	Other input open			±20	
			V_I =-2 V,	Other input open			±40	
			V_I = 4.4 V,	Other input open			±40	
		SN65LVDT	V_I = 0 V,	Other input open			±40	µA
			V_I =2.4 V,	Other input open			±40	
			V_I =-2 V,	Other input open			±80	
			V_I = 4.4 V,	Other input open			±80	
I_{ID}	Differential input current (I_{IA} - I_{IB})	SN65LVDS	V_{ID}= 100 mV, See Figure 1	V_{IC}= –2 V or 4.4 V,			±2	µA
		SN65LVDT	V_{ID}= 0.4 V,	V_{IC}= –2 V or 4.4 V	3.1		4.5	mA
			V_{ID}= –0.4 V,	V_{IC}= –2 V or 4.4 V	–3.1		–4.5	mA
$I_{I(OFF)}$	Power-off input current (A or B inputs)		V_A or V_B =0 or 2.4 V, V_{CC}= 0 V				±30	µA
			V_A or V_B =–2 V or 4.4 V, V_{CC}= 0 V				±50	
I_{IH}	High-level input current (enables)		V_{IH} = 2 V				10	µA
I_{IL}	Low-level input current (enables)		V_{IL} = 0.8 V				10	µA
I_{OZ}	High-impedance output current						±10	µA
C_{IN}	Input capacitance, A or B input to GND		V_I = 0.4 sin (4E6πt) + 0.5 V			5		pF

† All typical values are at 25°C and with a 3.3 V supply.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 3	2.5	4	6	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2.5	4	6	ns
t_{d1}	Delay time, fail-safe deactivate time				6.1	ns
t_{d2}	Delay time, fail-safe activate time		0.3		1	µs
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL1} - t_{PLH1} \rvert$)			200		ps
$t_{sk(o)}$	Output skew§			150		ps
$t_{sk(pp)}$	Part-to-part skew‡				1	ns
t_r	Output signal rise time			600		ps
t_f	Output signal fall time			600		ps
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 4		5.5	9	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			4.4	9	ns
t_{PZH}	Propagation delay time, high-impedance -to-high-level output			3.8	9	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			7	9	ns

† All typical values are at 25°C and with a 3.3 V supply.
‡ $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
§ $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all receivers of a single device with all of their inputs driven together.

PARAMETER MEASUREMENT INFORMATION

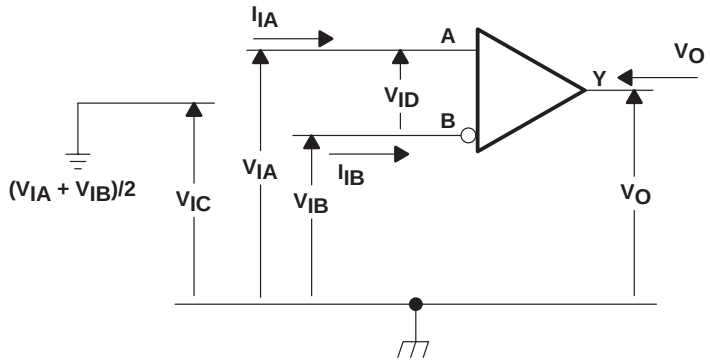


Figure 1. Voltage and Current Definitions

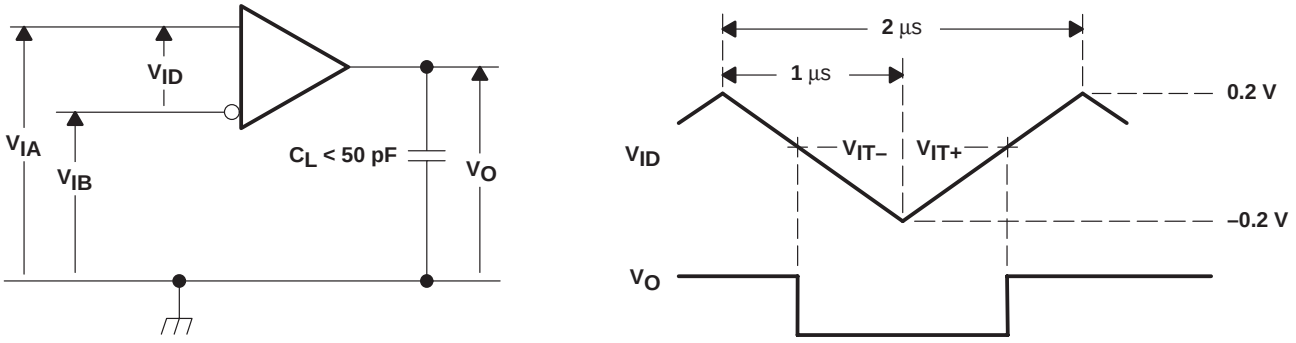


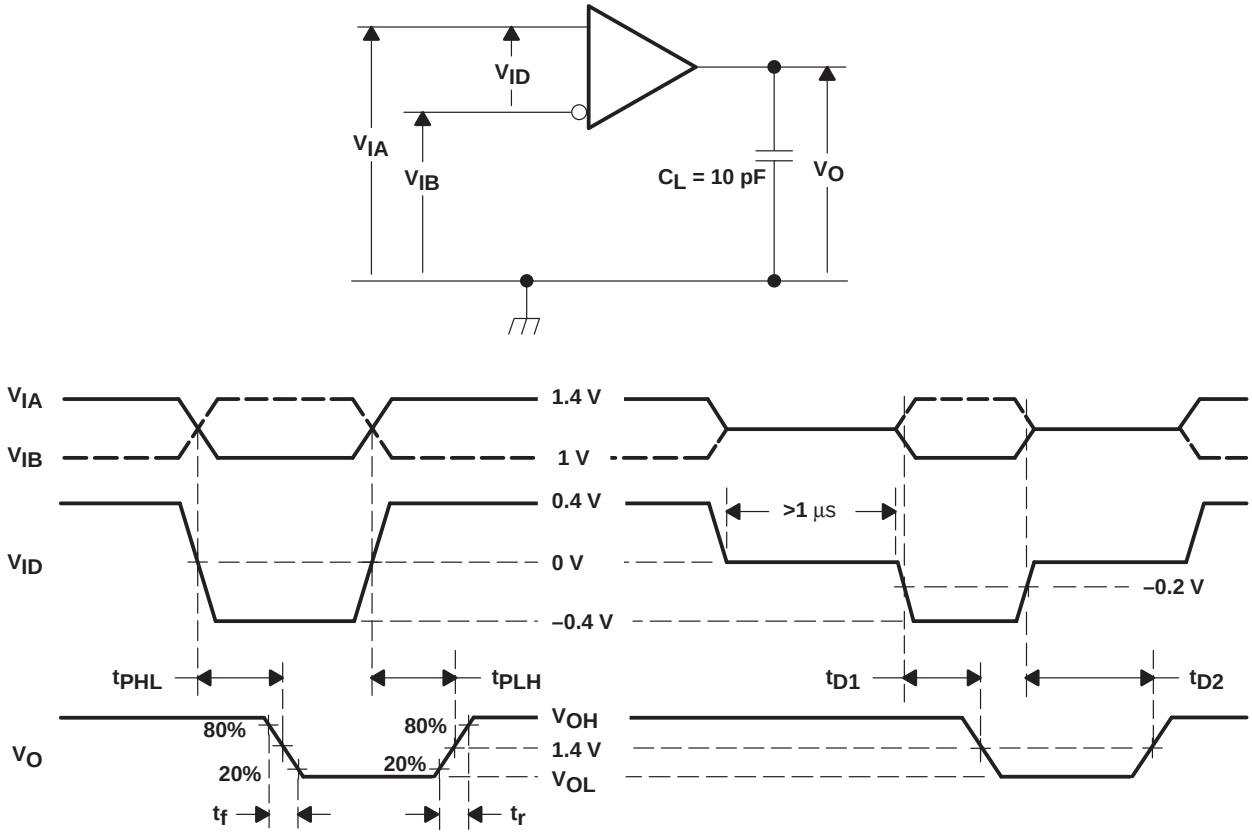
Figure 2. V_{ITH3} Input Voltage Threshold Test Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION

Table 1. Receiver Minimum and Maximum Fail-Safe Input Threshold Test Voltages

APPLIED VOLTAGES†		RESULTANT INPUTS		
V_{IA} (mV)	V_{IB} (mV)	V_{ID} (mV)	V_{IC} (mV)	Output
–2050	–1950	–100	–2000	L
–2035	–1965	–70	–2000	H
4350	4450	–100	4400	L
4365	4435	–70	4400	H

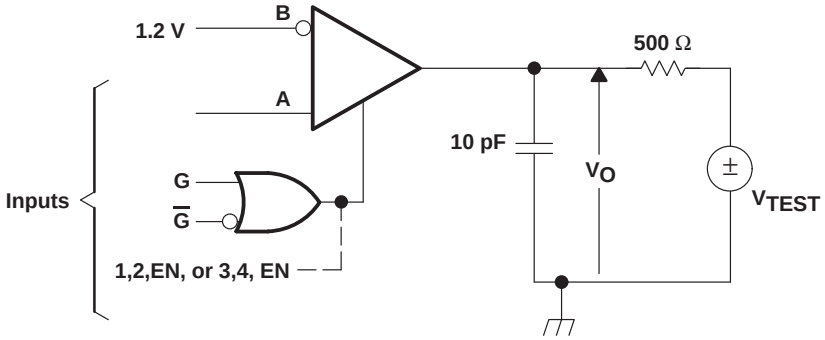
† These voltages are applied for a minimum of 1 µs.



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, Pulse Repetition Rate (PRR) = 50 Mpps, Pulsewidth = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 3. Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE B: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, Pulsewidth = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

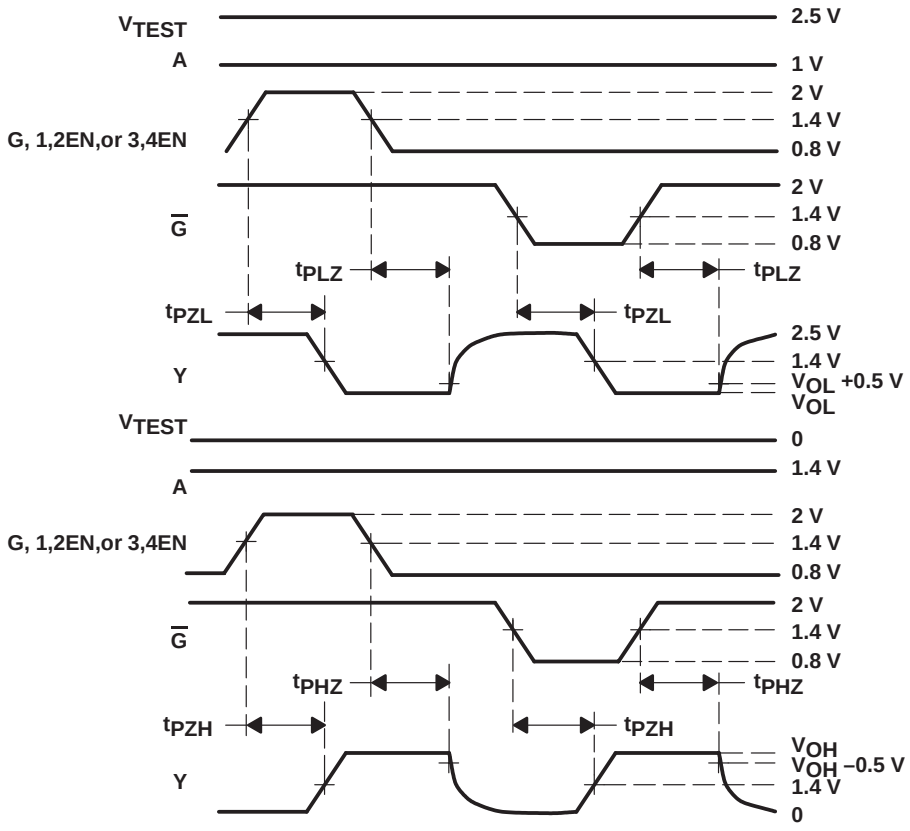


Figure 4. Enable/Disable Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

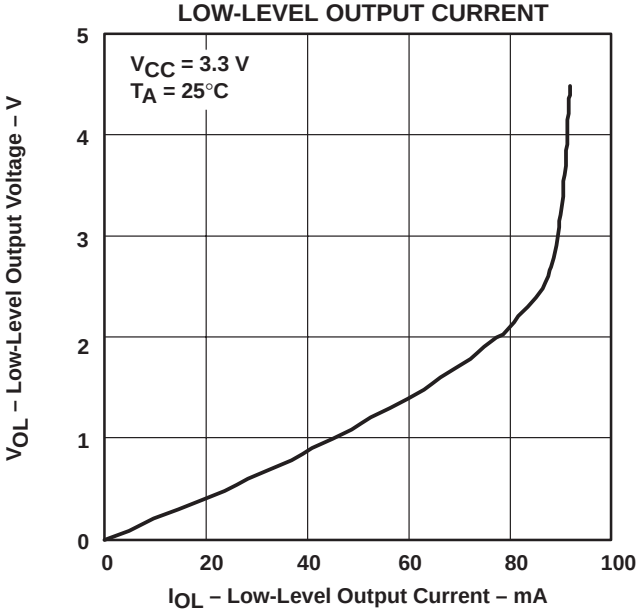


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

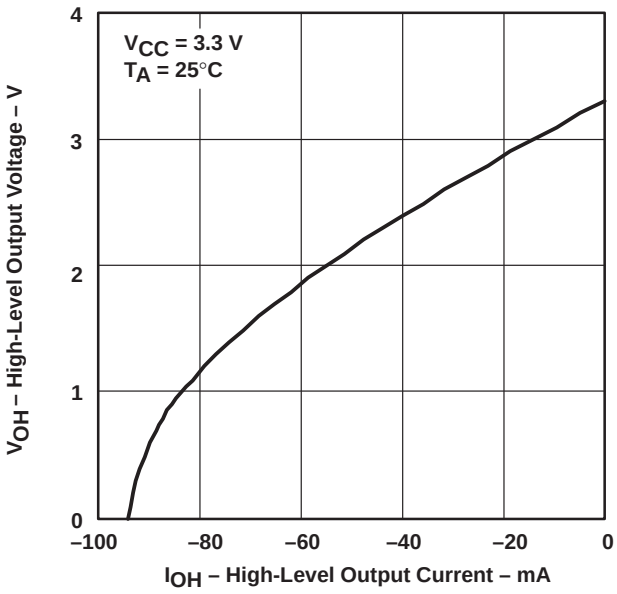


Figure 6

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

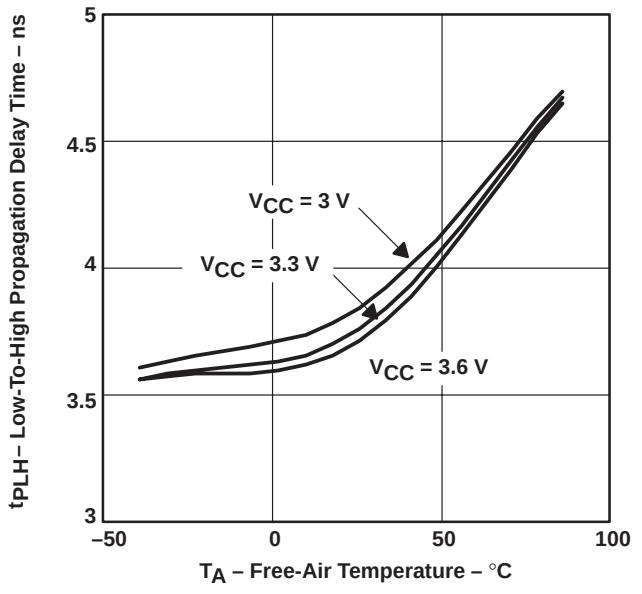


Figure 7

HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

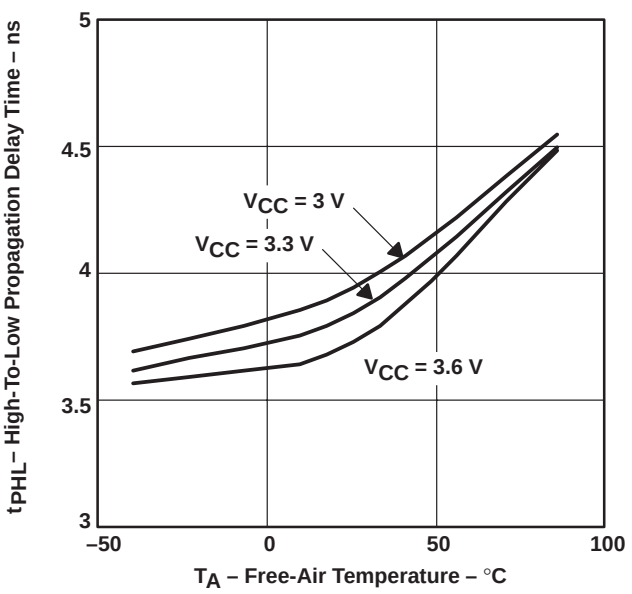


Figure 8

TYPICAL CHARACTERISTICS

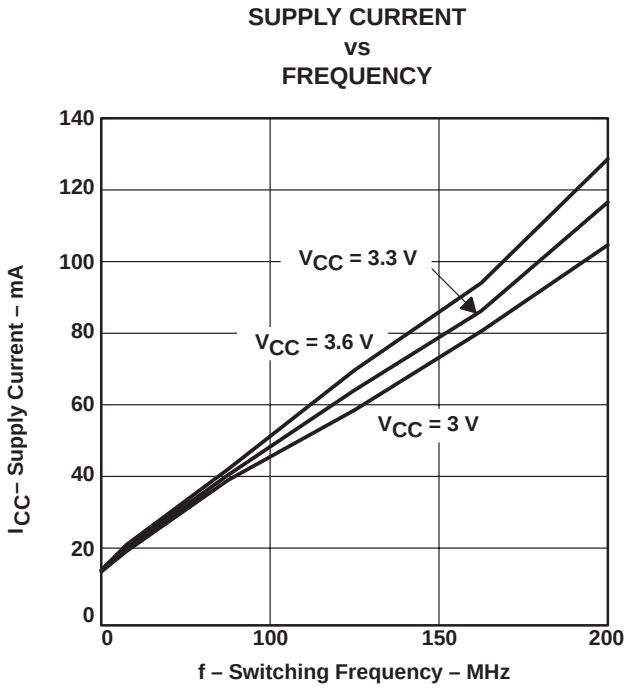
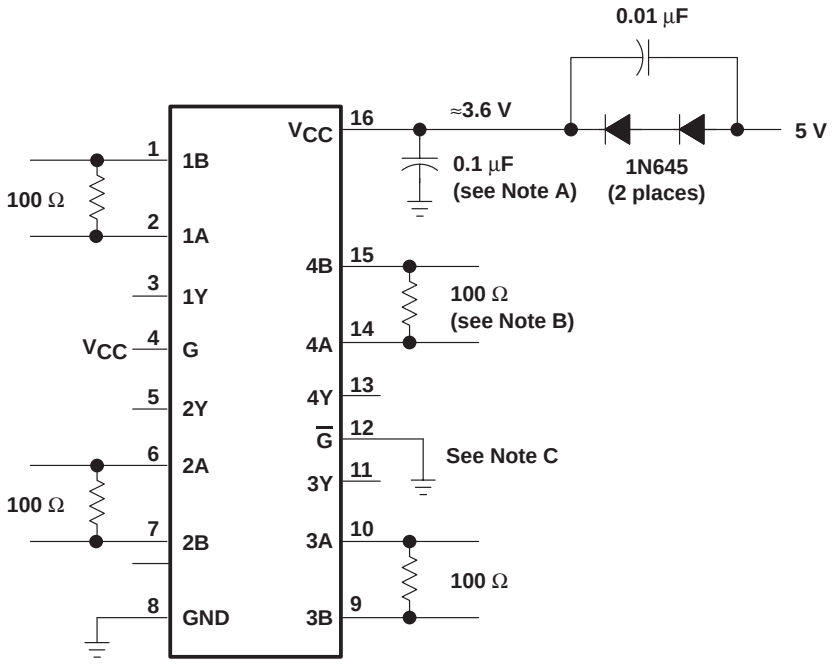


Figure 9

APPLICATION INFORMATION



NOTES: A. Place a 0.1 μF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.
B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.
C. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 10. Operation with 5-V Supply

related information

IBIS modeling is available for this device. Please contact the local TI sales office or the TI Web site at *www.ti.com* for more information.

For more application guidelines, please see the following documents:

- *Low-Voltage Differential Signalling Design Notes* (TI literature number SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (SLLA038)
- *Reducing EMI With LVDS* (SLLA030)
- *Slew Rate Control of LVDS Circuits* (SLLA034)
- *Using an LVDS Receiver With RS-422 Data* (SLLA031)
- *Evaluating the LVDS EVM* (SLLA033)

APPLICATION INFORMATION

abstract terminated failsafe

Differential data line receivers commonly have failsafe circuits to prevent the receiver from switching on input noise. This can occur when the bus driver is turned off or the interconnecting cable is damaged or left floating. This is generally solved with an external resistor network that applies a steady state bias voltage to the undriven input pins. In addition to the cost of external components, this has the effect of lowering the input magnitude thereby reducing the differential noise margin. Current Integrated solutions will not work in wired-OR or common mode termininated bus applications. The terminated failsafe circuit works over its entire extended common mode range and will ensure a known state regardless of the common mode signal present.

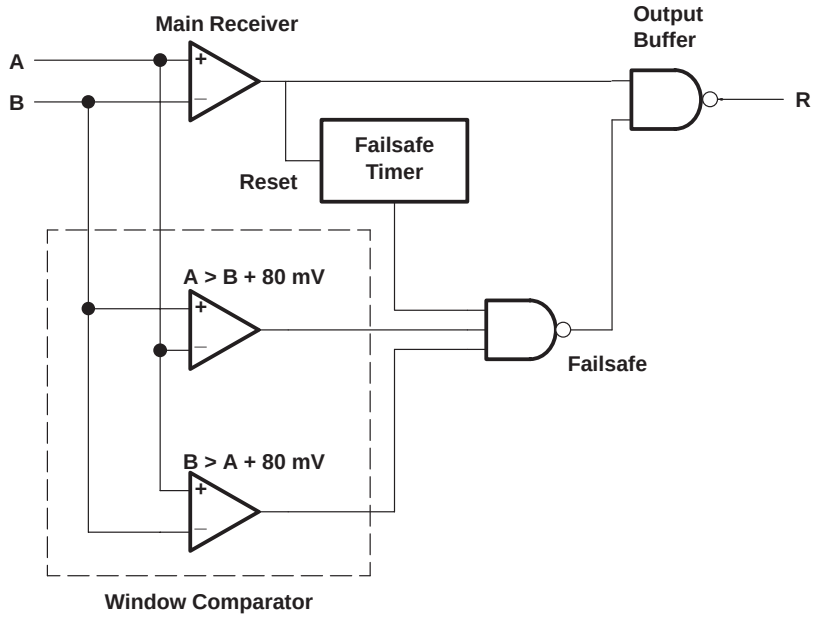
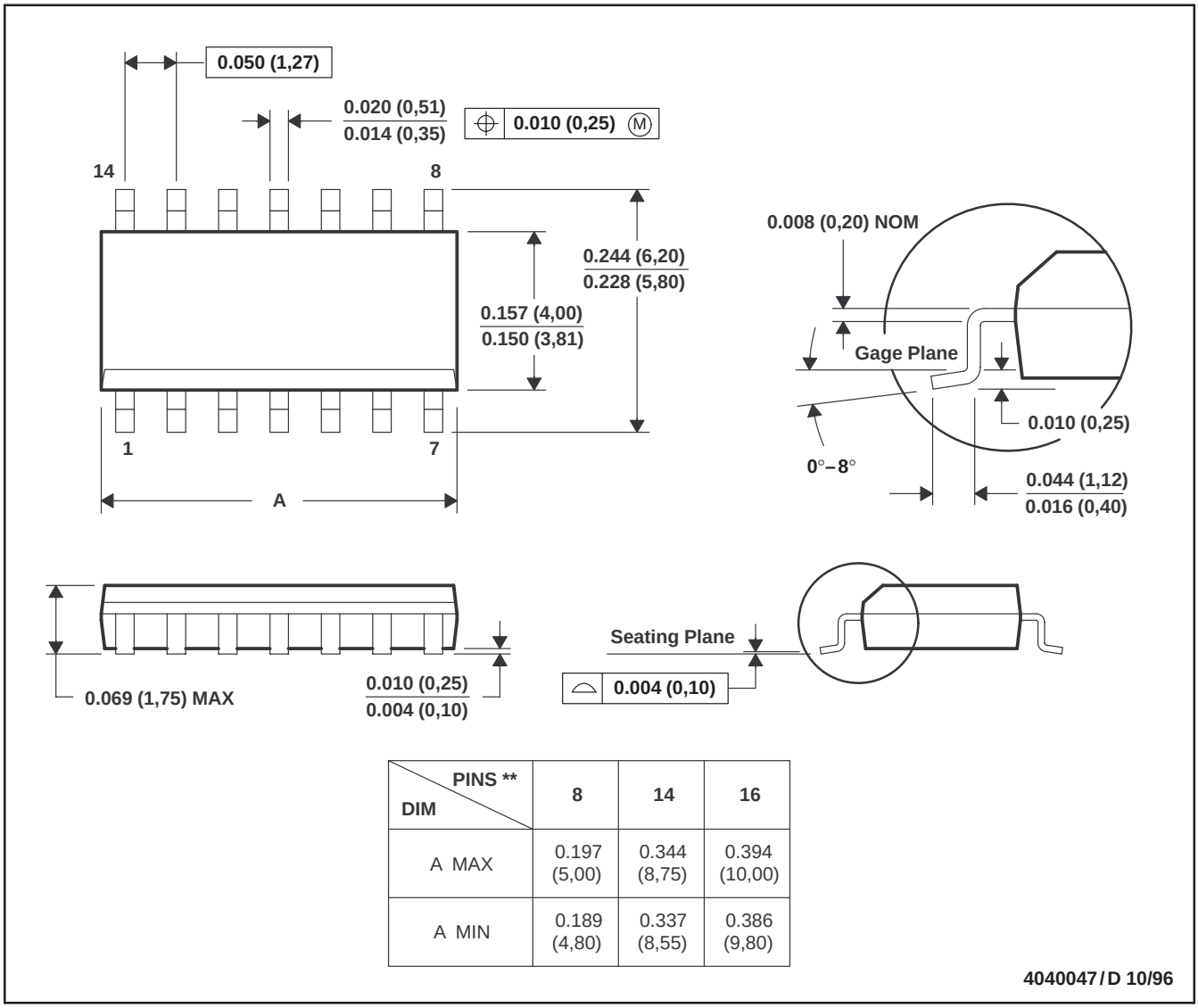


Figure 11. Receiver with Terminated Failsafe

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

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