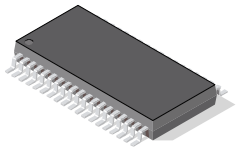


1.5 Gbps LVDS 4x4 CROSSPOINT SWITCH

FEATURES

- **Signaling Rates[1] >1.5 Gbps per Channel**
- **Supports Telecom/Datacom and HDTV Video Switching**
- **Non-Blocking Architecture Allows Each Output to be Connected to Any Input**
- **Total Jitter < 50ps**
- **330 mW When Operating at 1.5 Gbps**
- **Compatible With ANSI TIA/EIA-644-A LVDS Standard**
- **Available Packaging: 38-pin TSSOP**
- **25 mV of Input Voltage Threshold Hysteresis**
- **Propagation Delay Times, 1 ns Maximum**
- **Inputs Electrically Compatible With LVPECL, CML and LVDS Signal Levels**
- **Inputs and Outputs High Impedance on Power Down**
- **Receiver Input and Driver Output ESD Exceeds 8 kV**
- **Operates From a Single 3.3-V Supply**
- **Integrated 110-Ω Line Termination Resistors Available With SN65LVDT125**

APPLICATIONS

- **TBD**

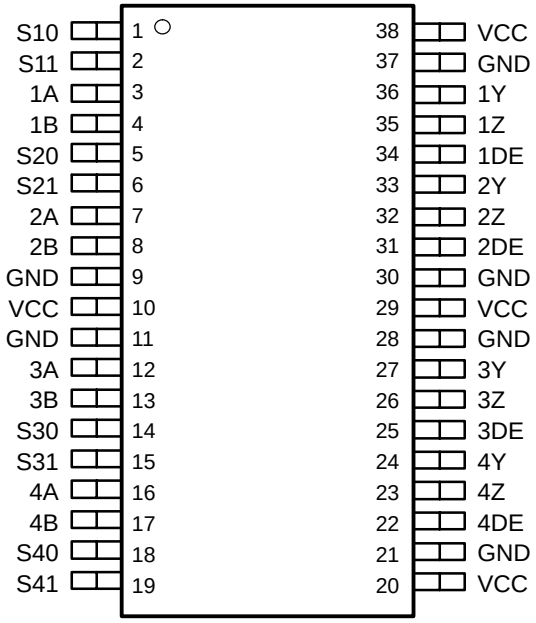
DESCRIPTION

The SN65LVDS125 and SN65LVDT125 are 4x4 nonblocking crosspoint switches. Low-voltage differential signaling (LVDS) is used to achieve signaling rates of 1.5 Gbps per channel. Each output driver includes a 4:1 multiplexer to allow any input to be routed to any output. Internal signal paths are fully differential to achieve the high signaling speeds while maintaining low signal skews. The SN65LVDT125 incorporates 110-Ω termination resistors for those applications where board space is a premium.

Designed to support signaling rates up to 1.5 Gbps for OC-12 clocks (622 MHz). The 1.5-Gbps signaling rate allows use in HDTV systems, including SMPTE 292 video applications requiring signaling rates of 1.485 Gbps. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics).

The SN65LVDS125 and SN65LVDT125 are characterized for operation from –40°C to 85°C.

SN65LVDS125DBT (Marked as LVDS125)
SN65LVDT125DBT (Marked as LVDT125)
(TOP VIEW)



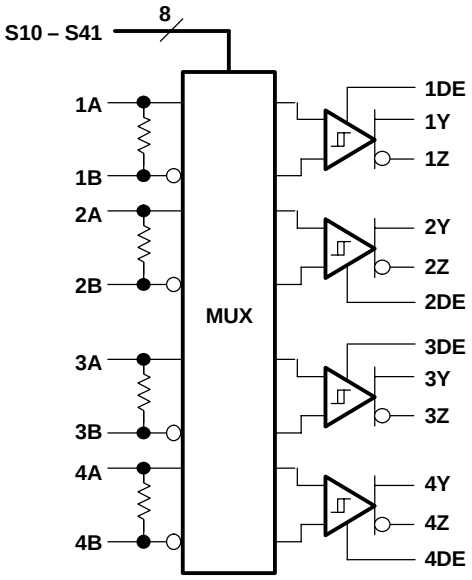
PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

(1) The signaling rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

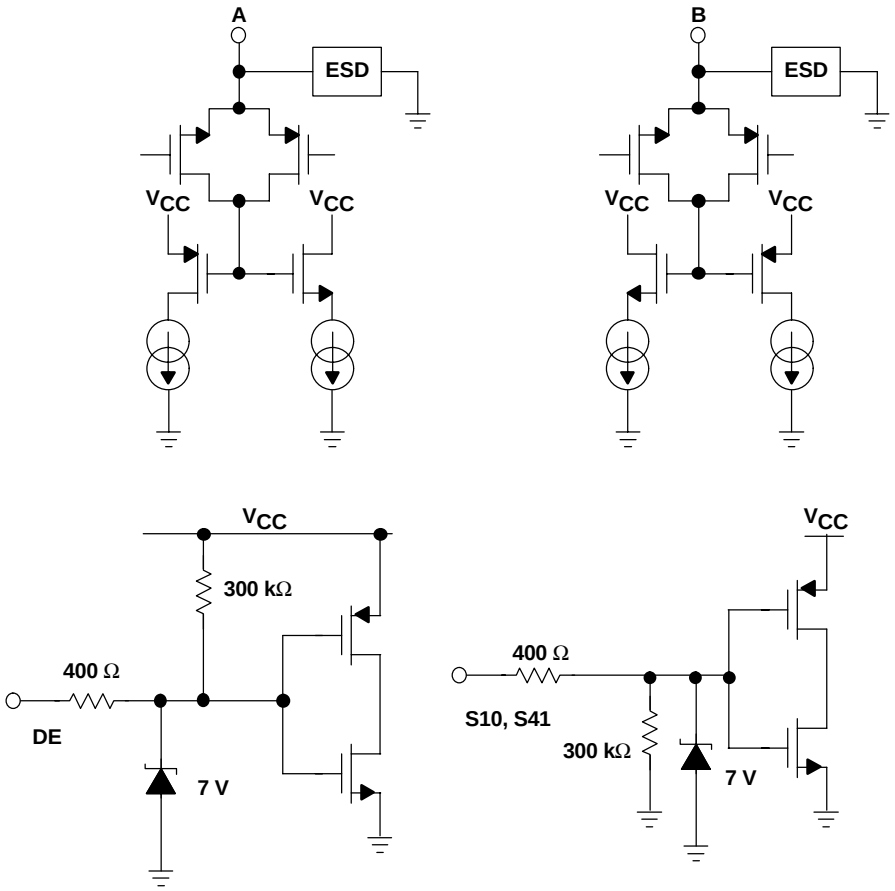
LOGIC DIAGRAM



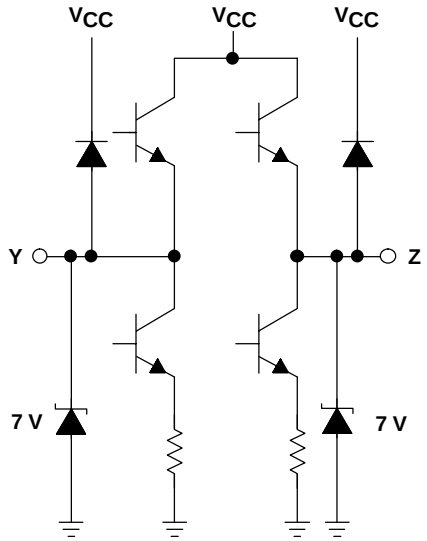
Integrated 110- Termination on LVDT Only

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

INPUT LVDS125



OUTPUT LVDS125



PRODUCT PREVIEW

CROSSPOINT LOGIC TABLES

S10	S11	1Y/1Z	S20	S21	2Y/2Z	S30	S31	3Y/3Z	S40	S41	4Y/4Z
0	0	1A/1B	0	0	1A/1B	0	0	1A/1B	0	0	1A/1B
0	1	2A/2B	0	1	2A/2B	0	1	2A/2B	0	1	2A/2B
1	0	3A/3B	1	0	3A/3B	1	0	3A/3B	1	0	3A/3B
1	1	4A/4B	1	1	4A/4B	1	1	4A/4B	1	1	4A/4B

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
DBT	1071 mW	8.5 mW/°C	556 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounded and with no air flow.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			UNITS
Supply voltage range, v_{CC}			–0.5 V to 4 V
Voltage range	S, DE		–0.5 V to V_{CC} + 2 V
	(A, B)		–0.7 V to 4 V
	$\|V_A - V_B\|$ (LVDT only)		1 V
	(Y, Z)		–0.5 V to 4 V
Elostrostatic discharge	Human body model(3)	A, B, Y, Z, and GND	±8 kV
		All pins	±2 kV
	Charged-device model(4)	All pins	±500 V
Continuous power dissipation			See Dissipation Rating Table
Storage temperature range			–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}	S10–S41, 1DE–4DE	2			V
Low-level input voltage, V_{IL}	S10–S41, 1DE–4DE			0.8	V
Magnitude of differential input voltage $\|V_{ID}\|$	LVDS	0.05			V
	LVDT	0.05		0.8	V
Input voltage (any combination of common–mode or input signals)		0		3.3	V
Operating free-air temperature, T_A		–40		85	°C

TIMING SPECIFICATIONS

PARAMETER			MIN	NOM	MAX	UNIT
t_{SET}	Input to select setup time	See Figure 6		0.5		ns
t_{HOLD}	Input to select hold time			0.5		ns
t_{SWITCH}	Select to switch output			TBD	1.6	ns

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted(1)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold		See Figure 1 and Table 1			50	mV
V_{IT-}	Negative-going differential input voltage threshold		See Figure 1 and Table 1	–50			mV
$V_{ID(HYS)}$	Differential input voltage hysteresis				25		mV
I_{IH}	High-level input current	1DE–4De	V_{IH} = 2 V			–10	µA
		S10–S41				20	
I_{IL}	Low-level input current	1DE–4DE	V_{IL} = 0.8 V			–10	µA
		S10–S41				20	
I_I	Input current (A or B inputs 'LVDS)		V_I = 0 V or 2.4 V, Second input at 1.2 V	–20		20	µA
			V_I = 2.4 V or 3.3 V, Second input at 1.2 V	0		33	
	Input current (A or B inputs 'LVDT)		V_{CC} = 1.5 V; V_I = 0 V or 2.4V, Second input at 1.2 V	–40		40	µA
			V_{CC} = 1.5 V; V_I = 2.4 V or 3.3 V, Second input at 1.2 V	0		66	µA
$I_{I(OFF)}$	Input current (A or B inputs 'LVDS)		V_I = 0 V or 2.4 V, Other input open	–20		20	µA
			V_I = 2.4 V or 3.3 V, Other input open	0		33	
	Input current (A or B inputs 'LVDT)		V_{CC} = 1.5 V; V_I = 0 V or 2.4 V, Other input open	–40		40	µA
			V_{CC} = 1.5 V; V_I = 2.4 V or 3.3 V, Other input open	0		66	µA
I_{IO}	Input offset current ($\lvert I_{IA} - I_{IB} \rvert$) ('LVDS)		V_{IA} = V_{IB}, 0≤ V_{IA} ≤ 3.3 V	–6		6	µA
R_T	Termination resistance ('LVDT)		V_{ID} = 300 mV, V_{IC}= 0 V to 3.3 V	90	111	132	Ω
	Termination resistance('LVDT with power-off)		V_{ID} = 300 mV, V_{IC}= 0 V to 3.3 V, V_{CC} = 1.5 V	90	111	132	
C_T	Differential input capacitance('LVDT with power-off)		V_I = 0.4 sin (4E6πt) + 0.5 V		3		pF
			Powered down		3		

(1) All typical values are at 25°C and with a 3.3 V supply.

PRODUCT PREVIEW

OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude	See Figure 2	247	350	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states	V_{ID} = ±100 mV	–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	150	mV
I_{CC}	Supply current	R_L=100Ω, C_L = 1 pF		70	85	mA
		Disabled		20	25	
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V	–26		26	mA
I_{OSD}	Differential short circuit output current	V_{OD} = 0 V	–12		12	mA
I_{OZ}	High-impedance output current	V_O = 0 V or V_{CC}			±1	µA
C_O	Differential output capacitance	V_I = 0.4 sin(4E6πt) + 0.5 V		3		pF

SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 4	250		1000	ps
t_{PHL}	Propagation delay time, high-to-low-level output		250		1000	
t_r	Differential output signal rise time (20%–80%)				220	
t_f	Differential output signal fall time (20%–80%)				220	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)(1)			0	50	ps
$t_{sk(o)}$	Channel-to-channel output skew(2)				50	ps
$t_{sk(pp)}$	Part-to-part skew(3)				120	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)(4)	750 MHz clock input(5)		1	3.7	ps
$t_{jit(cc)}$	Cycle-to-cycle jitter (peak)(4)	750 MHz clock input(6)		6	23	ps
$t_{jit(pp)}$	Peak-to-peak jitter(4)	1.5 Gbps 2^{23}–1 PRBS input(7)		28	65	ps
$t_{jit(det)}$	Deterministic jitter, peak-to-peak(4)	1.5 Gbps 2^7–1 PRBS input(8)		17	48	ps
t_{PHZ}	Propagation delay, high-level-to–high-impedance output	See Figure 5			5	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				5	
t_{PZH}	Propagation delay, high-impedance -to-high-level output				20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				20	

(1) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.
(2) $t_{sk(o)}$ is the maximum delay time difference between drivers over temperature, V_{CC}, and process.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.
(5) Input voltage = V_{ID} = 200 mV, 50% duty cycle at 750 MHz, t_r = t_f = 50 ps (20% to 80%), measured over 1000 samples.
(6) Input voltage = V_{ID} = 200 mV, 50% duty cycle at 750 MHz, t_r = t_f = 50 ps (20% to 80%).
(7) Input voltage = V_{ID} = 200 mV, 2^{23}–1 PRBS pattern at 1.5 Gbps, t_r = t_f = 50 ps (20% to 80%), measured over 200k samples.
(8) Input voltage = V_{ID} = 200 mV, 2^7–1 PRBS pattern at 1.5 Gbps, t_r = t_f = 50 ps (20% to 80%).

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

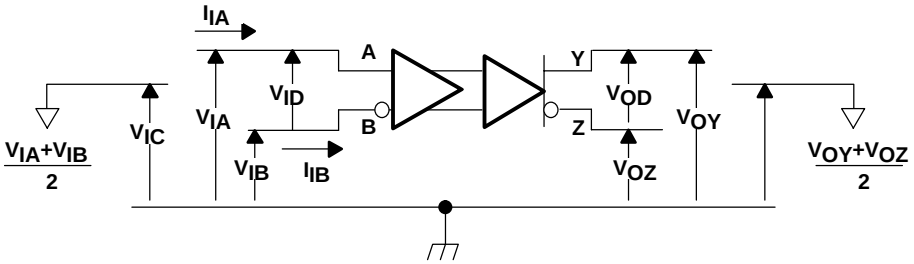


Figure 1. Voltage and Current Definitions

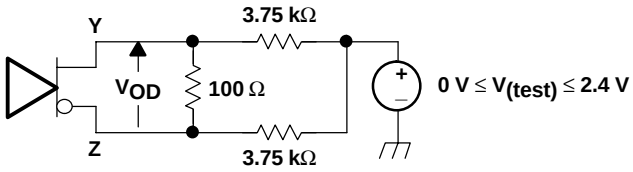
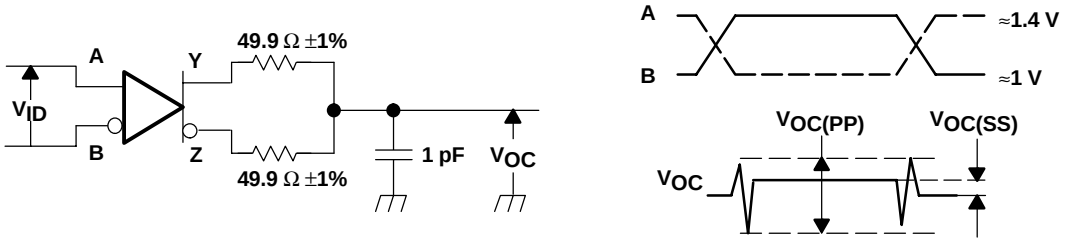
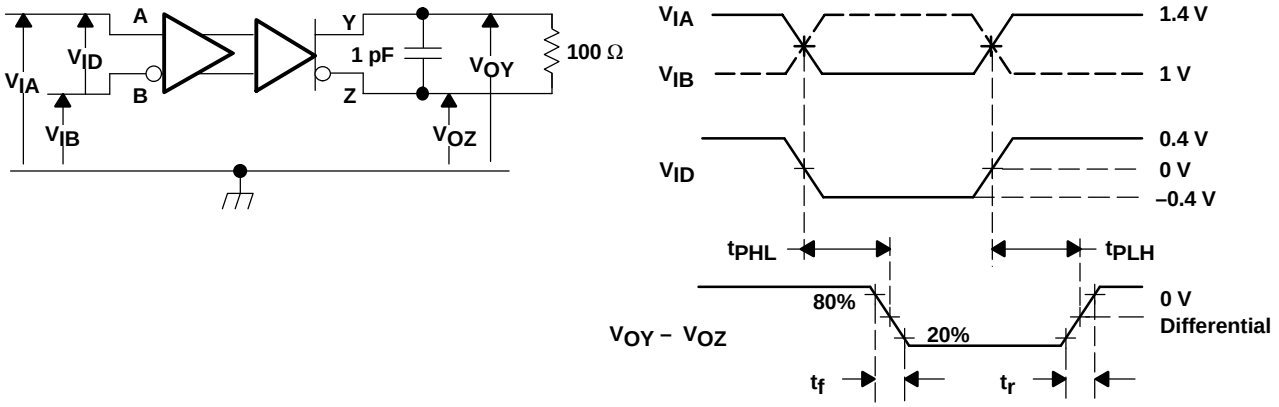


Figure 2. Differential Output Voltage (V_{OD}) Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10 ns; R_L = 100W; C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.;the measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

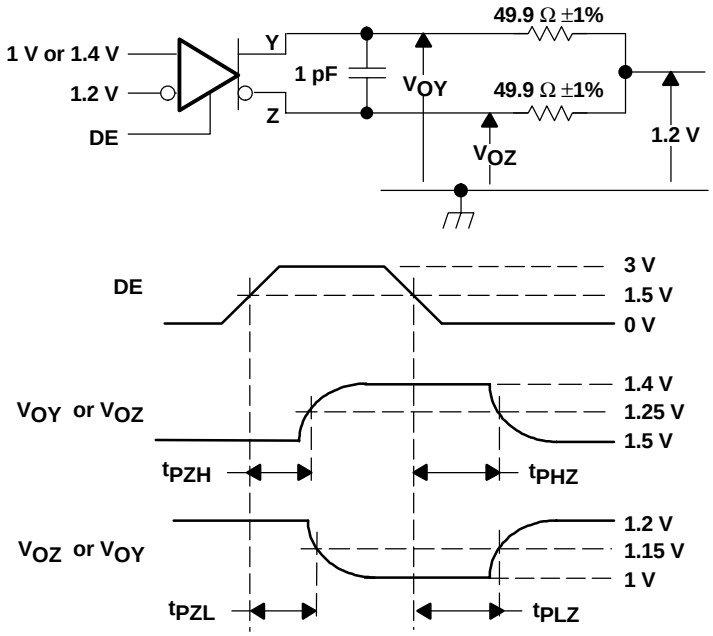
Figure 3. Test Circuit and Definitions fot the Driver Common-Mode Output Voltage



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq .25$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

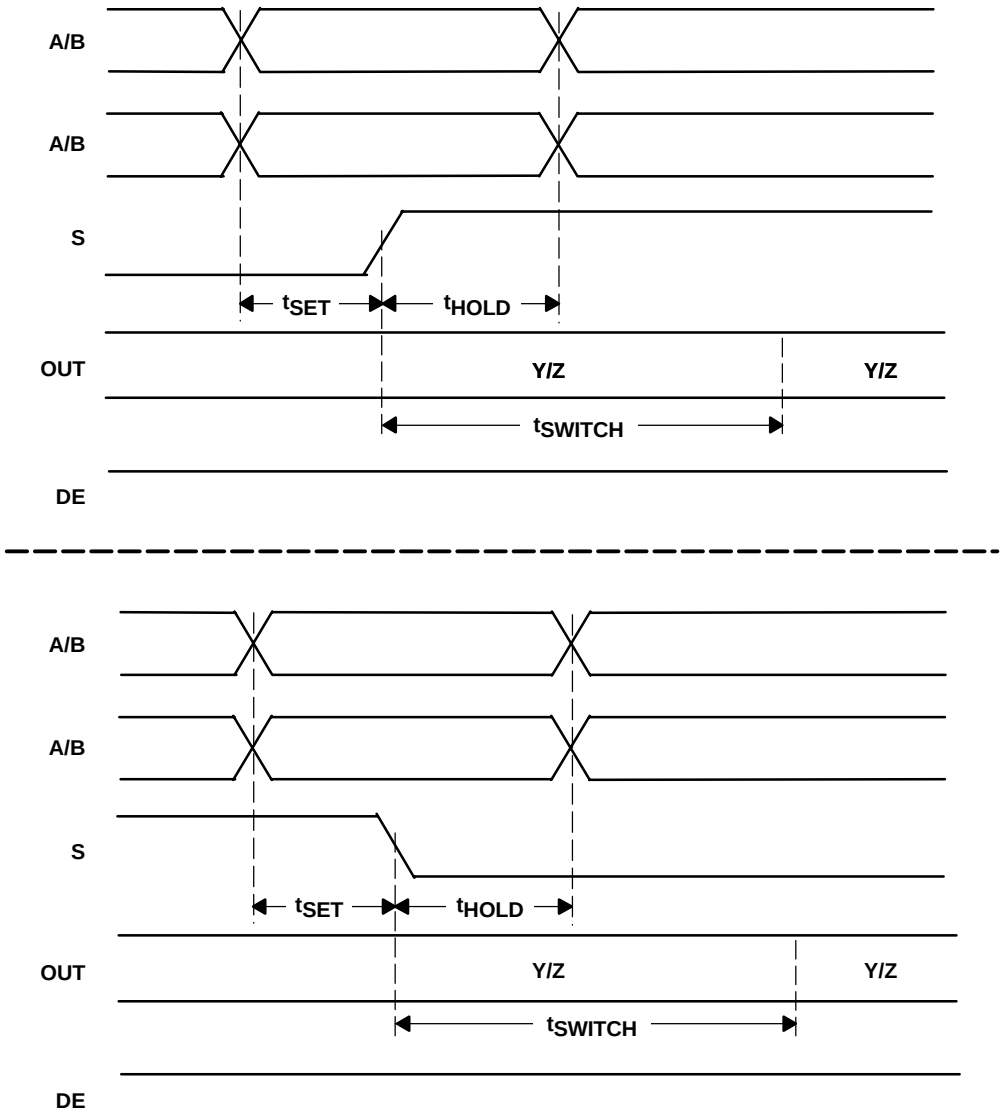
Figure 4. Timing Test Circuit and Waveforms

PRODUCT PREVIEW



NOTE: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions



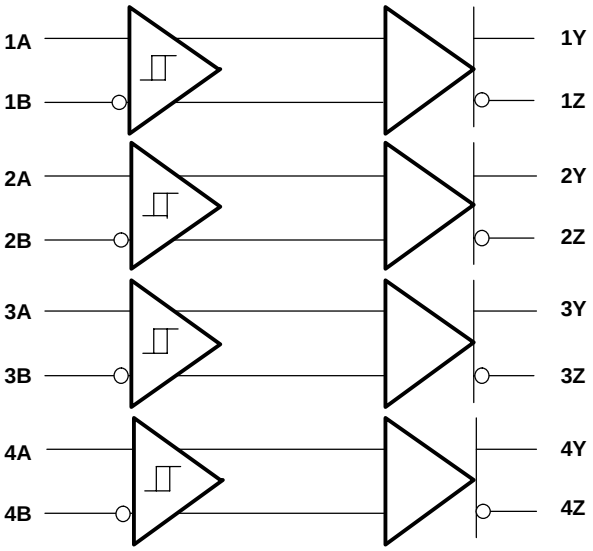
NOTE: t_{SET} and t_{HOLD} times specify that data must be in a stable state before and after mux control switches.

Figure 6. Input to Select for Both Rising and Falling Edge Setup and Hold Times

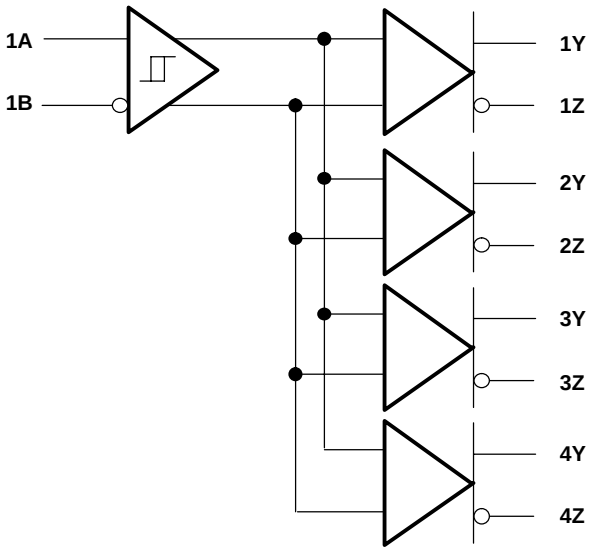
APPLICATION INFORMATION

CONFIGURATION EXAMPLES

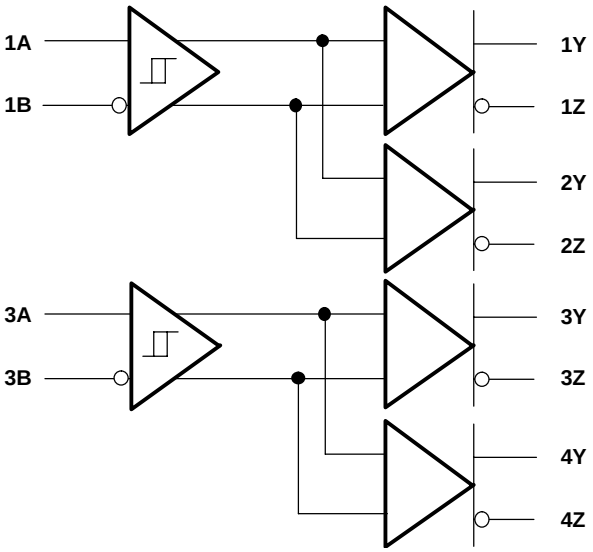
S10	S11	S20	S21
0	0	0	1
S30	S31	S40	S41
1	0	1	1



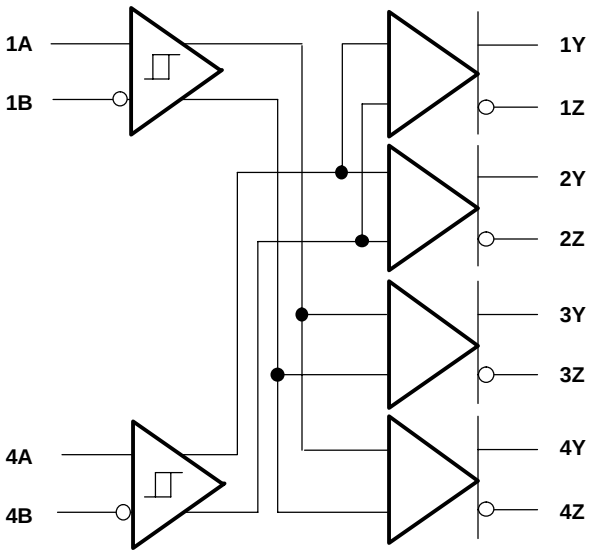
S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
0	0	0	0



S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
1	0	1	0



S10	S11	S20	S21
1	1	1	1
S30	S31	S40	S41
0	0	0	0

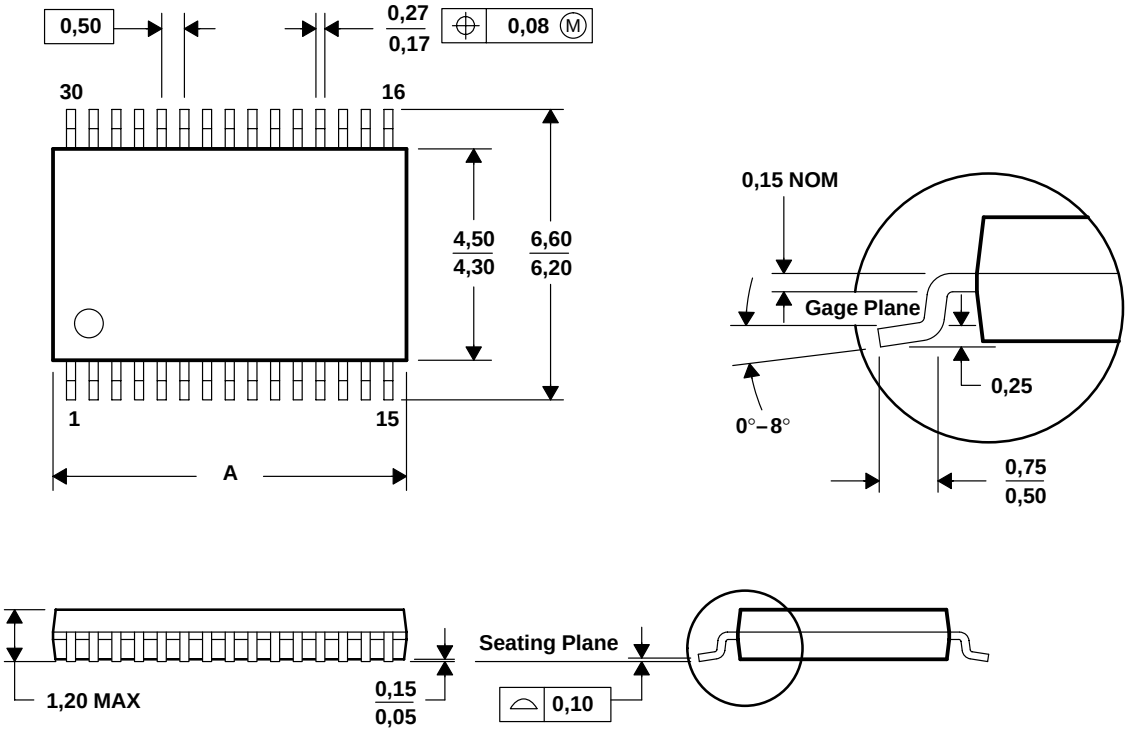


PRODUCT PREVIEW

MPDS019D – FEBRUARY 1996 – REVISED FEBRUARY 2002

DBT (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

30 PINS SHOWN



DIM \ PINS **	20	24	28	30	38	44	50
A MAX	5,10	6,60	7,90	7,90	9,80	11,10	12,60
A MIN	4.90	6,40	7,70	7,70	9,60	10,90	12,40

4073252/E 02/02

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153

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