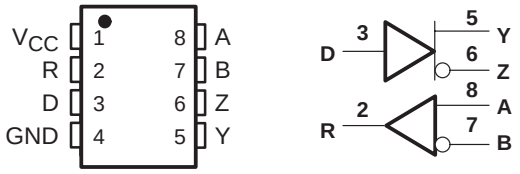
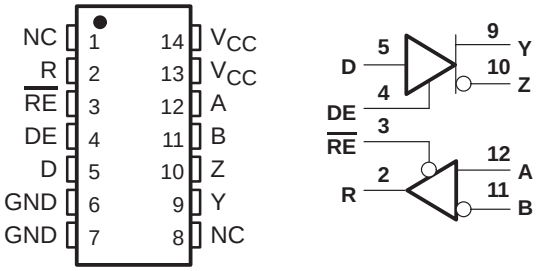
- **Low-Voltage Differential Drivers and Receivers for Half-Duplex Operation**
- **Signaling Rates up to 400 Mbps**
- **Bus-Terminal ESD Exceeds 12 kV**
- **Operates from a Single 3.3 V Supply**
- **Low-Voltage Differential Signaling with Typical Output Voltages of 340 mV with a 50-Ω Load**
- **Propagation Delay Times**
  - **Driver: 1.7 ns Typ**
  - **Receiver: 3.7 ns Typ**
- **Power Dissipation at 200 MHz**
  - **Driver: 50 mW Typical**
  - **Receiver: 60 mW Typical**
- **LVTTL Input Levels are 5 V Tolerant**
- **Driver is High Impedance When Disabled or With V_{CC} < 1.5 V**
- **Receiver has Open-Circuit Fail Safe**
- **Surface-Mount Packaging**
  - **D Package (SOIC)**
  - **DGK Package (MSOP) ('LVDM179 Only)**

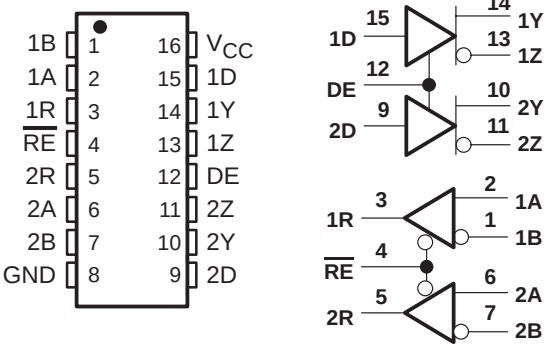
SN65LVDM179D (Marked as **DM179** or **LVM179**)
SN65LVDM179DGK (Marked as **M79**)
(TOP VIEW)



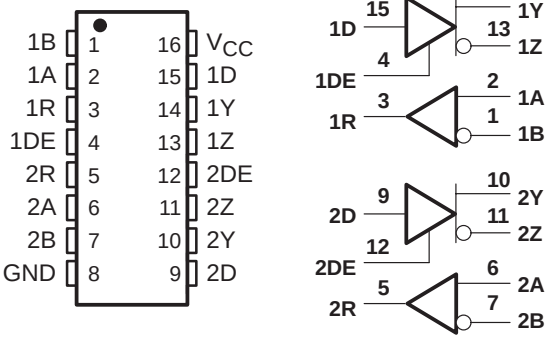
SN65LVDM180D (Marked as **LVDM180**)
(TOP VIEW)



SN65LVDM050D (Marked as **LVDM050**)
(TOP VIEW)



SN65LVDM051D (Marked as **LVDM051**)
(TOP VIEW)



description

The SN65LVDM179, SN65LVDM180, SN65LVDM050, and SN65LVDM051 are differential line drivers and receivers that use low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbps. These circuits are similar to TIA/EIA-644 standard compliant devices (SN65LVDS) counterparts, except that the output current of the drivers is doubled. This modification provides a minimum differential output voltage magnitude of 247 mV into a 50-Ω load and allows double-terminated lines and half-duplex operation. The receivers detect a voltage difference of 100 mV with up to 1 V of ground potential difference between a transmitter and receiver.

The intended application of these devices and signaling technique is half-duplex or multiplex baseband data transmission over controlled impedance media of approximately 100-Ω characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description (continued)

AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE (D)	SMALL OUTLINE (DGK)
–40°C to 85°C	SN65LVDM050D	—
	SN65LVDM051D	—
	SN65LVDM179D	SN65LVDM179DGK
	SN65LVDM180D	—

NOTE:
The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics.

The SN65LVDM179, SN65LVDM180, SN65LVDM050, and SN65LVDM051 are characterized for operation from –40°C to 85°C.

Function Tables

SN65LVDM179 RECEIVER

INPUTS	OUTPUT
$V_{ID} = V_A – V_B$	R
$V_{ID} \geq 100$ mV	H
–100 MV < V_{ID} < 100 mV	?
$V_{ID} \leq –100$ mV	L
Open	H

H = high level, L = low level, ? = indeterminate

SN65LVDM179 DRIVER

INPUT	OUTPUTS	
D	Y	Z
L	L	H
H	H	L
Open	L	H

H = high level, L = low level

SN65LVDM180, SN65LVDM050, and SN65LVDM051 RECEIVER

INPUTS		OUTPUT
$V_{ID} = V_A – V_B$	$\overline{RE}$	R
$V_{ID} \geq 100$ mV	L	H
–100 MV < V_{ID} < 100 mV	L	?
$V_{ID} \leq –100$ mV	L	L
Open	L	H
X	H	Z

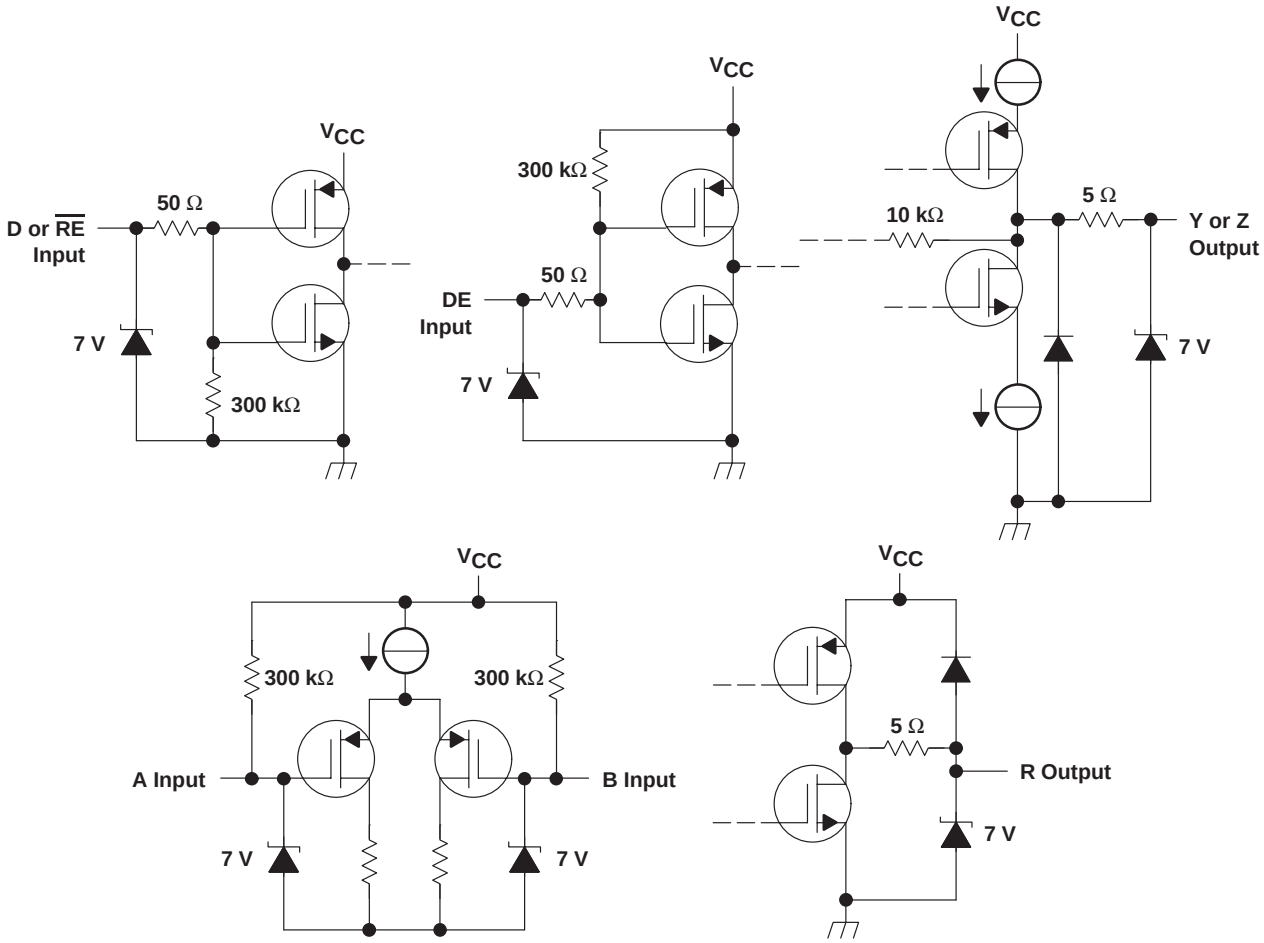
H = high level, L = low level, Z = high impedance,
X = don't care

SN65LVDM180, SN65LVDM050, and SN65LVDM051 DRIVER

INPUTS		OUTPUTS	
D	DE	Y	Z
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Z	Z

H = high level, L = low level, Z = high impedance,
X = don't care

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 4 V
Voltage range (D, R, DE, $\overline{RE}$) . . . . . –0.5 V to 6 V
Voltage range (Y, Z, A, and B) . . . . . –0.5 V to 4 V
Electrostatic discharge (Y, Z, A, B , and GND) (see Note 2) . . . . . CLass 3, A:12 kV, B:600 V
All . . . . . Class 3, A:7 kV, B:500 V
Continuous power dissipation . . . . . see dissipation rating table
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 250°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$†	$T_A = 85°C$ POWER RATING
D8	725 mW	5.8 mW/°C	377 mW
D14 or D16	950 mW	7.8 mW/°C	494 mW
DGK	424 mW	3.4 mW/°C	220 mW

† This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Magnitude of differential input voltage, $\lvert V_{ID} \rvert$	0.1		0.6	V
Common–mode input voltage, V_{IC} (see Figure 6)	$\frac{\lvert V_{ID} \rvert}{2}$		$2.4 - \frac{\lvert V_{ID} \rvert}{2}$	V
			$V_{CC}–0.8$	
Operating free–air temperature, T_A	–40		85	°C

device electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}	Supply current	SN65LVDM179	No receiver load, Driver R_L = 50 Ω		10	15	mA
		SN65LVDM180	Driver and receiver enabled, No receiver load, Driver R_L = 50 Ω		10	15	mA
			Driver enabled, Receiver disabled, R_L = 50 Ω		9	13	
			Driver disabled, Receiver enabled, No load		1.7	5	
			Disabled		0.5	2	
		SN65LVDM050	Drivers and receivers enabled, No receiver loads, Driver R_L = 50 Ω		19	27	mA
			Drivers enabled, Receivers disabled, R_L = 50 Ω		16	24	
			Drivers disabled, Receivers enabled, No loads		4	6	
			Disabled		0.5	1	
		SN65LVDM051	Drivers enabled, No receiver loads, Driver R_L = 50 Ω		19	27	mA
			Drivers disabled, No loads		4	6	

† All typical values are at 25°C and with a 3.3 V supply.

driver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OD}\rvert$	Differential output voltage magnitude		R_L = 50 Ω, See Figure 1 and Figure 2	247	340	454	mV
$\Delta\lvert V_{OD}\rvert$	Change in differential output voltage magnitude between logic states			–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 3	1.125	1.2	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				50	150	mV
I_{IH}	High-level input current	DE	V_{IH} = 5 V		–0.5	–20	µA
		D			2	20	
I_{IL}	Low-level input current	DE	V_{IL} = 0.8 V		–0.5	–10	µA
		D			2	10	
I_{OS}	Short-circuit output current		V_{OY} or V_{OZ} = 0 V		7	10	mA
			V_{OD} = 0 V		7	10	
I_{OZ}	High-impedance output current		V_{OD} = 600 mV			±1	µA
			V_O = 0 V or V_{CC}			±1	
$I_{O(OFF)}$	Power-off output current		V_{CC} = 0 V, V_O = 3.6 V			±1	µA
C_{IN}	Input capacitance				3		pF

receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 5 and Table 1			100	mV
$V_{ITH–}$	Negative-going differential input voltage threshold		–100			
V_{OH}	High-level output voltage	I_{OH} = –8 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V
I_I	Input current (A or B inputs)	V_I = 0	–2	–11	–20	µA
		V_I = 2.4 V	–1.2	–3		
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_{CC} = 0			±20	µA
I_{IH}	High-level input current (enables)	V_{IH} = 5 V			10	µA
I_{IL}	Low-level input current (enables)	V_{IL} = 0.8 V			10	µA
I_{OZ}	High-impedance output current	V_O = 0 or 5 V			±10	µA
C_I	Input capacitance			5		pF

† All typical values are at 25°C and with a 3.3-V supply.

driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50Ω, C_L = 10 pF, See Figure 6		1.7	2.7	ns
t_{PHL}	Propagation delay time, high-to-low-level output			1.7	2.7	ns
t_r	Differential output signal rise time			0.6	1	ns
t_f	Differential output signal fall time			0.6	1	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)			250		ps
$t_{sk(o)}$	Channel-to-channel output skew‡			100		ps
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 7		6	10	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			6	10	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			4	10	ns
t_{pLZ}	Propagation delay time, low-level-to-high-impedance output			5	10	ns

† All typical values are at 25°C and with a 3.3-V supply.
‡ $t_{sk(o)}$ is the maximum delay time difference between drivers on the same device.

receiver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 6		3.7	4.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3.7	4.5	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)			0.1		ns
$t_{sk(o)}$	Channel-to-channel output skew			0.2		ns
t_r	Output signal rise time	C_L = 10 pF, See Figure 6		0.7	1.5	ns
t_f	Output signal fall time			0.9	1.5	ns
t_{PZH}	Propagation delay time, high-level-to-high-impedance output	See Figure 7		2.5		ns
t_{PZL}	Propagation delay time, low-level-to-low-impedance output			2.5		ns
t_{PHZ}	Propagation delay time, high-impedance-to-high-level output			7		ns
t_{PLZ}	Propagation delay time, low-impedance-to-high-level output			4		ns

† All typical values are at 25°C and with a 3.3-V supply.

PARAMETER MEASUREMENT INFORMATION

driver

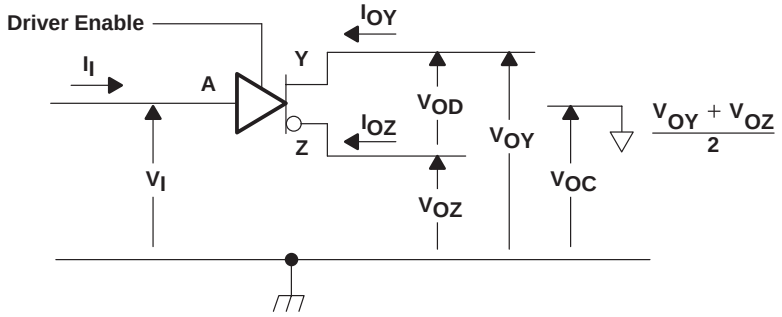
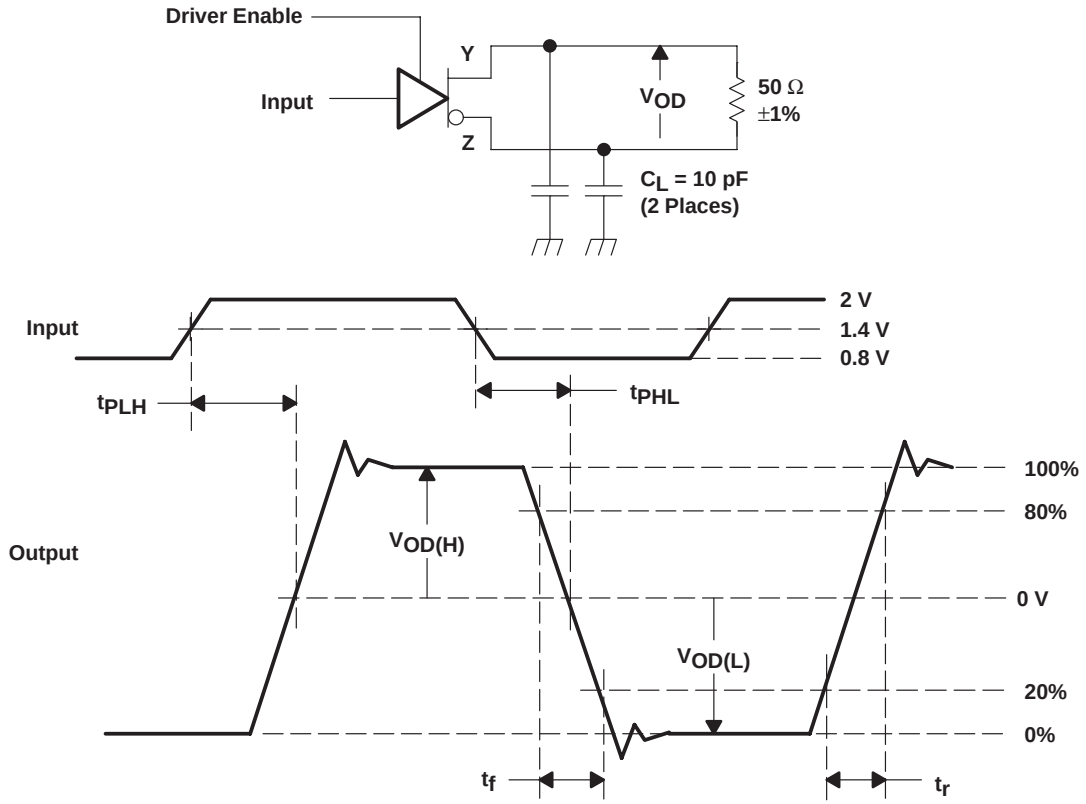


Figure 1. Driver Voltage and Current Definitions

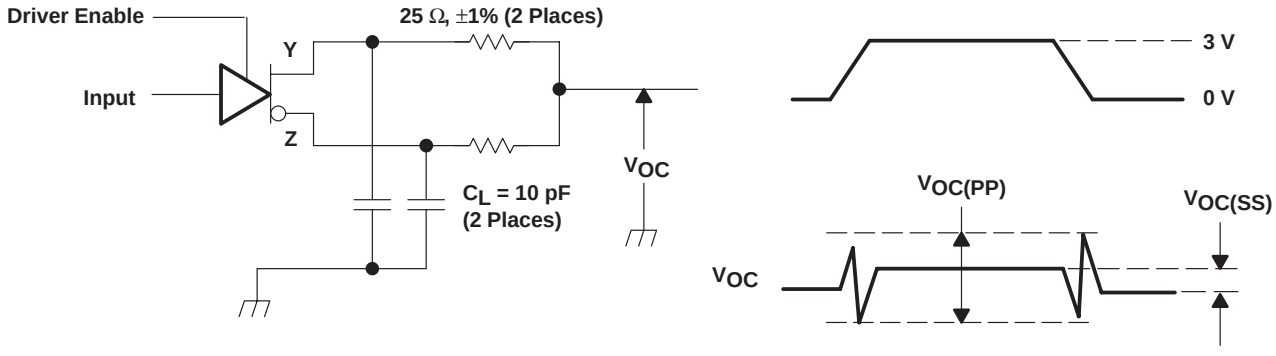
PARAMETER MEASUREMENT INFORMATION

driver (continued)



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

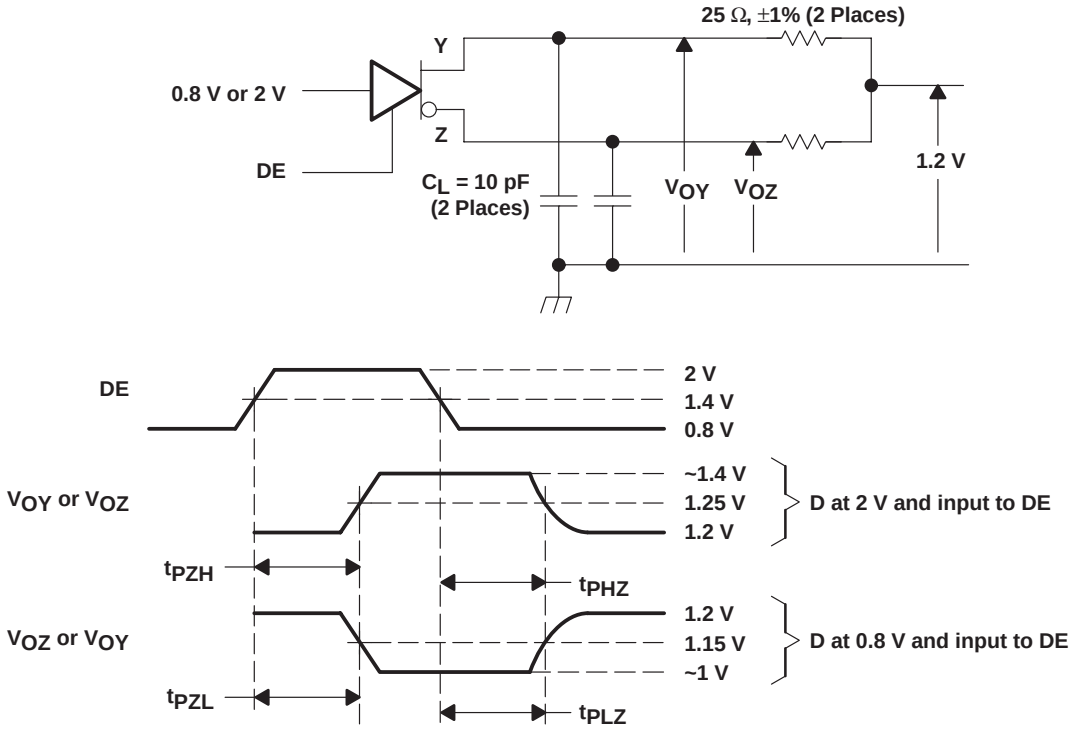


NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION

driver (continued)



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Enable and Disable Time Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION

receiver

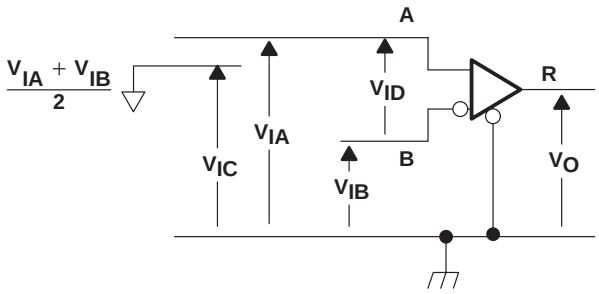


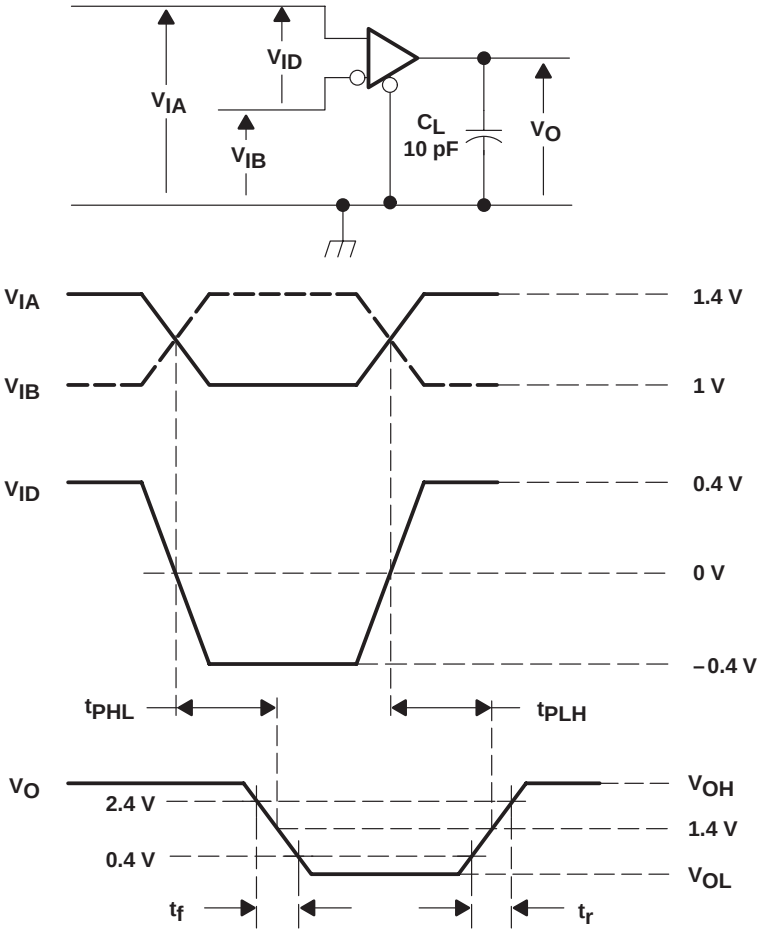
Figure 5. Receiver Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES (V)		RESULTING DIFFERENTIAL INPUT VOLTAGE (mV)	RESULTING COMMON-MODE INPUT VOLTAGE (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.15	100	1.2
1.15	1.25	–100	1.2
2.4	2.3	100	2.35
2.3	2.4	–100	2.35
0.1	0	100	0.05
0	0.1	–100	0.05
1.5	0.9	600	1.2
0.9	1.5	–600	1.2
2.4	1.8	600	2.1
1.8	2.4	–600	2.1
0.6	0	600	0.3
0	0.6	–600	0.3

PARAMETER MEASUREMENT INFORMATION

receiver (continued)

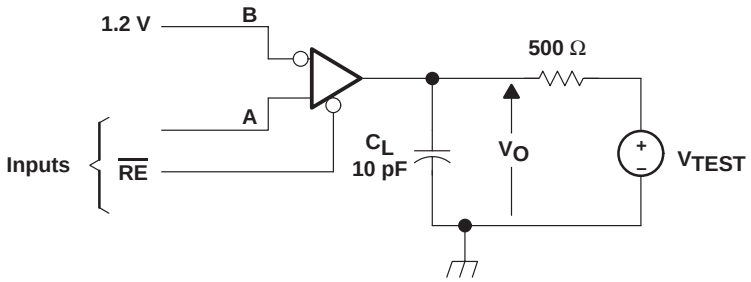


NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 6. Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION

receiver (continued)



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

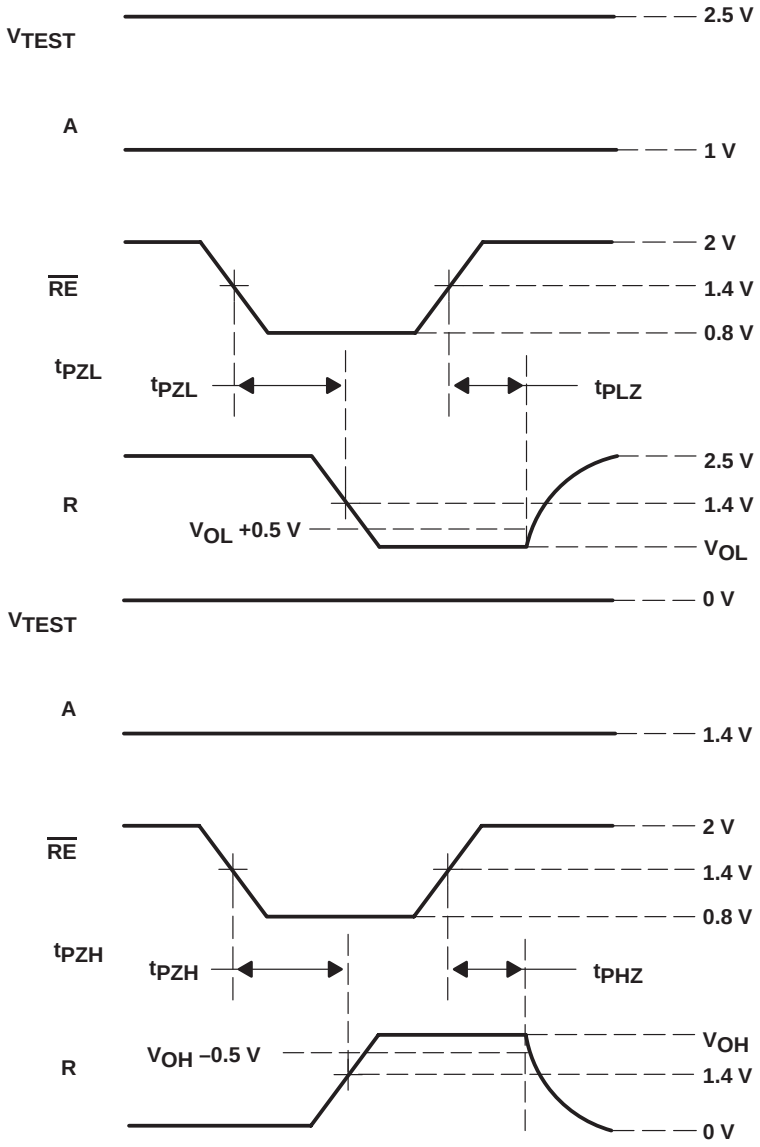


Figure 7. Enable/Disable Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

COMMON-MODE INPUT VOLTAGE vs SUPPLY VOLTAGE

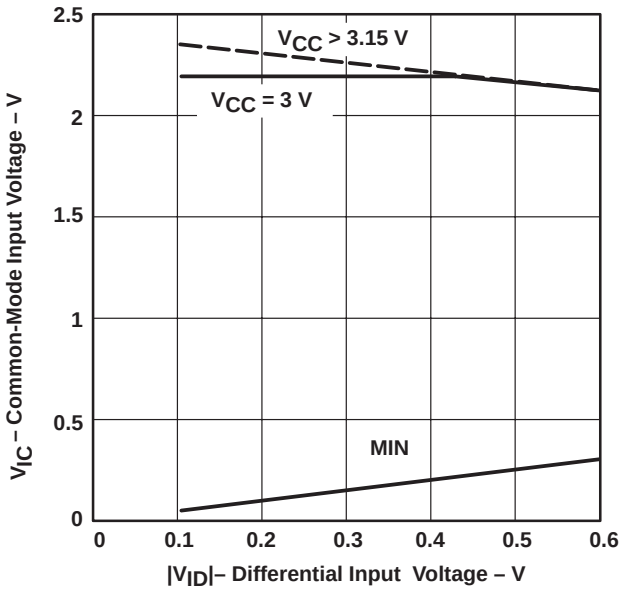


Figure 8

DRIVER LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

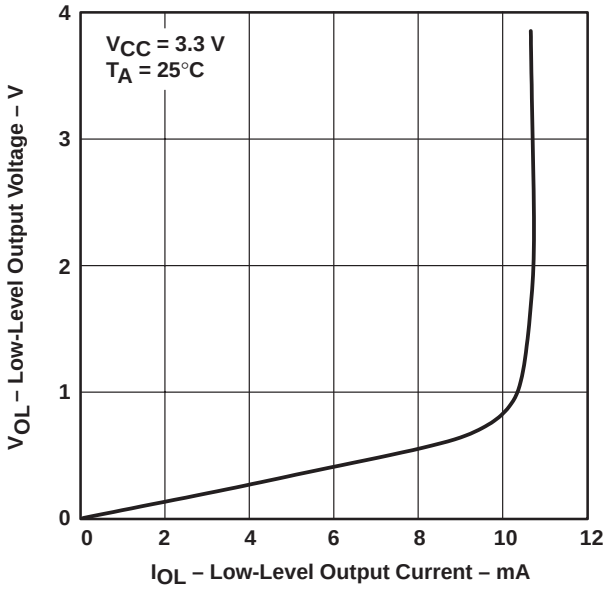


Figure 9

DRIVER HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

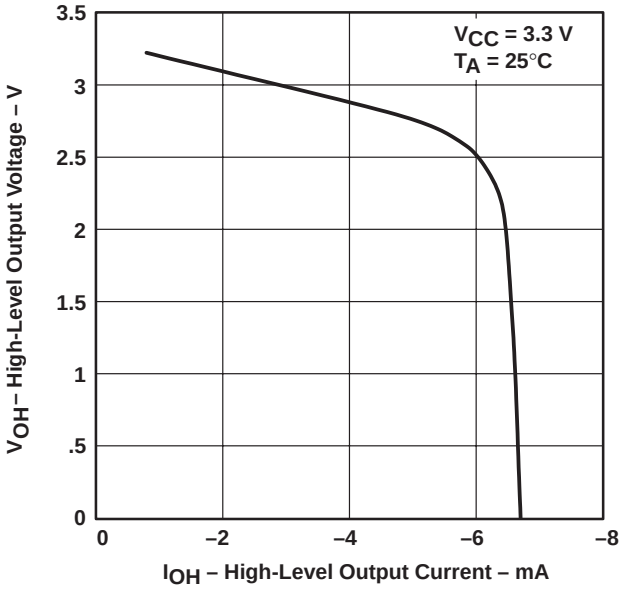


Figure 10

TYPICAL CHARACTERISTICS

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

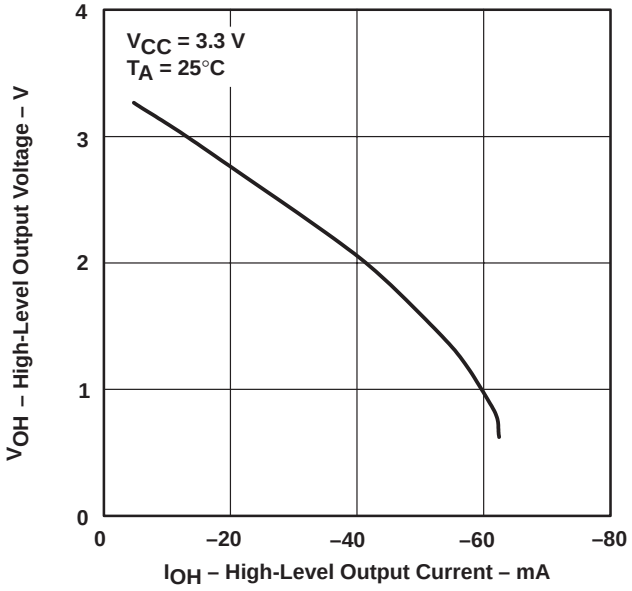


Figure 11

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

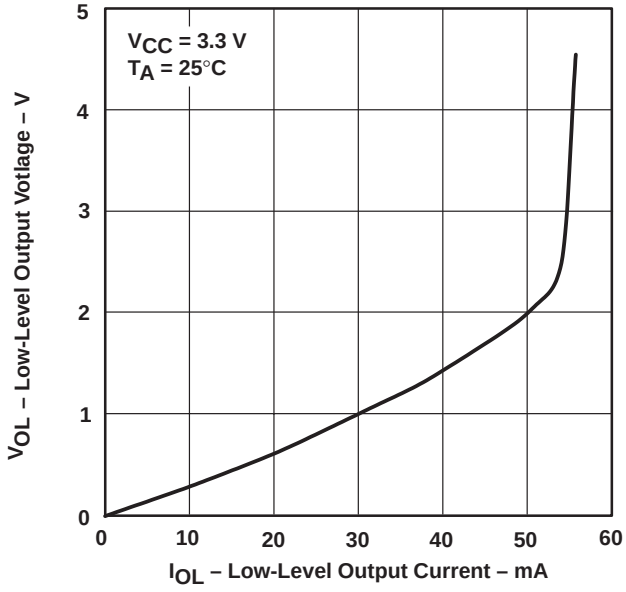


Figure 12

DRIVER
HIGH-TO-LOW LEVEL PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

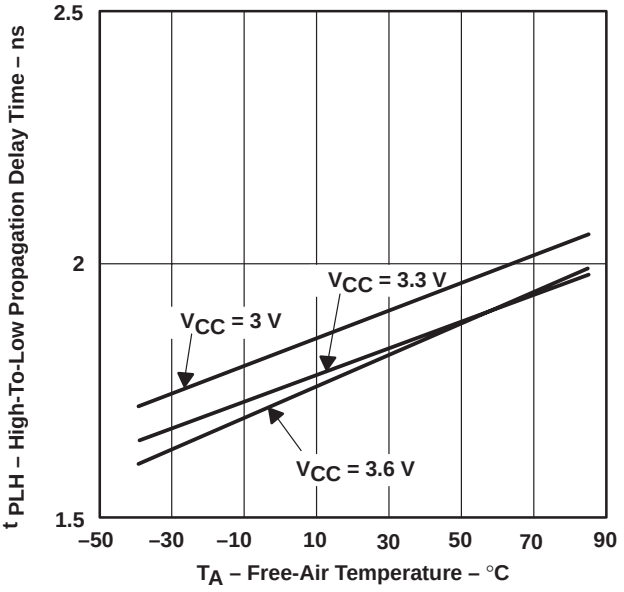


Figure 13

DRIVER
LOW-TO-HIGH LEVEL PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

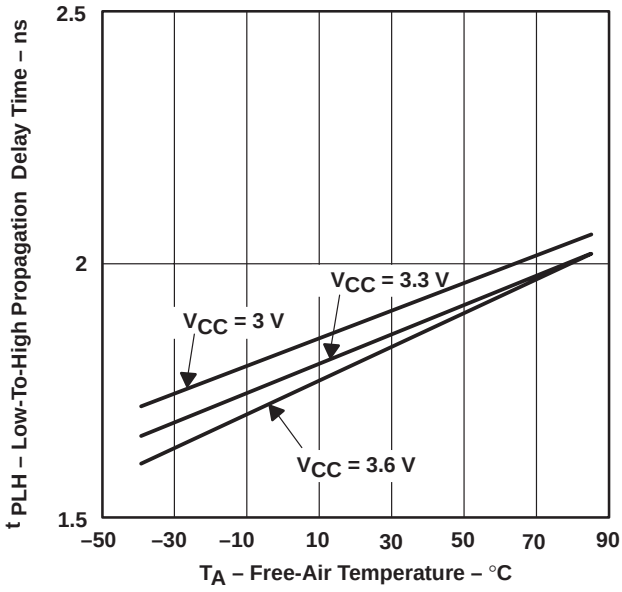


Figure 14

TYPICAL CHARACTERISTICS

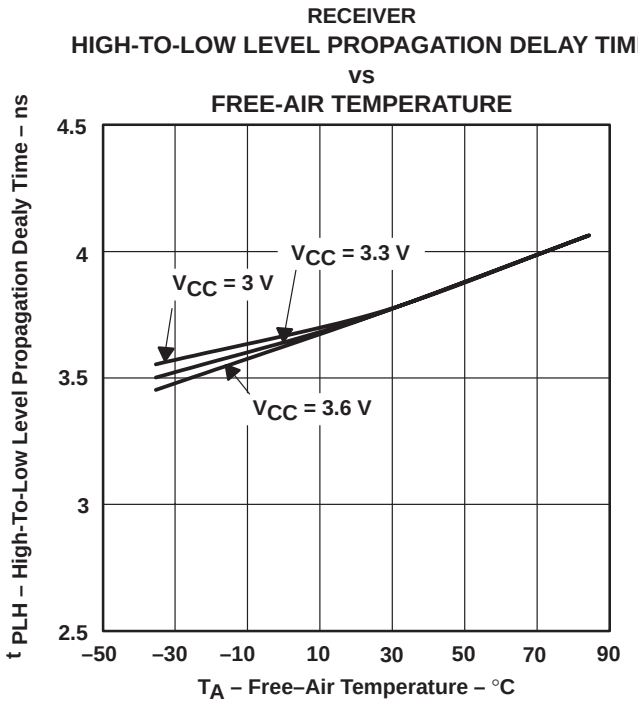


Figure 15

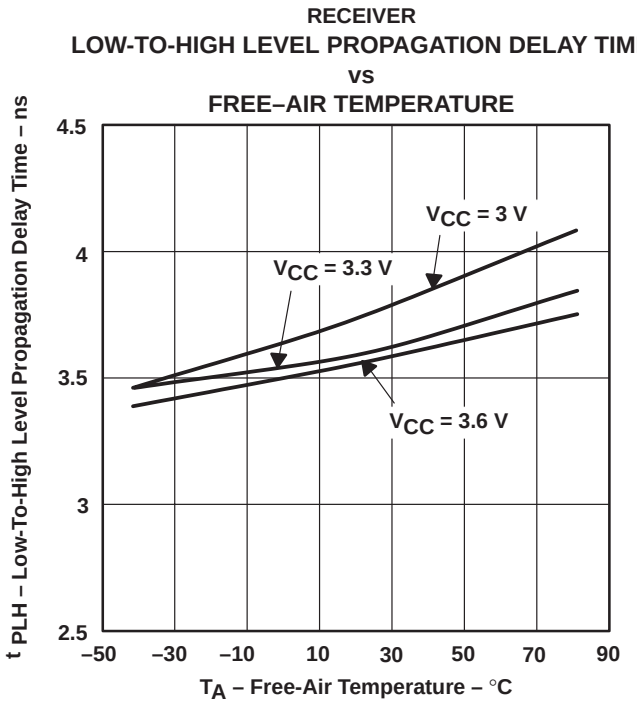


Figure 16

APPLICATION INFORMATION

The devices are generally used as building blocks for high-speed point-to-point data transmission. Ground differences are less than 1 V with a low common–mode output and balanced interface for very low noise emissions. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/Receivers maintain ECL speeds without the power and dual supply requirements.

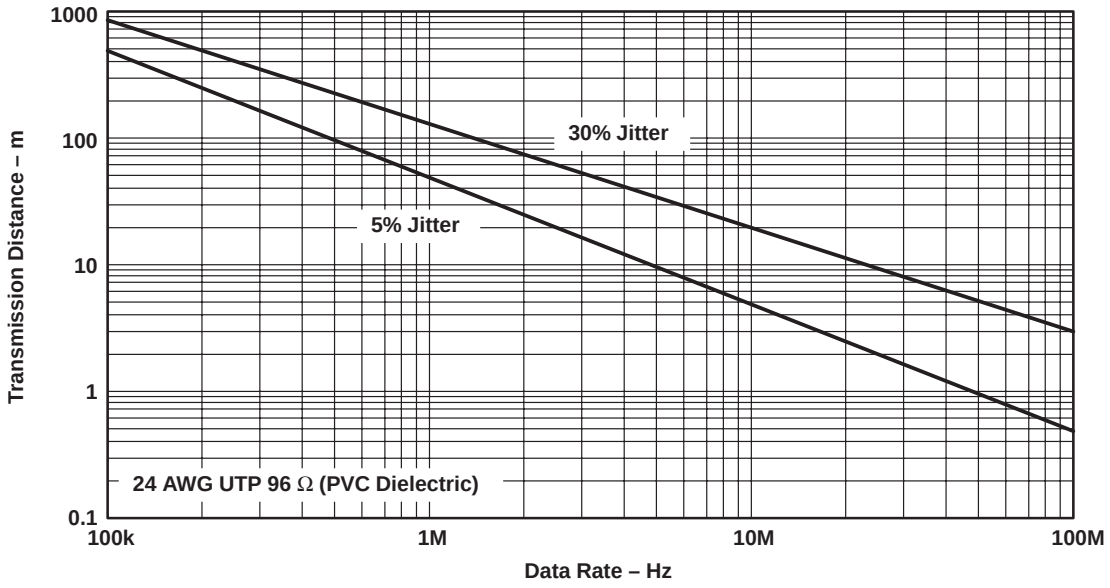


Figure 17. Data Transmission Distance Versus Rate

APPLICATION INFORMATION

fail safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different, however, in how it handles the open-input circuit situation.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near V_{CC} through 300-kΩ resistors as shown in Figure 11. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level, regardless of the differential input voltage.

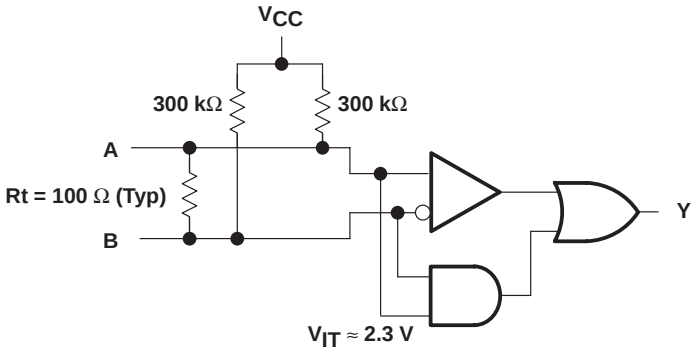


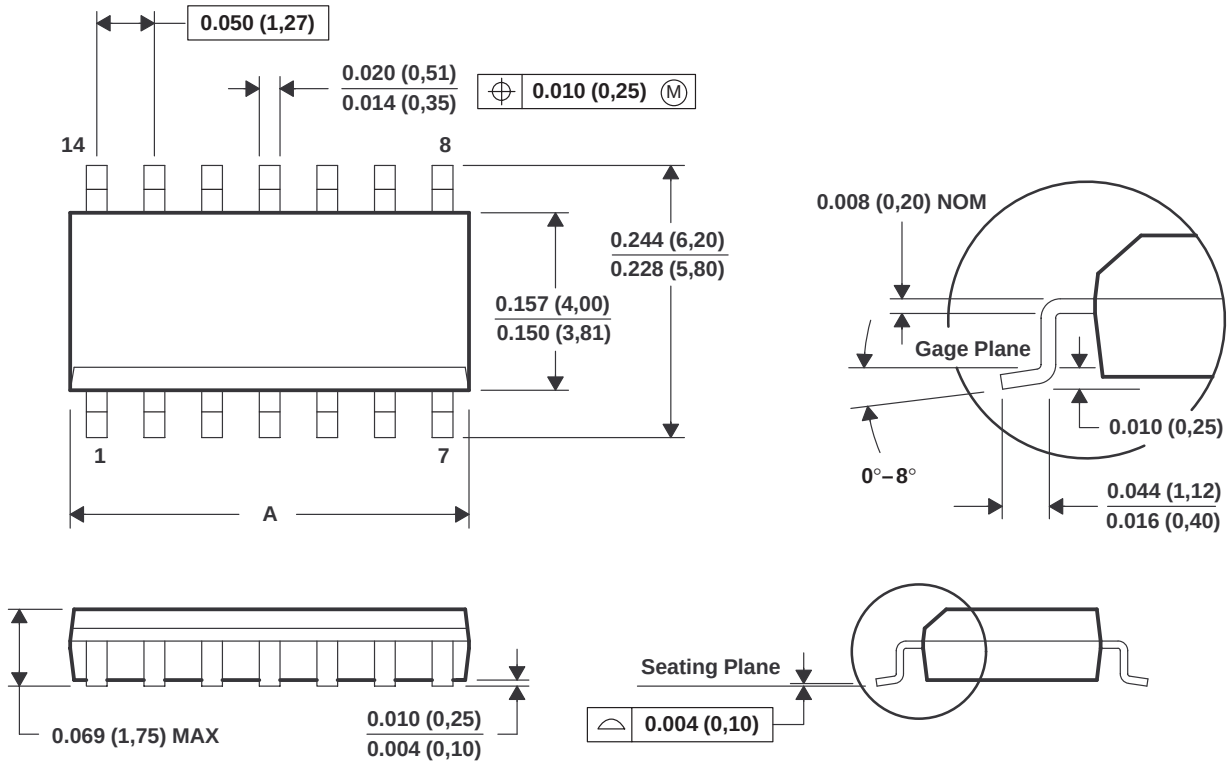
Figure 18. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pull-up currents from the receiver and the fail-safe feature.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

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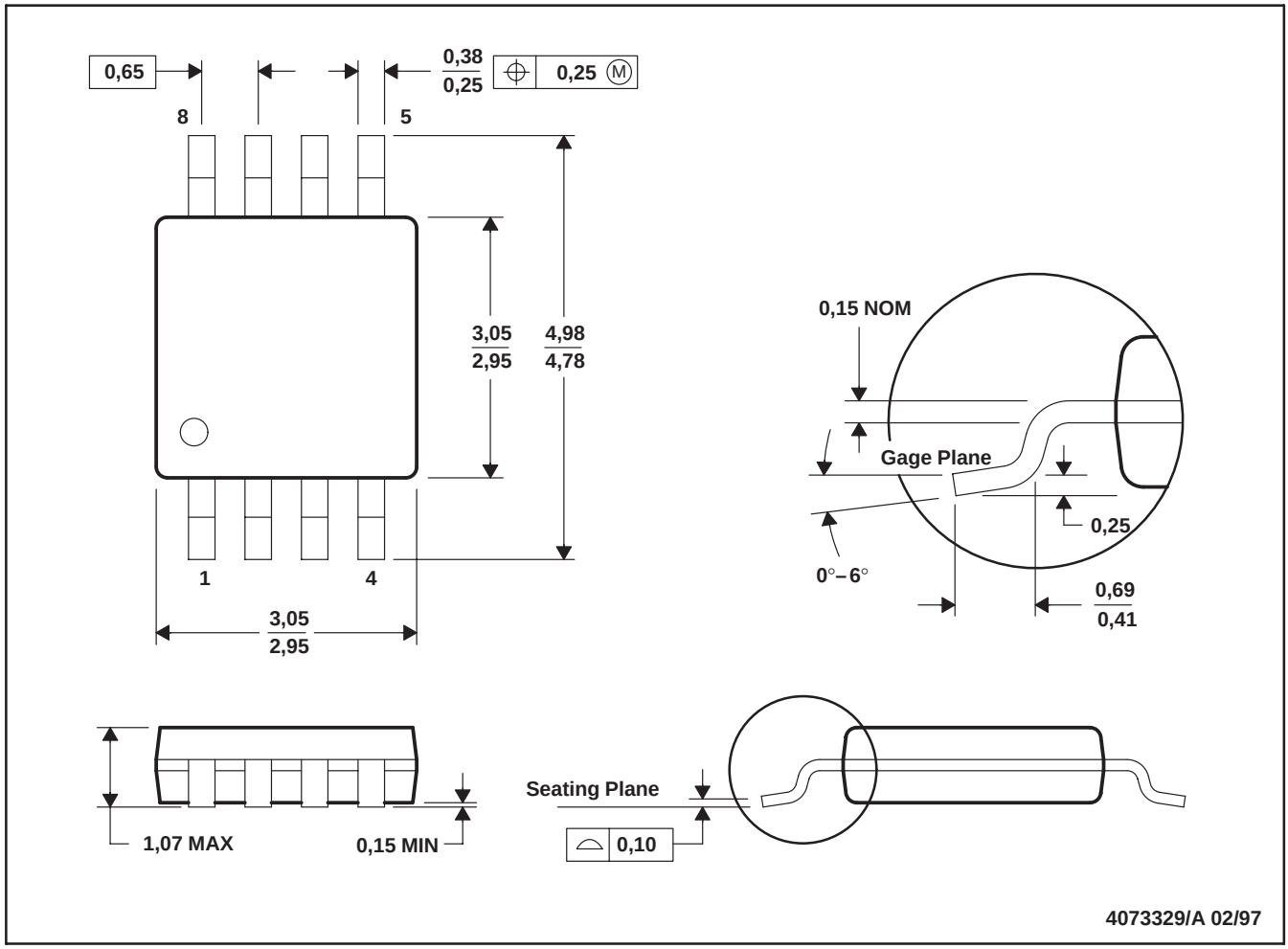
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

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