

# SN65LBC184, SN75LBC184 DIFFERENTIAL TRANSCIEVER WITH TRANSIENT VOLTAGE SUPPRESSION

SLLS236A – OCTOBER 1996 – REVISED MAY 1998

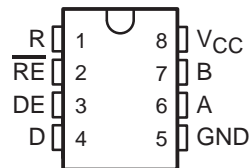
- Integrated Transient Voltage Suppression
- ESD Protection for Bus Terminals:
  - $\pm 15$  kV Human Body Model
  - $\pm 8$  kV IEC1000-4-2, Contact Discharge
  - $\pm 15$  kV IEC1000-4-2, Air-Gap Discharge
- Circuit Damage Protection of 400 W Peak (Typical)
- Controlled Driver Output-Voltage Slew Rates Allows Longer Cable Stub Lengths
- 250-kbits/s in Electrically Noisy Environments
- Open-Circuit Fail-Safe Receiver Design
- 1/2 Unit Load Allows for 64 Devices Connected on Bus
- Thermal Shutdown Protection
- Power-Up/-Down Glitch Protection
- Each Transceiver Meets or Exceeds the Requirements of EIA RS-485 and ISO/IEC 8482:1993(E) Standards
- Low Disabled Supply Current 300  $\mu$ A Max
- Pin Compatible with SN75176

## description

The SN75LBC184 and SN65LBC184 are differential data line transceivers in the trade-standard footprint of the SN75176 with built-in protection against high-energy noise transients. This feature provides a substantial increase in reliability for better immunity to noise transients coupled to the data cable over most existing devices. Use of these circuits provides a reliable low-cost direct-coupled (with no isolation transformer) data line interface without requiring any external components.

The SN75LBC184 and SN65LBC184 can withstand overvoltage transients of 400 W peak (typical). The conventional combination wave called out in CEI IEC 1000-4-5 simulates the overvoltage transient and models a unidirectional surge caused by overvoltages from switching and secondary lightning transients.

D OR P PACKAGE  
(TOP VIEW)



functional logic diagram (positive logic)

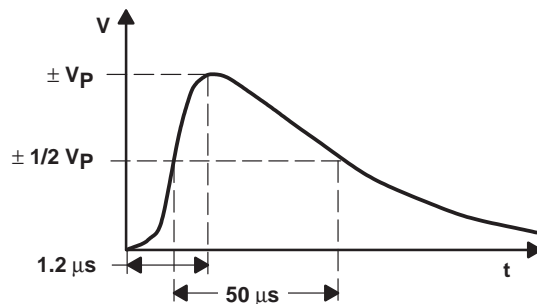
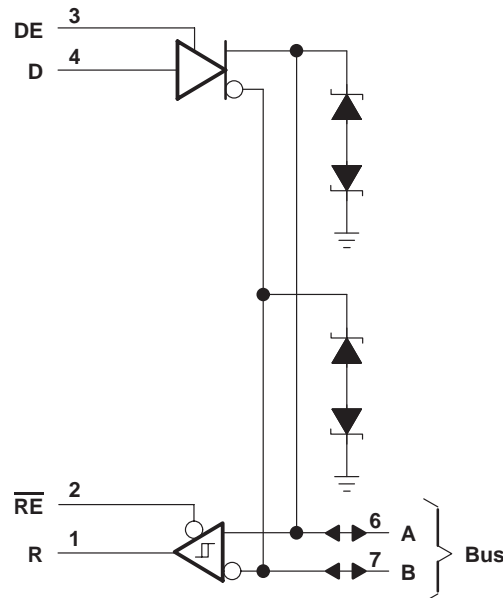


Figure 1. Surge Waveform — Combination Wave



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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## description (continued)

A biexponential function defined by separate rise and fall times for voltage and current simulates the combination wave. The standard 1.2  $\mu$ s/50  $\mu$ s combination waveform is shown in Figure 1 and in the test description in Figure 9.

The device also includes additional desirable features for party-line data buses in electrically noisy environment applications including industrial process control. The differential-driver design incorporates slew-rate-controlled outputs sufficient to transmit data up to 250 kbits/s. Slew-rate control allows longer unterminated cable runs and longer stub lengths from the main backbone than possible with uncontrolled and faster voltage transitions. A unique receiver design provides a fail-safe output of a high level when the inputs are left floating (open circuit). The SN75LBC184 and SN65LBC184 receiver also includes a high input resistance equivalent to one-half unit load allowing connection of up to 64 similar devices on the bus.

The SN75LBC184 is characterized for operation from 0°C to 70°C. The SN65LBC184 is characterized from -40°C to 85°C.

DRIVER FUNCTION TABLE

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

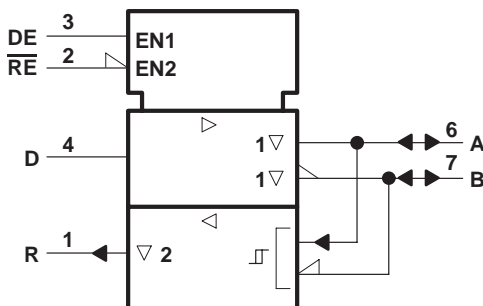
H = high level, L = low level, ? = indeterminate,  
X = irrelevant, Z = high impedance (off)

RECEIVER FUNCTION TABLE

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A - B	RE	R
$V_{ID} \geq 0.2$ V	L	H
$-0.2$ V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate,  
X = irrelevant, Z = high impedance (off)

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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**DIFFERENTIAL TRANSCEIVER**  
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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$ (see Note 1)	–0.5 V to 7 V
Continuous voltage range at any bus terminal	–15 V to 15 V
Data input/output voltage	–0.3 V to 7 V
Electrostatic discharge:	
All Terminals (Class 3 A) (see Note 3)	8 kV
All Terminals (Class 3 B) (see Note 3)	1200 V
Continuous total power dissipation (see Note 2)	Internally Limited
Operating free-air temperature range, $T_A$ : SN65LBC184	–40°C to 85°C
SN75LBC184	0°C to 70°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
  2. The driver shuts down at a junction temperature of approximately 160°C. To operate below this temperature, see the Dissipation Rating Table.
  3. GND and bus terminal ESD ratings are beyond readily available test equipment capabilities for MIL-STD-883C method 3015.3.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1150 mW	9.2 mW/°C	736 mW	598 mW

**recommended operating conditions**

		MIN	TYP	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), $V_I$ or $V_{IC}$		–7‡		12	V
High-level input voltage, $V_{IH}$	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, $V_{IL}$	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, $ V_{ID} $				12	V
High-level output current, $I_{OH}$	Driver			–60	mA
	Receiver			–8	mA
Low-level output current, $I_{OL}$	Driver			60	mA
	Receiver			4	mA
Operating free-air temperature, $T_A$	SN75LBC184	0		70	°C
	SN65LBC184	–40‡		85	°C

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for input voltage, common-mode input voltage, common-mode output voltage, and free-air temperature levels only.

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## DRIVER SECTION

### electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER	ALTERNATE SYMBOLS	TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
I <sub>CC</sub>	Supply current	DE = RE = 5 V, No Load	SN75LBC184	12	25	mA	
			SN65LBC184	12	30		
		DE = 0 V, RE = 5 V, No Load	SN75LBC184	175	300	μA	
			SN65LBC184	175	300		
I <sub>IH</sub>	High-level input current (D, DE, $\overline{RE}$ )	NA	V <sub>I</sub> = 2.4 V		±100	μA	
I <sub>IL</sub>	Low-level input current (D, DE, $\overline{RE}$ )	NA	V <sub>I</sub> = 0.4 V		±100	μA	
I <sub>OS</sub>	Short-circuit output current (see Note 5)	NA	V <sub>O</sub> = -7 V		-120	-250	mA
			V <sub>O</sub> = V <sub>CC</sub>		250		
			V <sub>O</sub> = 12 V		250		
I <sub>OZ</sub>	High-impedance output current	NA			See Receiver I <sub>I</sub>	mA	
V <sub>O</sub>	Output voltage	V <sub>Oa</sub> , V <sub>Ob</sub>	I <sub>O</sub> = 0‡		0	6	V
V <sub>OC(PP)</sub>	Peak-to-peak change in common-mode output voltage during state transitions	NA	See Figures 5 and 6		0.8		V
V <sub>OC</sub>	Common-mode output voltage	V <sub>OS</sub>	See Figure 4		1	3	V
ΔV <sub>OC(SS)</sub>	Magnitude of change, common-mode steady-state output voltage	V <sub>OS</sub> - $\overline{V}_{OS}$	See Figure 5		0.2		V
V <sub>OD</sub>	Magnitude of differential output voltage  V <sub>A</sub> - V <sub>B</sub>   (see Note 4)	V <sub>O</sub>	I <sub>O</sub> = 0		1.5	6	V
			R <sub>L</sub> = 54 Ω, See Figure 4	T <sub>A</sub> ≥ 0°C	1.5		V
				T <sub>A</sub> < 0°C	1		V
Δ V <sub>OD</sub>	Change in differential voltage magnitude between logic states	V <sub>t</sub>   - $\overline{ V_t }$	R <sub>L</sub> = 54 Ω		0.2		V

† All typical values are measured with T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5 V.

‡ I<sub>O</sub> = I<sub>ia</sub>, I<sub>ib</sub>. I<sub>ia</sub> and I<sub>ib</sub> are alternate symbols for input voltage.

NOTES: 4. The minimum V<sub>OD</sub> specification of the SN75LBC184 and the SN65LBC184 may not fully comply with ANSI RS-485 at operating temperature below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal-transmission distance.

5. This parameter is measured with only one output being driven at a time.



**DRIVER SECTION (CONTINUED)**

**switching characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{d(DH)}$	Differential output delay time, low-to-high-level output	$R_L = 54 \Omega$ , $C_L = 15 \text{ pF}$	See Figure 5				1.5	$\mu\text{s}$
$t_{d(DL)}$	Differential-output delay time, high-to-low-level output						1.5	$\mu\text{s}$
$t_{PLH}$	Propagation delay time, low-to-high-level output				0.5	1.5	$\mu\text{s}$	
$t_{PHL}$	Propagation delay time, high-to-low-level output				0.5	1.5	$\mu\text{s}$	
$t_{sk(p)}$	Pulse skew ( $ t_{d(DH)} - t_{d(DL)} $ )				75	225	ns	
$t_r$	Rise time, single ended	$R_L = 54 \Omega$ , $C_L = 15 \text{ pF}$	See Figure 5		0.25		1.8	$\mu\text{s}$
$t_f$	Fall time, single ended				0.25		1.8	$\mu\text{s}$
$t_{PZH}$	Output enable time to high level	$R_L = 110 \Omega$ ,	See Figure 2				3.5	$\mu\text{s}$
$t_{PZL}$	Output enable time to low level	$R_L = 110 \Omega$ ,	See Figure 3				3.5	$\mu\text{s}$
$t_{PHZ}$	Output disable time from high level	$R_L = 110 \Omega$ ,	See Figure 2				2	$\mu\text{s}$
$t_{PLZ}$	Output disable time from low level	$R_L = 110 \Omega$ ,	See Figure 3				2	$\mu\text{s}$

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**RECEIVER SECTION**

**electrical characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>†</sup>	MAX	UNIT
I <sub>CC</sub>	Supply current (total package)	DE = RE = 0 V, No Load			3.9	mA
		RE = 5 V, DE = 0 V, No Load			300	μA
I <sub>I</sub>	Input current	Other input = 0 V	V <sub>I</sub> = 12 V		500	μA
			V <sub>I</sub> = 12 V, V <sub>CC</sub> = 0		500	
			V <sub>I</sub> = -7 V		-400	
			V <sub>I</sub> = -7 V, V <sub>CC</sub> = 0		-400	
I <sub>OZ</sub>	High-impedance-state output current	V <sub>O</sub> = 0.4 V to 2.4 V			±100	μA
V <sub>hys</sub>	Input hysteresis voltage			70		mV
V <sub>IT+</sub>	Positive-going input threshold voltage				200	mV
V <sub>IT-</sub>	Negative-going input threshold voltage				-200 <sup>‡</sup>	mV
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -8 mA Figure 7	2.7			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4 mA Figure 7			0.5	V

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

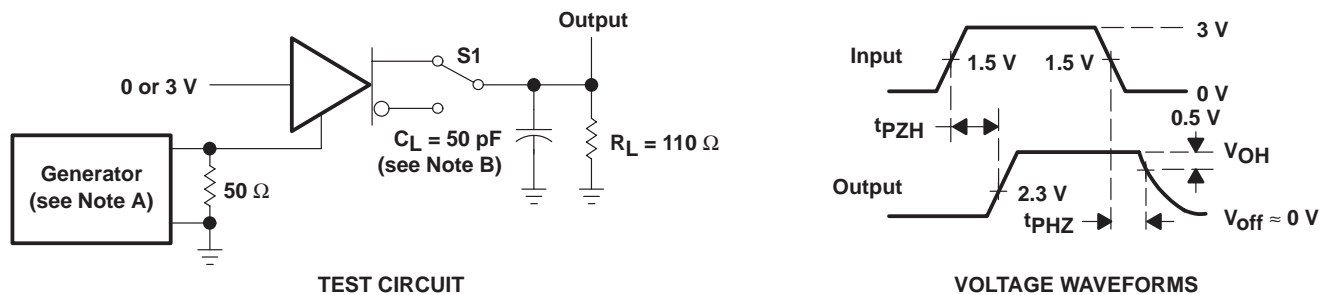
<sup>‡</sup> The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for input voltage, common-mode input voltage, common-mode output voltage and free-air temperature levels only.

**switching characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	C <sub>L</sub> = 50 pF, See Figure 7			300	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output				300	ns
t <sub>sk(p)</sub>	Pulse skew ( t <sub>PHL</sub> - t <sub>PLH</sub>  )				100	ns
t <sub>r</sub>	Rise time, single ended	See Figure 7		20		ns
t <sub>f</sub>	Fall time, single ended			20		ns
t <sub>PZH</sub>	Output enable time to high level	See Figure 8			300	ns
t <sub>PZL</sub>	Output enable time to low level				300	ns
t <sub>PHZ</sub>	Output disable time from high level				300	ns
t <sub>PLZ</sub>	Output disable time from low level				300	ns

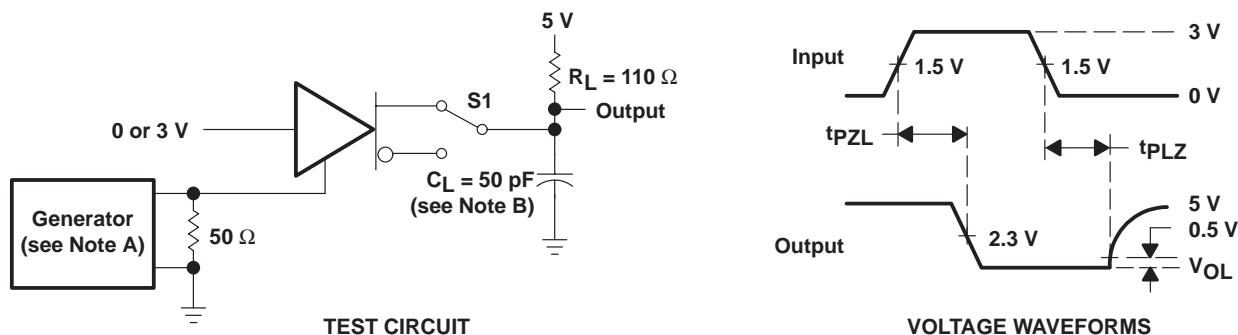


**PARAMETER MEASUREMENT INFORMATION**



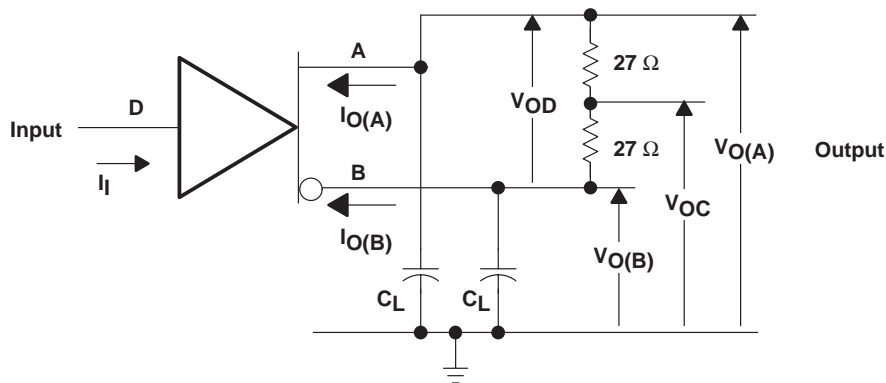
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

**Figure 2. Driver  $t_{pZH}$  and  $t_{pHZ}$  Test Circuit and Voltage Waveforms**



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

**Figure 3. Driver  $t_{pZL}$  and  $t_{pLZ}$  Test Circuit and Voltage Waveforms**



- NOTES: A. Resistance values are in ohms and are 1% tolerance.  
B.  $C_L$  includes probe and jig capacitance.

**Figure 4. Driver Test Circuit, Voltage, and Current Definitions**

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PARAMETER MEASUREMENT INFORMATION

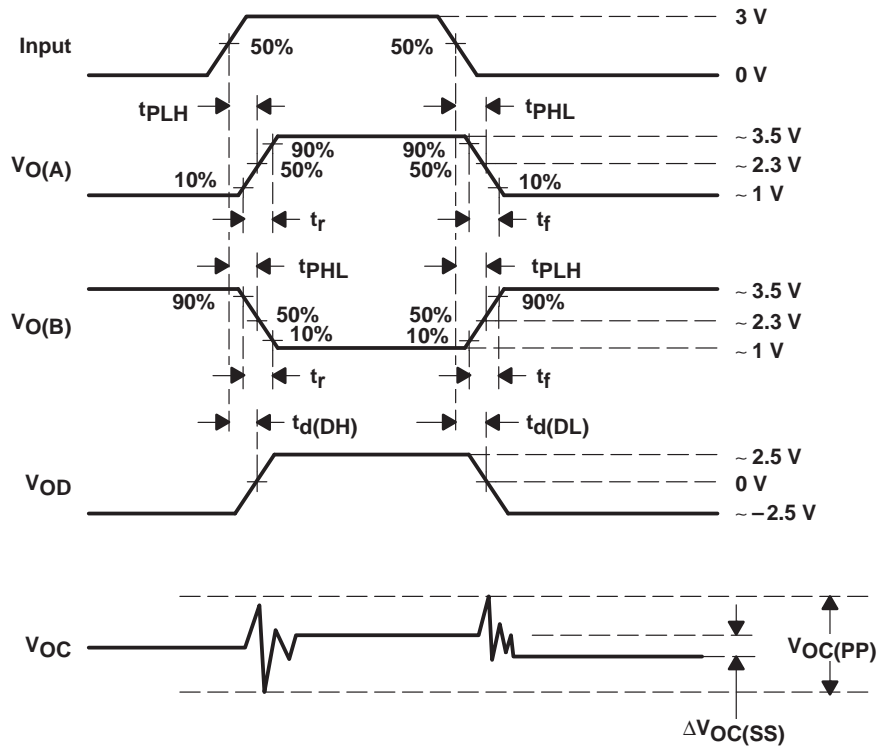
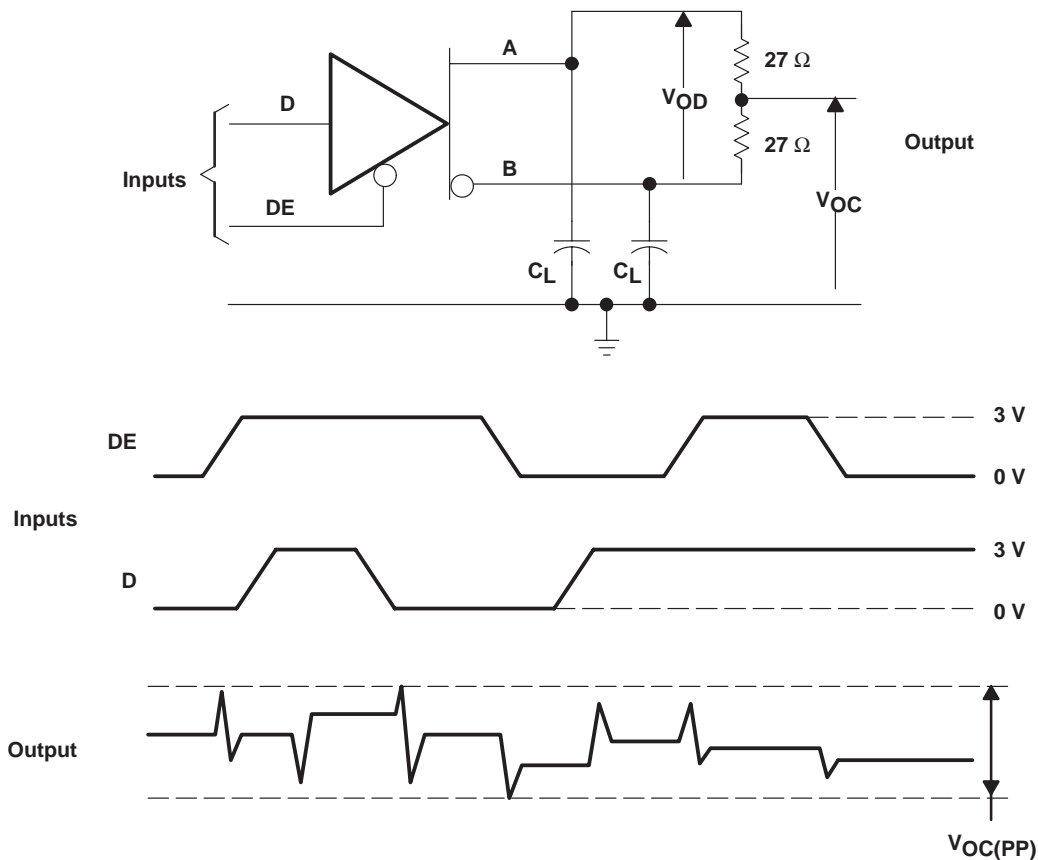


Figure 5. Driver Timing, Voltage and Current Waveforms

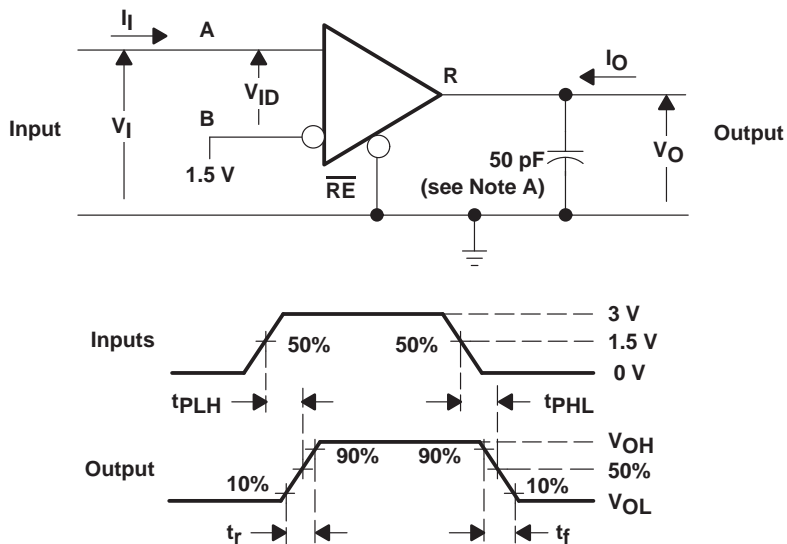


**PARAMETER MEASUREMENT INFORMATION**



NOTES: A. Resistance values are in ohms and are 1% tolerance.  
 B.  $C_L$  includes probe and jig capacitance ( $\pm 10\%$ ).

**Figure 6. Driver  $V_{OC(PP)}$  Test Circuit and Waveforms**



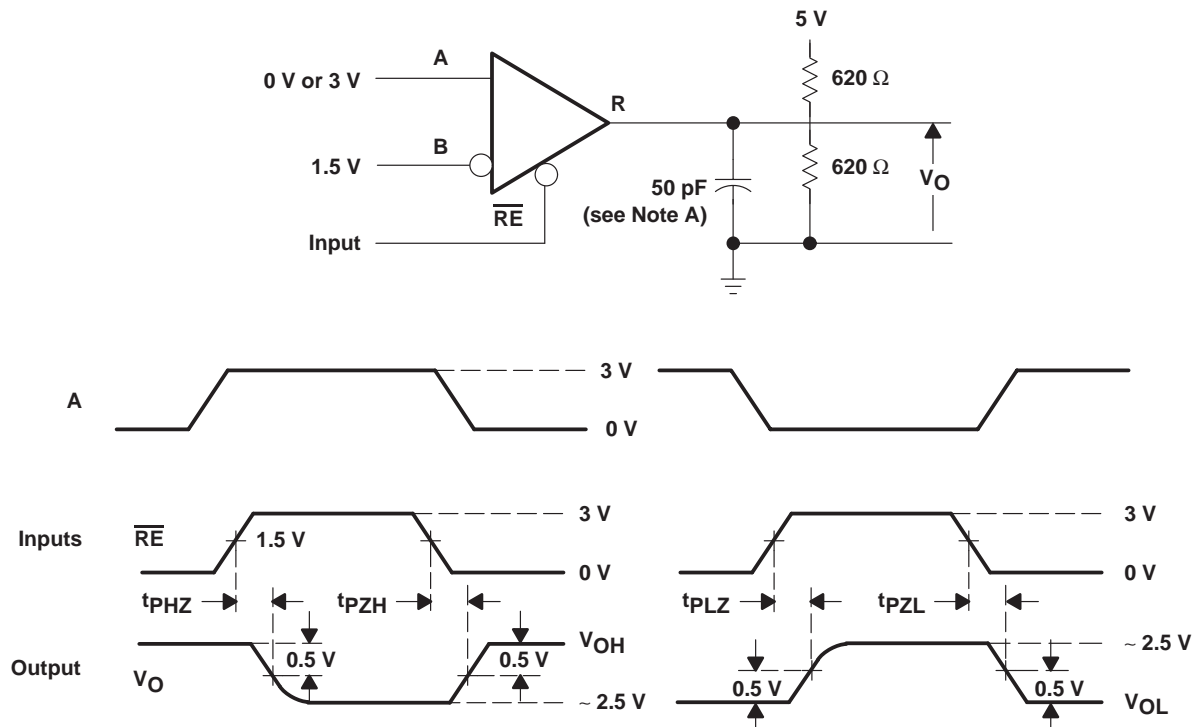
NOTE A: This value includes probe and jig capacitance ( $\pm 10\%$ ).

**Figure 7. Receiver  $t_{PLH}$  and  $t_{PHL}$  Test Circuit and Voltage Waveforms**

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PARAMETER MEASUREMENT INFORMATION



NOTE A: This value includes probe and jig capacitance ( $\pm 10\%$ ).

Figure 8. Receiver  $t_{PZL}$ ,  $t_{PLZ}$ ,  $t_{PZH}$ , and  $t_{PHZ}$  Test Circuit and Voltage Waveforms

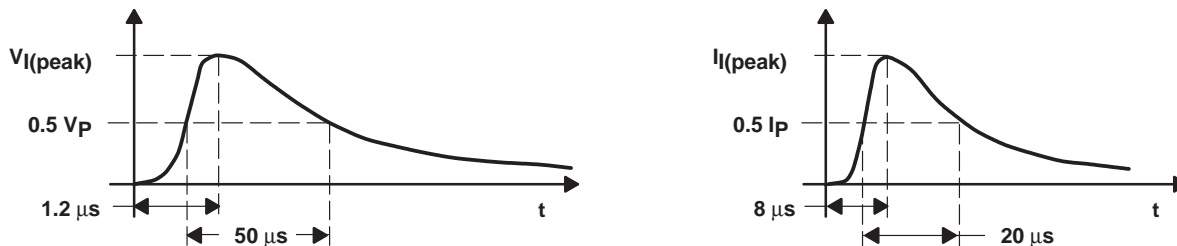
## APPLICATION INFORMATION

### 'LBC184 test description

The 'LBC184 is tested against the CEI IEC 1000–4–5 recommended transient identified as the combination wave. The combination wave provides a 1.2-/50- $\mu$ s open-circuit voltage waveform and a 8-/20- $\mu$ s short-circuit current waveform shown in Figure 9. The testing is performed with a combination/hybrid pulse generator with an effective output impedance of 2  $\Omega$ . The setup for the overvoltage stress is shown in Figure 10 with all testing performed with power applied to the 'LBC184 circuit.

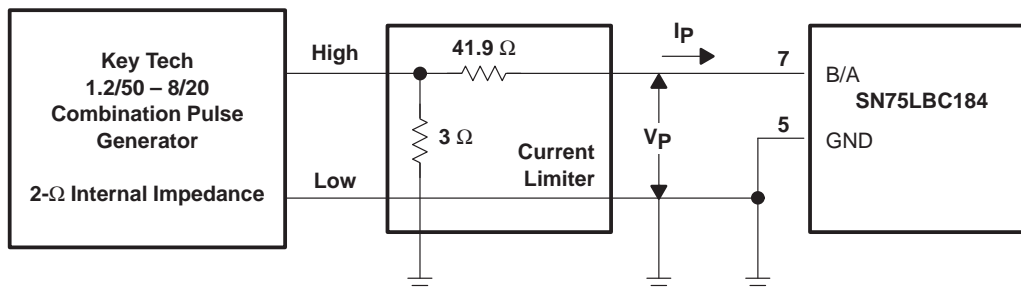
**NOTE**

High voltage transient testing is done on a sampling basis.



**Figure 9. Short-Circuit Current Waveforms**

The 'LBC184 is tested and evaluated for both maximum (single pulse) as well as life test (multiple pulse) capabilities. The 'LBC184 is evaluated against transients of both positive and negative polarity and all testing is performed with the worst-case transient polarity. Transient pulses are applied to the bus pins (A & B) across ground as shown in Figure 10.



**Figure 10. Overvoltage-Stress Test Circuit**

An example waveform as seen by the 'LBC184 is shown in Figure 11. The bottom trace is current, the middle trace shows the clamping voltage of the device and the top trace is power as calculated from the voltage and current waveforms. This example shows a peak clamping voltage of 16 V, peak current of 33.6 A yielding an absorbed peak power of 538 W.

**NOTE**

A circuit reset may be required to ensure normal data communications following a transient noise pulse of greater than 250 W peak.

APPLICATION INFORMATION

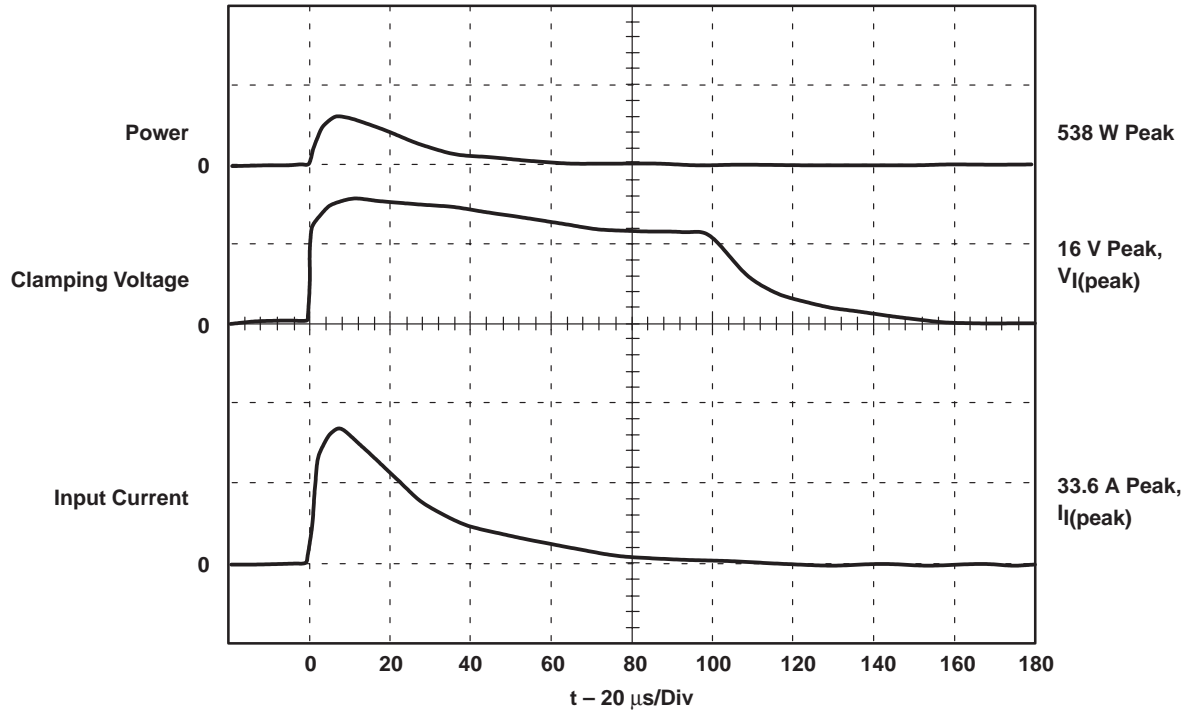


Figure 11. Typical Surge Waveform Measured At Terminals 5 and 7

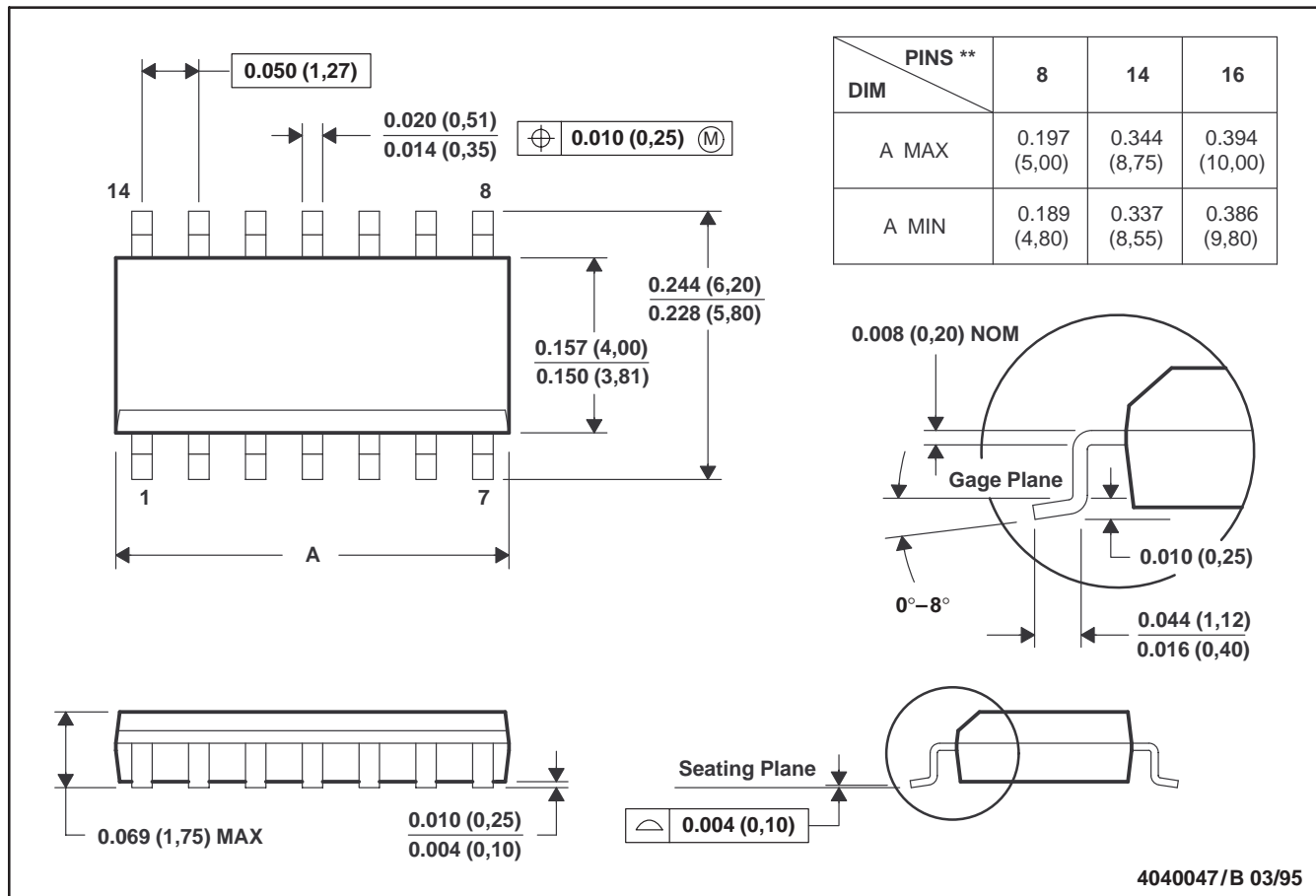
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**MECHANICAL INFORMATION**

**D (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



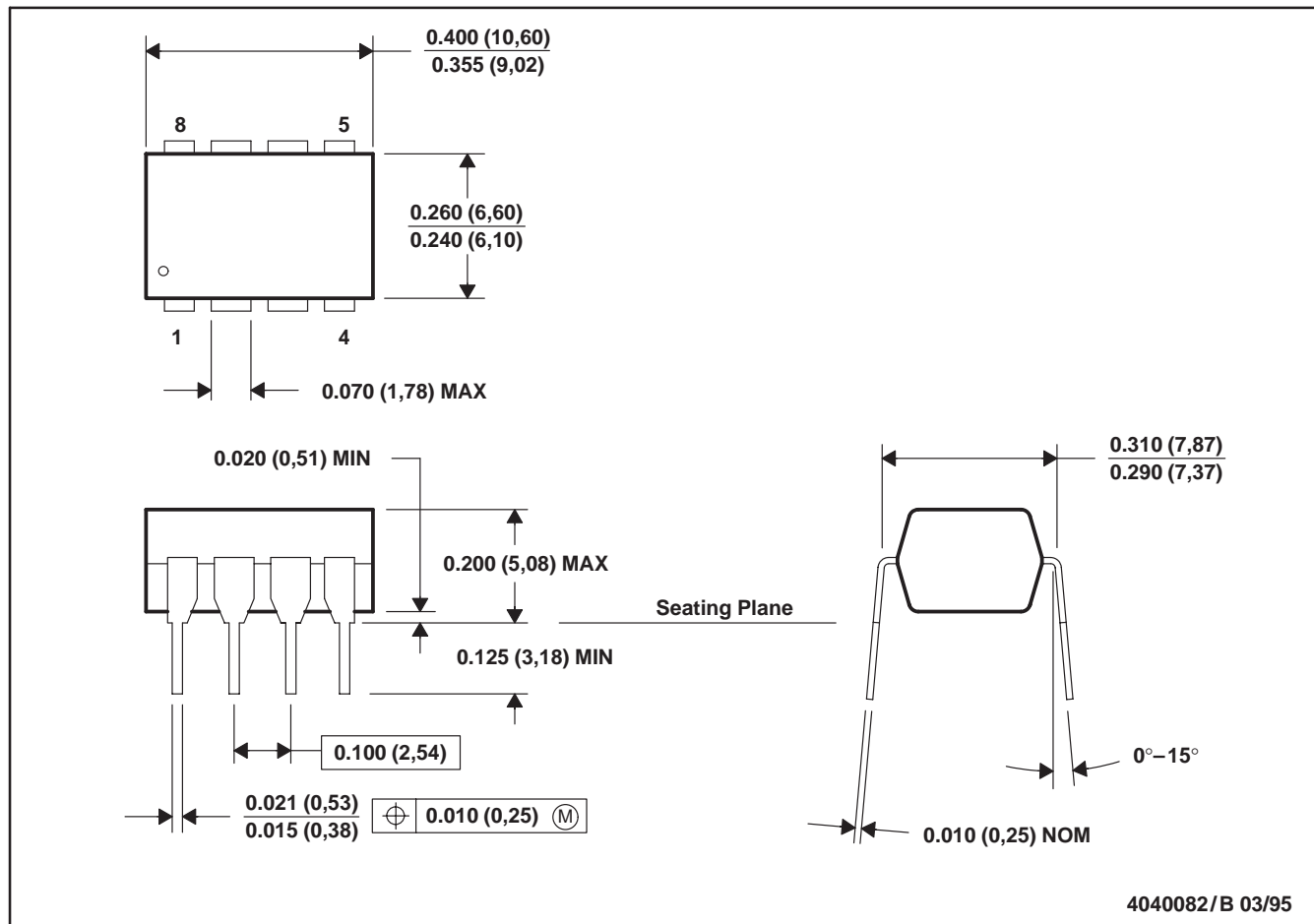
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
  - Four center pins are connected to die mount pad.
  - Falls within JEDEC MS-012

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**MECHANICAL INFORMATION**

**P (R-PDIP-T8)**

**PLASTIC DUAL-IN-LINE PACKAGE**



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

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