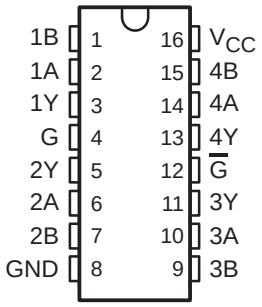
- **Designed for TIA/EIA-485, TIA/EIA-422, and ISO 8482 Applications**
- **Signaling Rate† Exceeding 50 Mbps**
- **Fail-Safe in Bus Short-Circuit, Open-Circuit, and Idle-Bus Conditions**
- **ESD Protection on Bus Inputs Exceeds 6 kV**
- **Common-Mode Bus Input Range –7 V to 12 V**
- **Propagation Delay Times <16 ns**
- **Low Standby Power Consumption <20 μA**
- **Pin-Compatible Upgrade for AM26LS32, DS96F173, LTC488, and SN75173**

SN65LBC173A (Marked as 65LBC173A)
SN75LBC173A (Marked as 75LBC173A)
D or N PACKAGE
(TOP VIEW)

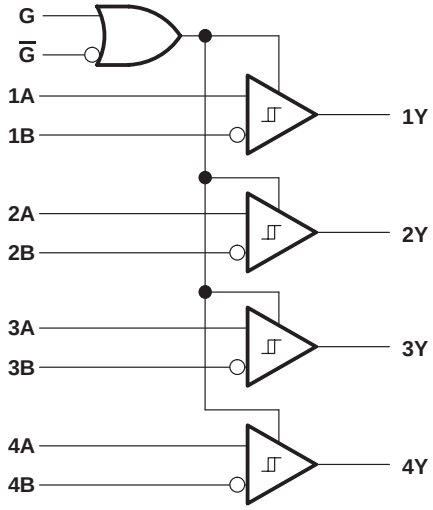


description

The SN65LBC173A and SN75LBC173A are quadruple differential line receivers with 3-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 (Euro RS-485) applications.

These devices are optimized for balanced multipoint bus communication at data rates up to and exceeding 50 million bits per second. The transmission media may be twisted-pair cables, printed-circuit board traces, or backplanes. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

logic diagram



Each receiver operates over a wide range of positive and negative common-mode input voltages, and features ESD protection to 6 kV, making it suitable for high-speed multipoint data transmission applications in harsh environments. These devices are designed using LinBiCMOS™, facilitating low power consumption and robustness.

The G and $\overline{G}$ inputs provide enable control logic for either positive- or negative-logic enabling all four drivers. When disabled or powered off, the receiver inputs present a high-impedance to the bus for reduced system loading.

The SN75LBC173A is characterized for operation over the temperature range of 0°C to 70°C. The SN65LBC173A is characterized over the temperature range from –40°C to 85°C.

LinBiCMOS is a trademark of Texas Instruments.
†The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A – B (V_{ID})	ENABLES		OUTPUT Y
	G	$\overline{G}$	
$V_{ID} \le -0.2$ V	H	X	L
	X	L	
-0.2 V $< V_{ID} < -0.01$ V	H	X	?
	X	L	
-0.01 V $\le V_{ID}$	H	X	H
	X	L	
X	L	H	Z
	OPEN	OPEN	
Short circuit	H	X	H
	X	L	
Open circuit	H	X	H

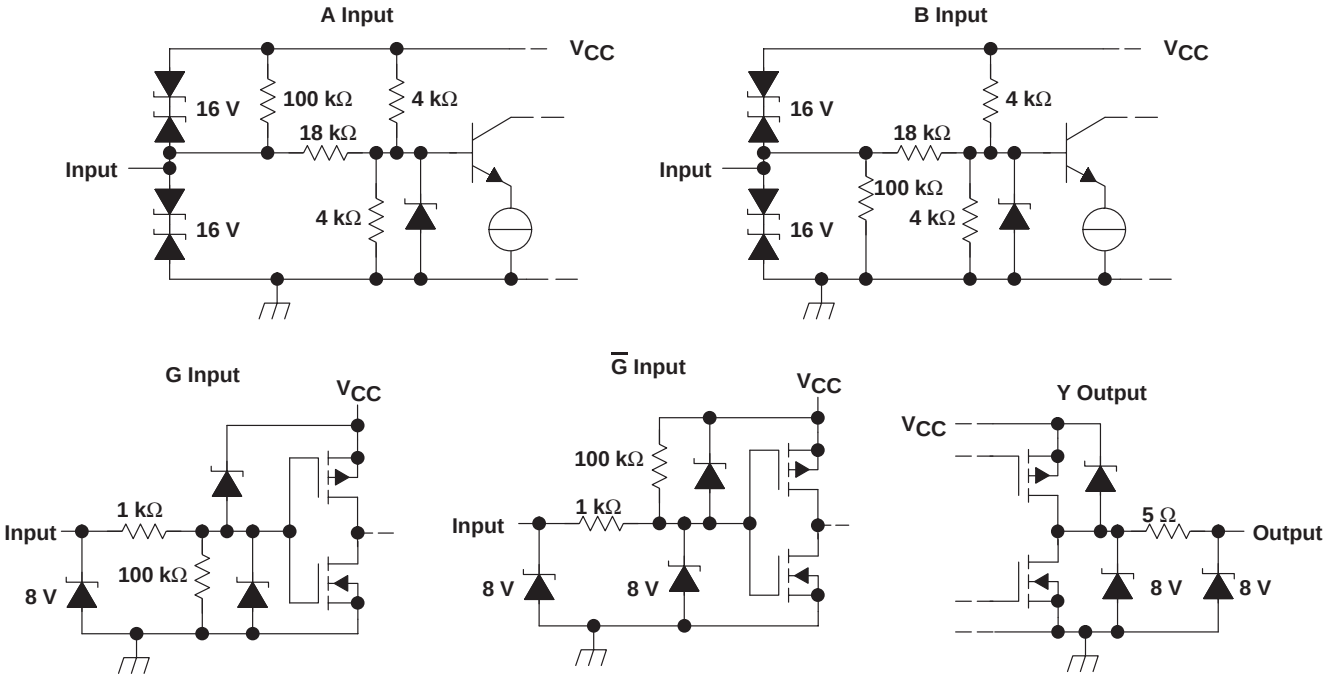
H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

AVAILABLE OPTIONS

T_A	PACKAGE	
	PLASTIC SMALL OUTLINE† (JEDEC MS-012)	PLASTIC DUAL-IN-LINE (JEDEC MS-001)
0°C to 70°C	SN75LBC173AD	SN75LBC173AN
–40°C to 85°C	SN65LBC173AD	SN65LBC173AN

† Add an R suffix for taped and reeled

equivalent input and output schematic diagrams



absolute maximum ratings†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.3 V to 6 V
Voltage range at any bus input (DC) . . . . . –10 V to 15 V
Voltage range at any bus input (transient pulse through 100 Ω, see Figure 5) . . . . . –30 V to 30 V
Voltage input range at G and $\overline{G}$, V_I . . . . . –0.5 V to V_{CC} + 0.5 V
Electrostatic discharge:
Human body model (see Note 2): A and B to GND . . . . . 6 kV
All pins . . . . . 5 kV
Charged-device model (see Note 3): All pins . . . . . 2 kV
Storage temperature range . . . . . –65°C to 150°C
Continuous power dissipation . . . . . See Power Dissipation Rating Table
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to GND, and are steady-state (unless otherwise specified).
2. Tested in accordance with JEDEC Standard 22, Test Method A114-A.
3. Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	1080 mW	8.7 mW/°C	690 mW	560 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal	A, B	–7		12	V
High-level input voltage, V_{IH}	G, $\overline{G}$	2		V_{CC}	V
Low-level input voltage, V_{IL}	G, $\overline{G}$	0		0.8	V
Output current	Y	–8		8	mA
Operating free-air temperature, T_A	SN75LBC173A	0		70	°C
	SN65LBC173A	–40		85	°C

electrical characteristics over recommended operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold		$-7\ V \le V_{CM} \le 12\ V$ ($V_{CM} = (V_A + V_B)/2$)			–80	–10	mV
V_{IT-}	Negative-going differential input voltage threshold				–200	–120		
V_{HYS}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					40		mV
V_{IK}	Input clamp voltage		I_I = –18 mA		–1.5	–0.8		V
V_{OH}	High-level output voltage		V_{ID} = 200 mV, I_{OH} = –8 mA	See Figure 1	2.7	4.8		V
V_{OL}	Low-level output voltage		V_{ID} = –200 mV, I_{OL} = 8 mA			0.2	0.4	
I_{OZ}	High-impedance-state output current		V_O = 0 V to V_{CC}		–1		1	µA
I_I	Line input current		Other input at 0 V, V_{CC} = 0 V or 5 V	V_I = 12 V			0.9	mA
				V_I = –7 V	–0.7			
I_{IH}	High-level input current	Enable inputs G, $\overline{G}$					100	µA
I_{IL}	Low-level input current				–100			µA
R_I	Input resistance	A, B inputs			12			kΩ
I_{CC}	Supply current		V_{ID} = 5 V	G at 0 V, $\overline{G}$ at V_{CC}			20	µA
			No load	G at V_{CC}, $\overline{G}$ at 0 V		11	16	mA

† All typical values are at V_{CC} = 5 V and 25°C.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_r	Output rise time	V_{ID} = –3 V to 3 V, See Figure 2		2	4	ns
t_f	Output fall time			2	4	ns
t_{PLH}	Propagation delay time, low-to-high level output		9	12	16	ns
t_{PHL}	Propagation delay time, high-to-low level output		9	12	16	ns
t_{PZH}	Propagation delay time, high-impedance to high-level output	See Figure 3		27	38	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output			7	16	ns
t_{PZL}	Propagation delay time, high-impedance to low level output	See Figure 4		29	38	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output			12	16	ns
$t_{sk(p)}$	Pulse skew ($\lvert (t_{PLH} - t_{PHL}) \rvert$)			0.2	1	ns
$t_{sk(o)}$	Output skew (see Note 4)				2	ns
$t_{sk(pp)}$	Part-to-part skew (see Note 5)				2	ns

† All typical values are at V_{CC} = 5 V and 25°C.

NOTES: 4. Outputs skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.

5. Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

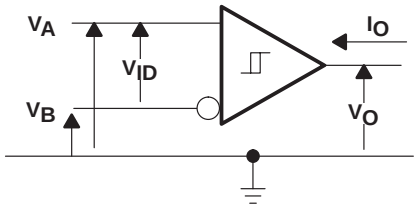
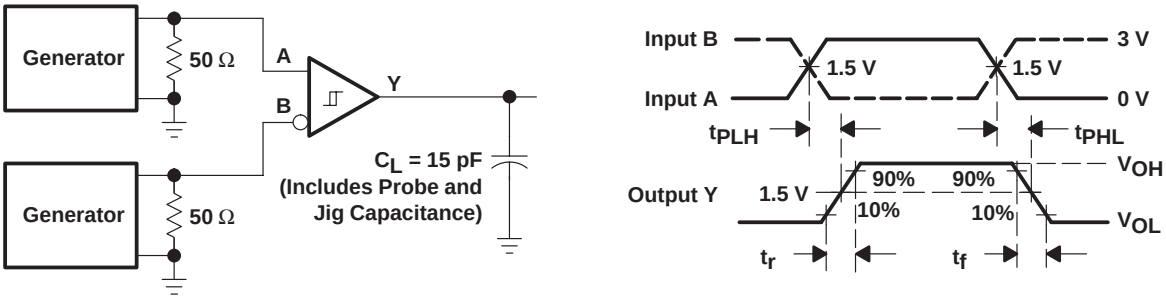
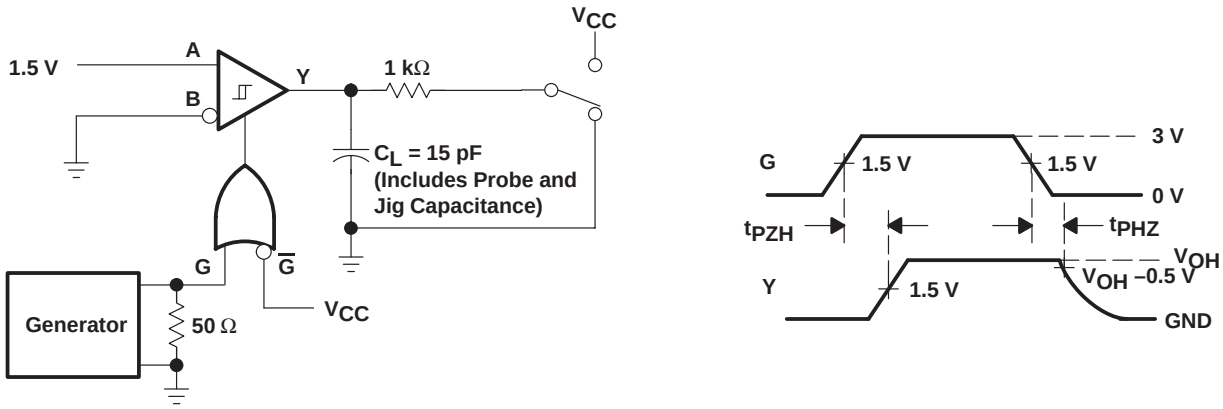


Figure 1. Voltage and Current Definitions



Generators: PRR = 1 MHz, 50% Duty Cycle,
t_r <6 ns, Z_O = 50 Ω

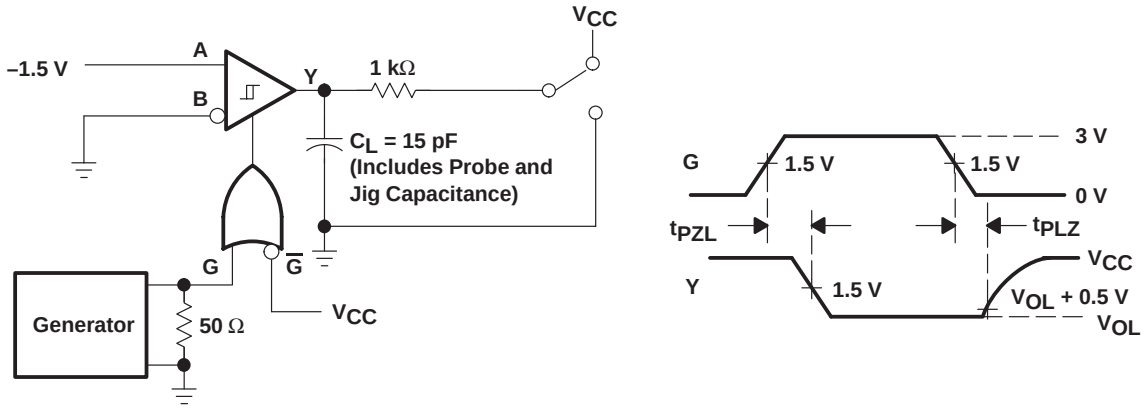
Figure 2. Switching Test Circuit and Waveforms



Generators: PRR = 1 MHz, 50% Duty Cycle,
t_r <6 ns, Z_O = 50 Ω

Figure 3. Test Circuit Waveforms, t_{PZH} and t_{PHZ}

PARAMETER MEASUREMENT INFORMATION



Generators: PRR = 1 MHz, 50% Duty Cycle, t_r <6 ns, Z_O = 50 Ω

Figure 4. Test Circuit Waveforms, t_{PZL} and t_{PLZ}

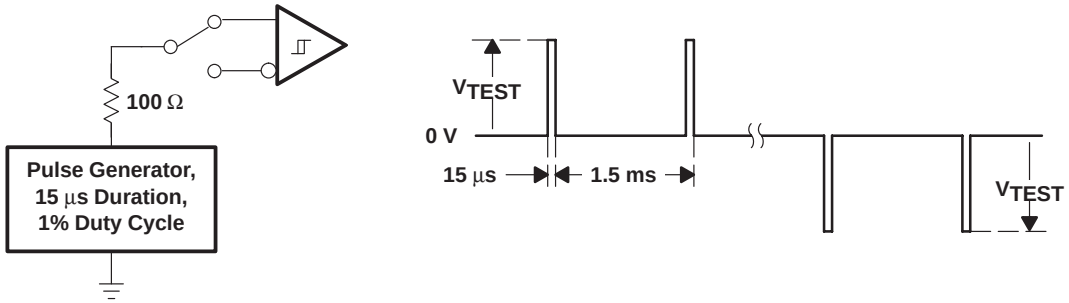


Figure 5. Test Circuit and Waveform, Transient Over-Voltage Test

TYPICAL CHARACTERISTICS

BUS INPUT CURRENT vs BUS INPUT VOLTAGE

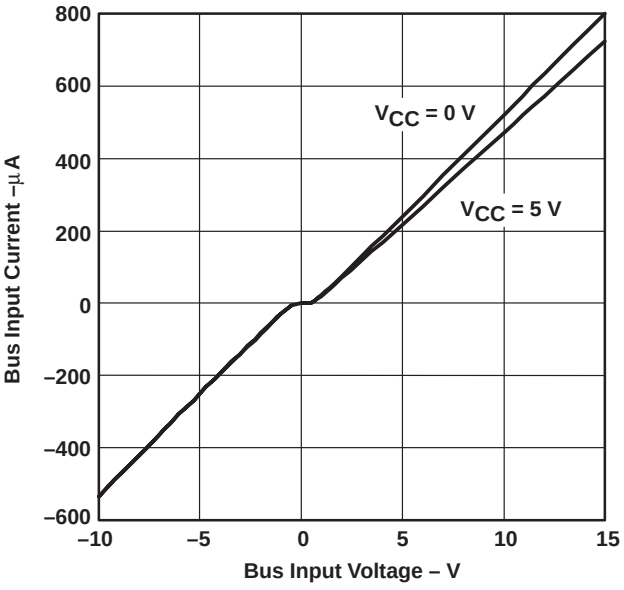


Figure 6

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

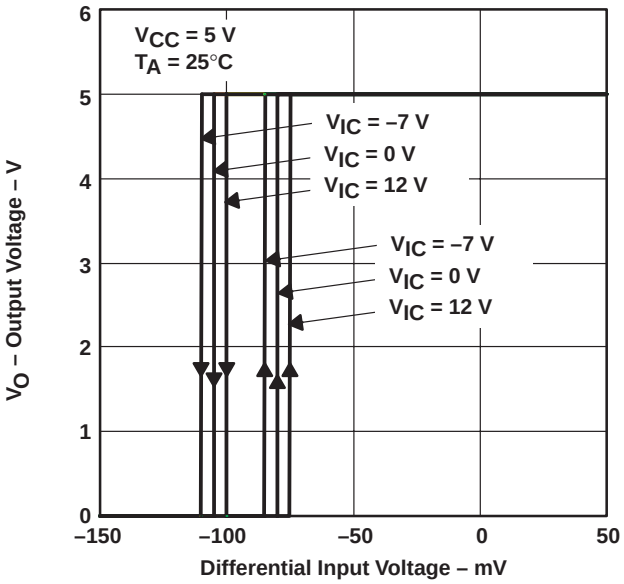


Figure 7

SUPPLY CURRENT vs SIGNALING RATE (ALL FOUR CHANNELS)

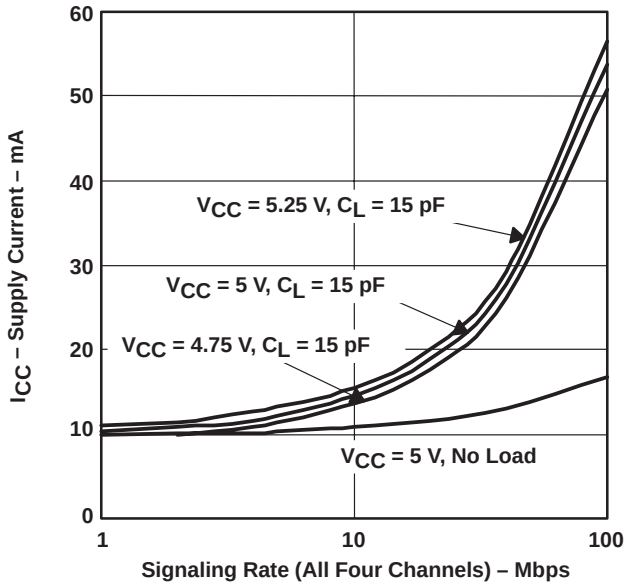


Figure 8

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

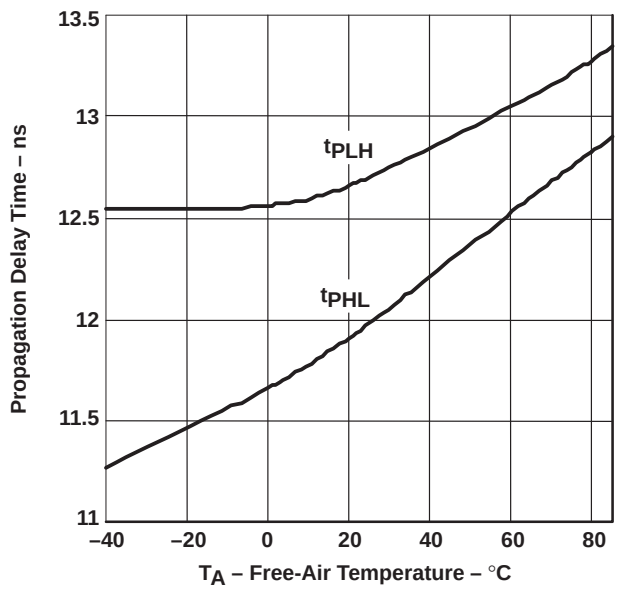


Figure 9

TYPICAL CHARACTERISTICS

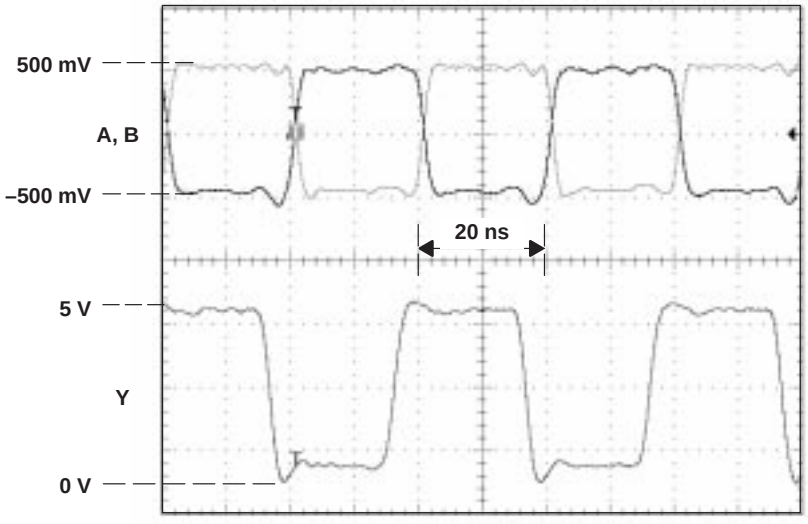


Figure 10. Receiver Inputs and Outputs, 50 Mbps Signaling Rate

APPLICATION INFORMATION

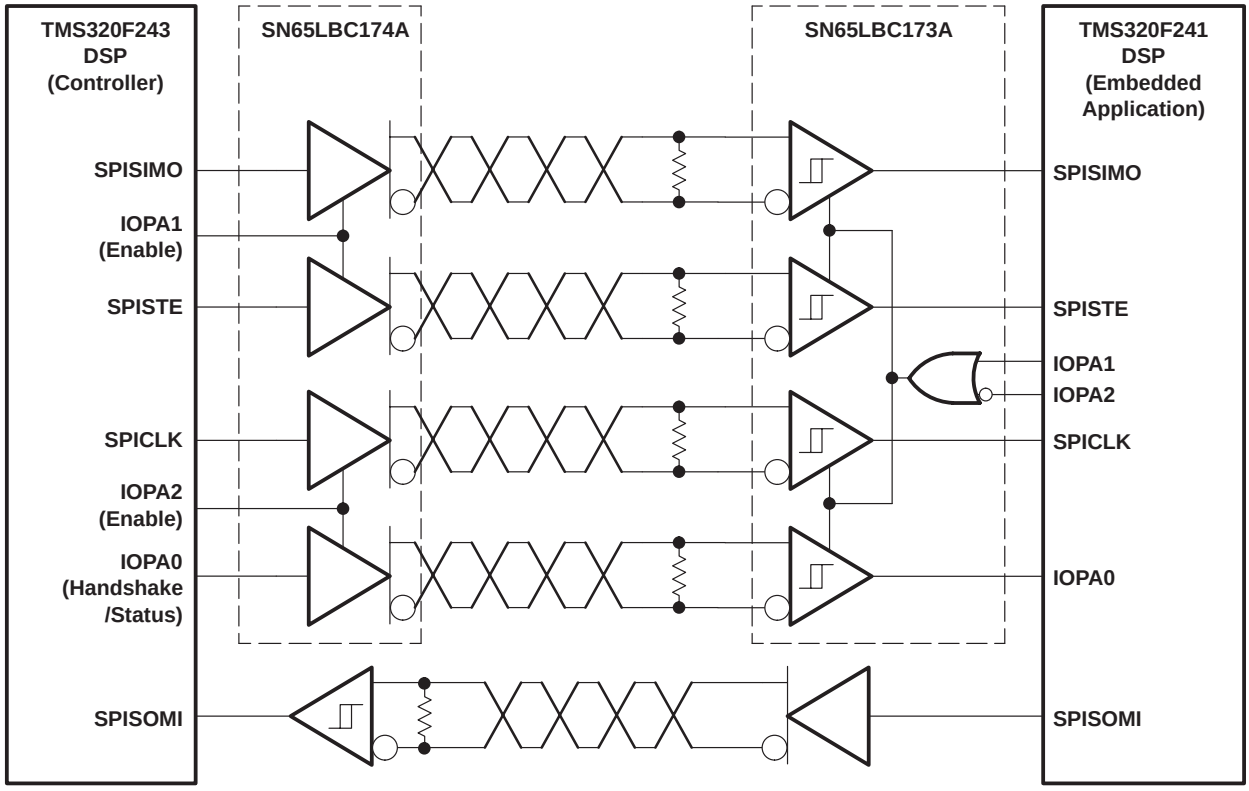


Figure 11. Typical Application Circuit, DSP-to-DSP Link via Serial Peripheral Interface

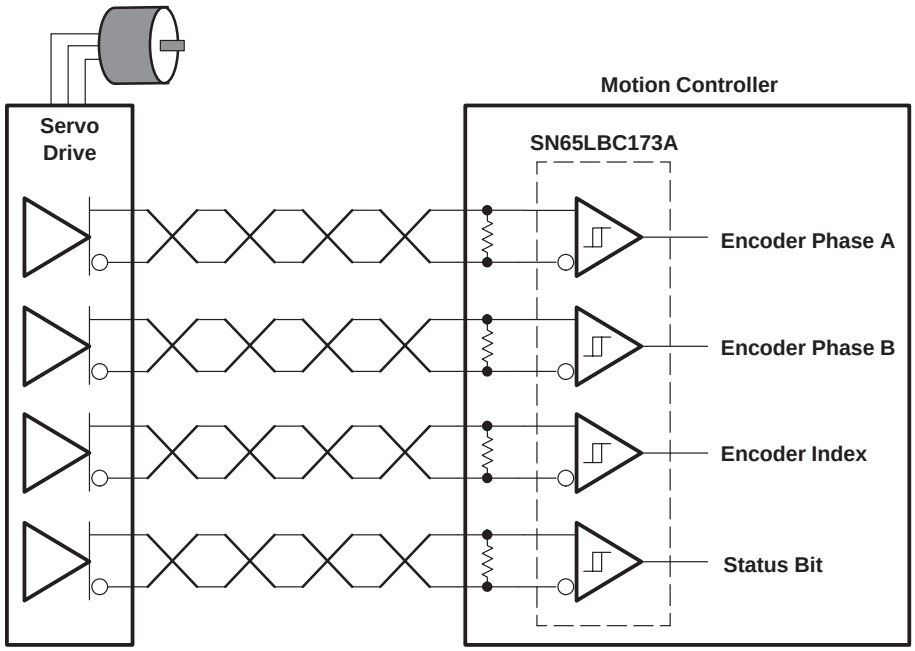
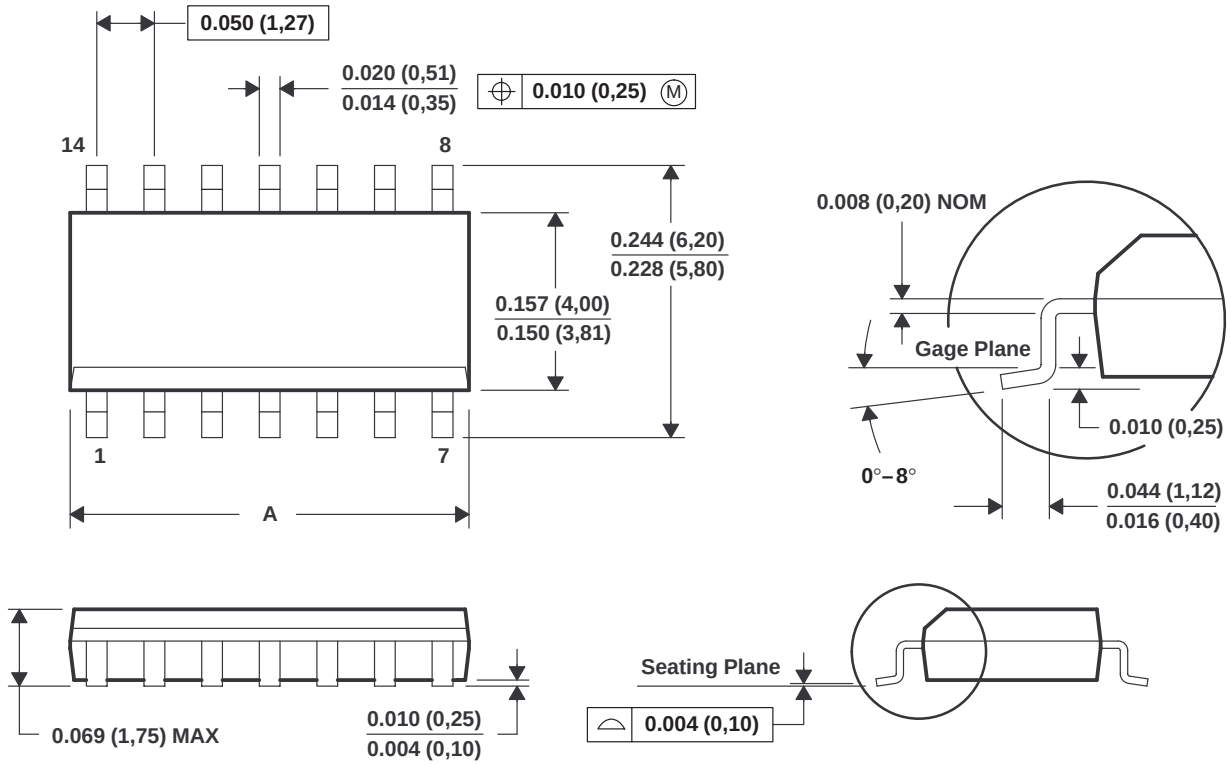


Figure 12. Typical Application Circuit, High-Speed Servomotor Encoder Interface

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

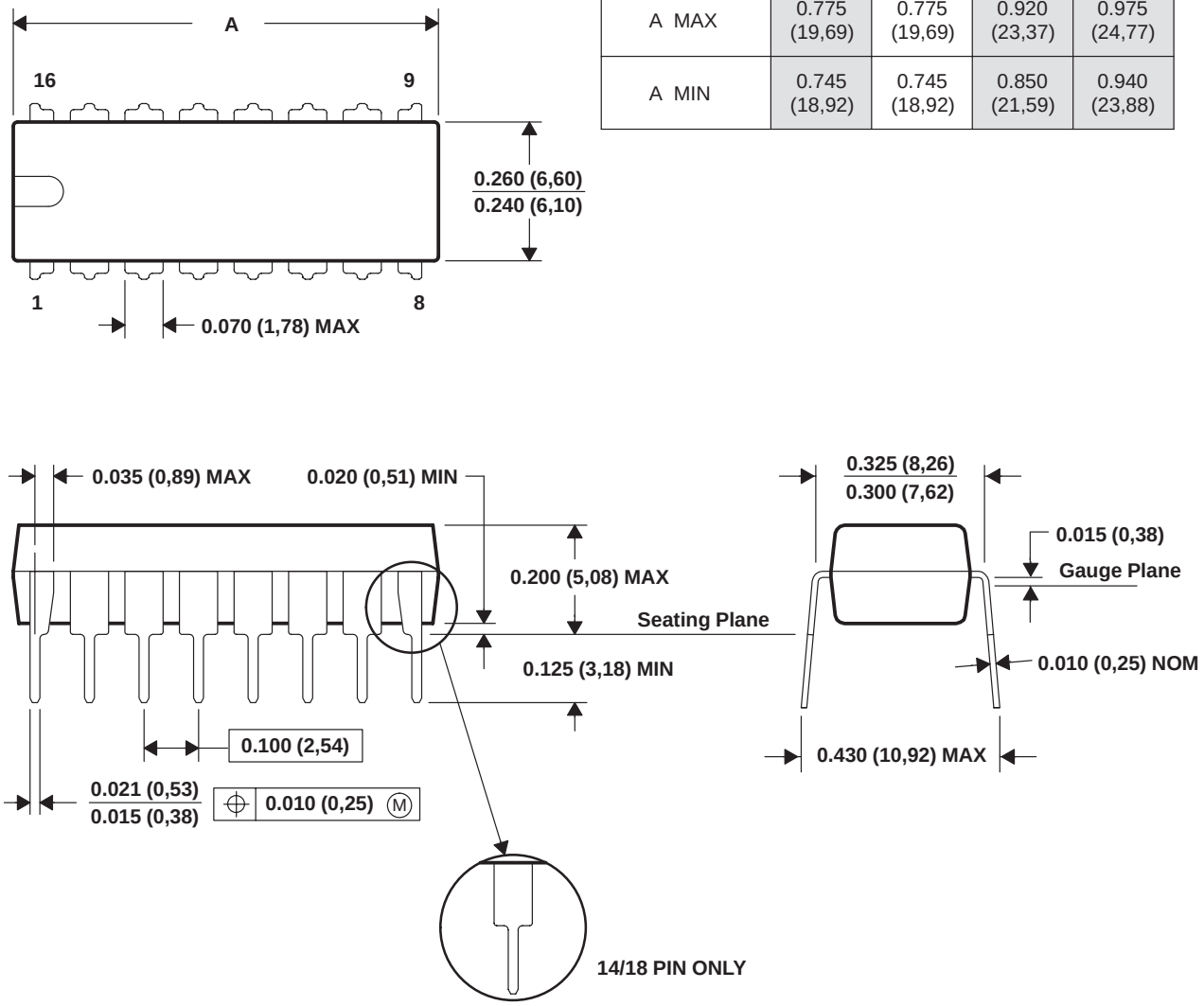
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, license, warranty or endorsement thereof.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Resale of TI's products or services with *statements different from or beyond the parameters* stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Also see: Standard Terms and Conditions of Sale for Semiconductor Products. www.ti.com/sc/docs/stdterms.htm

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265