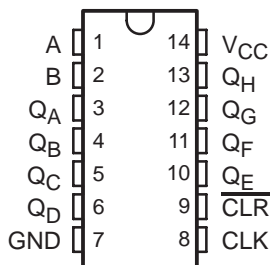


# SN54LV164A, SN74LV164A 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

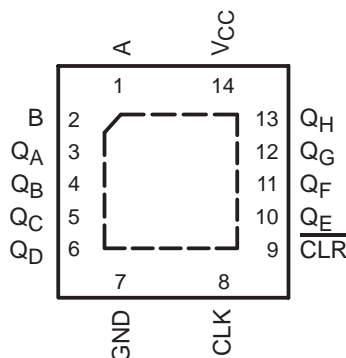
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- 2-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 10.5 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2.3$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

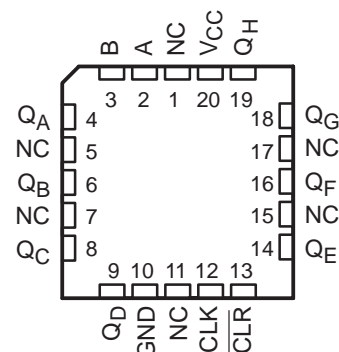
SN54LV164A ... J OR W PACKAGE  
SN74LV164A ... D, DB, DGV, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LV164A ... RGY PACKAGE  
(TOP VIEW)



SN54LV164A ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'LV164A devices are 8-bit parallel-out serial shift registers designed for 2-V to 5.5-V  $V_{CC}$  operation.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV164ARGYR	LV164A
	SOIC – D	Tube of 50	SN74LV164AD	LV164A
		Reel of 2500	SN74LV164ADR	
	SOP – NS	Reel of 2000	SN74LV164ANSR	74LV164A
	SSOP – DB	Reel of 2000	SN74LV164ADBR	LV164A
	TSSOP – PW	Tube of 90	SN74LV164APW	LV164A
		Reel of 2000	SN74LV164APWR	
Reel of 250		SN74LV164APWT		
TVSOP – DGV	Reel of 2000	SN74LV164ADGVR	LV164A	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV164AJ	SNJ54LV164AJ
	CFP – W	Tube of 150	SNJ54LV164AW	SNJ54LV164AW
	LCCC – FK	Tube of 55	SNJ54LV164AFK	SNJ54LV164AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
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# SN54LV164A, SN74LV164A 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

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## description/ordering information (continued)

These devices feature AND-gated serial (A and B) inputs and an asynchronous clear ( $\overline{\text{CLR}}$ ) input. The gated serial inputs permit complete control over incoming data, as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock (CLK) input.

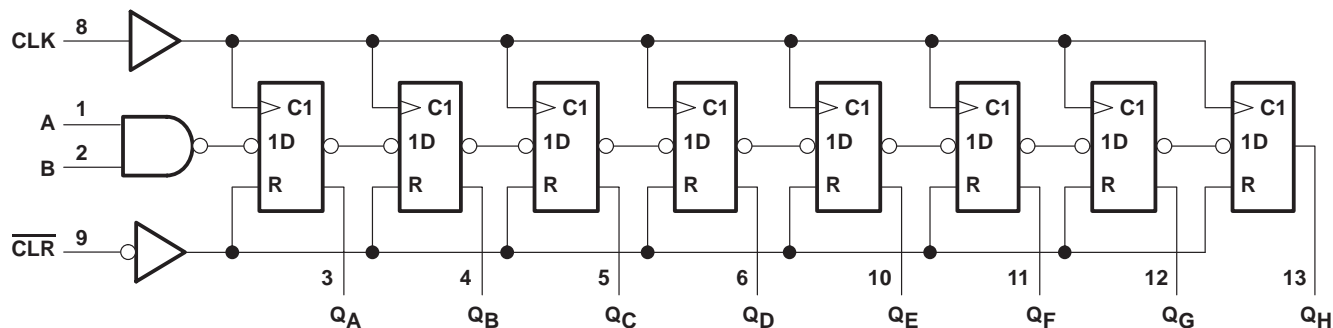
FUNCTION TABLE

INPUTS				OUTPUTS		
$\overline{\text{CLR}}$	CLK	A	B	$Q_A$	$Q_B \dots Q_H$	
L	X	X	X	L	L	L
H	L	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$
H	$\uparrow$	H	H	H	$Q_{An}$	$Q_{Gn}$
H	$\uparrow$	L	X	L	$Q_{An}$	$Q_{Gn}$
H	$\uparrow$	X	L	L	$Q_{An}$	$Q_{Gn}$

$Q_{A0}$ ,  $Q_{B0}$ ,  $Q_{H0}$  = the level of  $Q_A$ ,  $Q_B$ , or  $Q_H$ , respectively, before the indicated steady-state input conditions were established.

$Q_{An}$ ,  $Q_{Gn}$  = the level of  $Q_A$  or  $Q_G$  before the most recent  $\uparrow$  transition of the clock: indicates a 1-bit shift.

## logic diagram (positive logic)

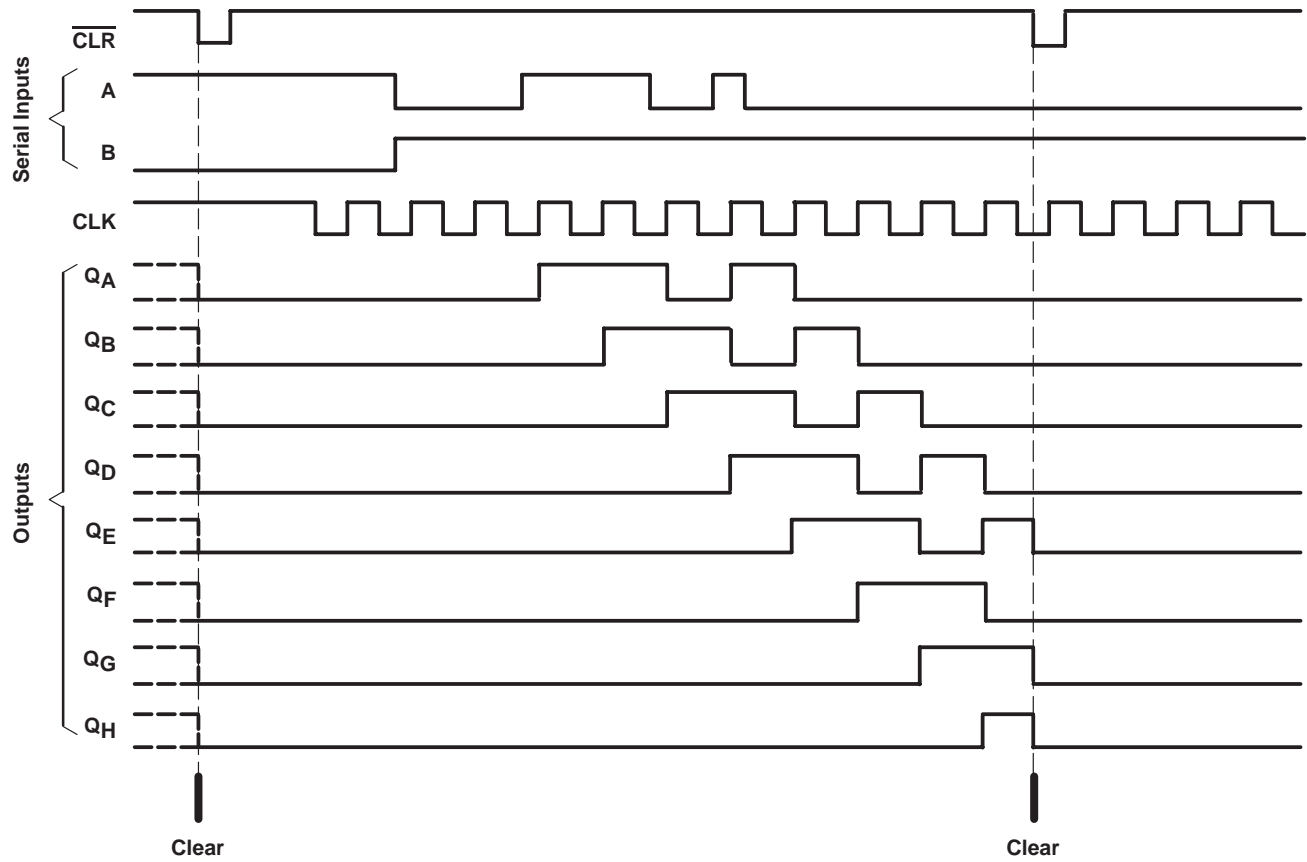


Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

# SN54LV164A, SN74LV164A 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

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## typical clear, shift, and clear sequences



# SN54LV164A, SN74LV164A

## 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package .....	86°C/W
(see Note 3): DB package .....	96°C/W
(see Note 3): DGV package .....	127°C/W
(see Note 3): NS package .....	76°C/W
(see Note 3): PW package .....	113°C/W
(see Note 4): RGY package .....	47°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
  2. This value is limited to 5.5 V maximum.
  3. The package thermal impedance is calculated in accordance with JESD 51-7.
  4. The package thermal impedance is calculated in accordance with JESD 51-5.



# SN54LV164A, SN74LV164A

## 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

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### recommended operating conditions (see Note 5)

		SN54LV164A		SN74LV164A		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	1.5		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7	V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5	0.5	V
		V <sub>CC</sub> = 2.3 V to 2.7 V		V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 3 V to 3.6 V		V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 4.5 V to 5.5 V		V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		-50	-50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		-2	-2	mA
		V <sub>CC</sub> = 3 V to 3.6 V		-6	-6	
		V <sub>CC</sub> = 4.5 V to 5.5 V		-12	-12	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50	50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		2	2	mA
		V <sub>CC</sub> = 3 V to 3.6 V		6	6	
		V <sub>CC</sub> = 4.5 V to 5.5 V		12	12	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V		200	200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V		100	100	
		V <sub>CC</sub> = 4.5 V to 5.5 V		20	20	
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 5: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LV164A			SN74LV164A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V to 5.5 V	V <sub>CC</sub> -0.1			V <sub>CC</sub> -0.1			V
	I <sub>OH</sub> = -2 mA	2.3 V	2			2			
	I <sub>OH</sub> = -6 mA	3 V	2.48			2.48			
	I <sub>OH</sub> = -12 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I <sub>OL</sub> = 2 mA	2.3 V			0.4			0.4	
	I <sub>OL</sub> = 6 mA	3 V			0.44			0.44	
	I <sub>OL</sub> = 12 mA	4.5 V			0.55			0.55	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±1			±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			20			20	μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V				5			5	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		2.2			2.2		pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



# SN54LV164A, SN74LV164A 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

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timing requirements over recommended operating free-air temperature range,  $V_{CC} = 2.5 V \pm 0.2 V$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54LV164A		SN74LV164A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	$\overline{CLR}$ low	6	6.5	6.5	6.5	ns	
		CLK high or low	6.5	7.5	7.5			
$t_{su}$	Setup time	Data before CLK $\uparrow$	6.5	8.5	8.5	ns		
		$\overline{CLR}$ inactive	3	3	3			
$t_h$	Hold time	Data after CLK $\uparrow$	-0.5	0	0	ns		

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3 V \pm 0.3 V$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54LV164A		SN74LV164A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	$\overline{CLR}$ low	5	5	5	5	ns	
		CLK high or low	5	5	5			
$t_{su}$	Setup time	Data before CLK $\uparrow$	5	6	6	ns		
		$\overline{CLR}$ inactive	2.5	2.5	2.5			
$t_h$	Hold time	Data after CLK $\uparrow$	0	0	0	ns		

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5 V \pm 0.5 V$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54LV164A		SN74LV164A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	$\overline{CLR}$ low	5	5	5	5	ns	
		CLK high or low	5	5	5			
$t_{su}$	Setup time	Data before CLK $\uparrow$	4.5	4.5	4.5	ns		
		$\overline{CLR}$ inactive	2.5	2.5	2.5			
$t_h$	Hold time	Data after CLK $\uparrow$	1	1	1	ns		

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 2.5 V \pm 0.2 V$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ C$			SN54LV164A		SN74LV164A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			$C_L = 15 \text{ pF}$	55*	105*		50*		50	MHz	
			$C_L = 50 \text{ pF}$	45	85		40		40		
$t_{pd}$	CLK	Q	$C_L = 15 \text{ pF}$	9.2*	17.6*		1*	20*	1	20	ns
$t_{PHL}$	$\overline{CLR}$	Q		8.6*	16*		1*	18*	1	18	
$t_{pd}$	CLK	Q	$C_L = 50 \text{ pF}$	11.5	21.1		1	24	1	24	ns
$t_{PHL}$	$\overline{CLR}$	Q		10.8	19.5		1	22	1	22	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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# SN54LV164A, SN74LV164A 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

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**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV164A		SN74LV164A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	80*	155*		65*		65		MHz
			$C_L = 50\text{ pF}$	50	120		45		45		
$t_{\text{pd}}$	CLK	Q	$C_L = 15\text{ pF}$		6.4*	12.8*	1*	15*	1	15	ns
$t_{\text{PHL}}$	$\overline{\text{CLR}}$				6*	12.8*	1*	15*	1	15	
$t_{\text{pd}}$	CLK	Q	$C_L = 50\text{ pF}$		8.3	16.3	1	18.5	1	18.5	ns
$t_{\text{PHL}}$	$\overline{\text{CLR}}$				7.9	16.3	1	18.5	1	18.5	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV164A		SN74LV164A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	125*	220*		105*		105		MHz
			$C_L = 50\text{ pF}$	85	165		75		75		
$t_{\text{pd}}$	CLK	Q	$C_L = 15\text{ pF}$		4.5*	9*	1*	10.5*	1	10.5	ns
$t_{\text{PHL}}$	$\overline{\text{CLR}}$				4.2*	8.6*	1*	10*	1	10	
$t_{\text{pd}}$	CLK	Q	$C_L = 50\text{ pF}$		6	11	1	12.5	1	12.5	ns
$t_{\text{PHL}}$	$\overline{\text{CLR}}$				5.8	10.6	1	12.5	1	12.5	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**noise characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 6)**

PARAMETER		SN74LV164A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.28	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.22	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		3.09		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 6: Characteristics are for surface-mount packages only.

**operating characteristics,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS		$V_{CC}$	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ ,	$f = 10\text{ MHz}$	3.3 V	48.1	pF
				5 V	47.5	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

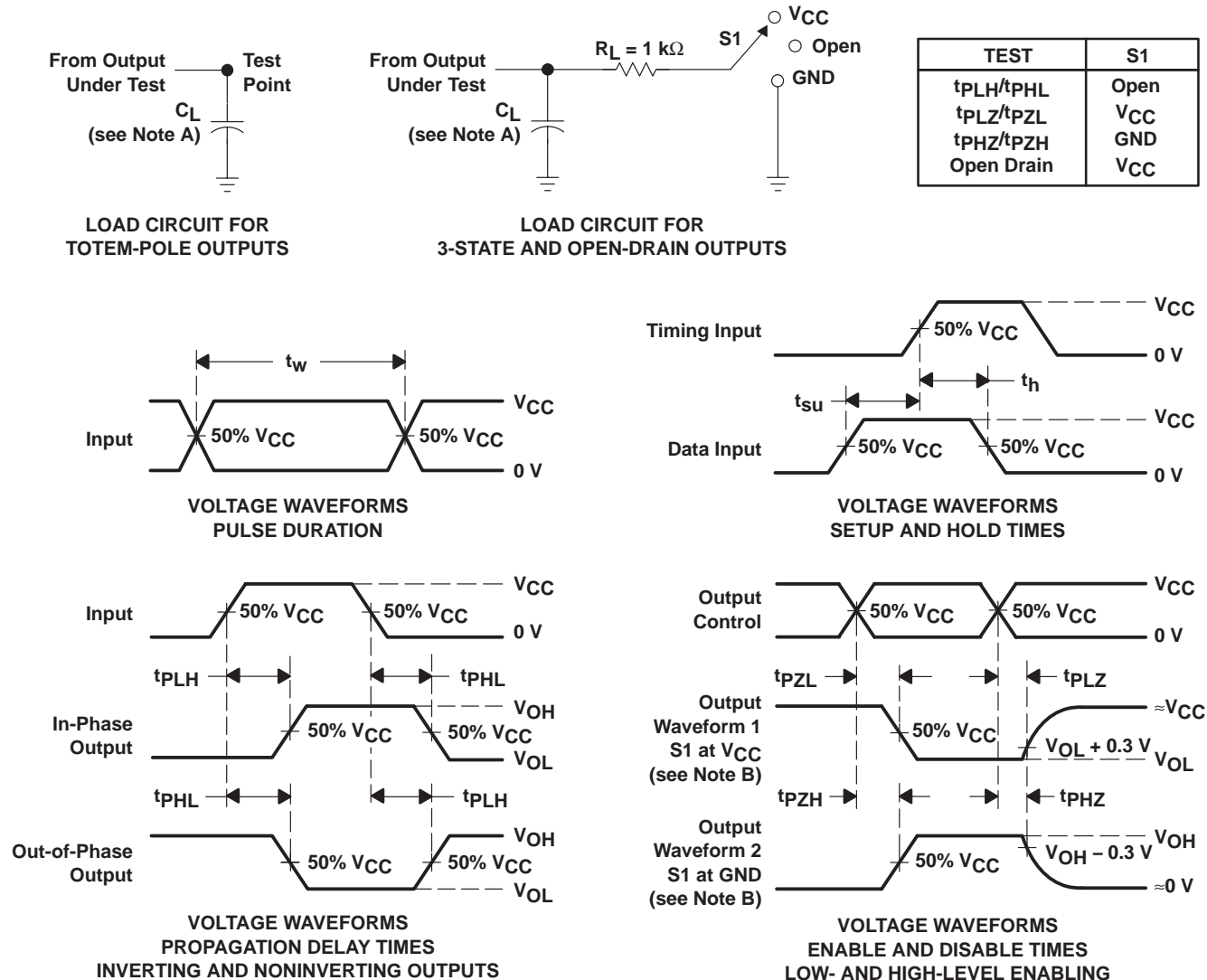


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# SN54LV164A, SN74LV164A 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LV164AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV164ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV164ADBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV164ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV164ADGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV164ADGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV164ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV164ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV164ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV164ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV164APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV164APWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV164APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV164APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV164APWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV164APWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV164ARGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE





- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AB.

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



4203539-2/G 04/2005

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance.
  -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - F. Package complies to JEDEC MO-241 variation BA.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



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