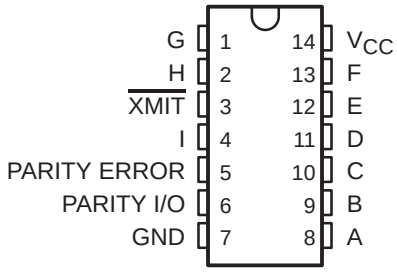
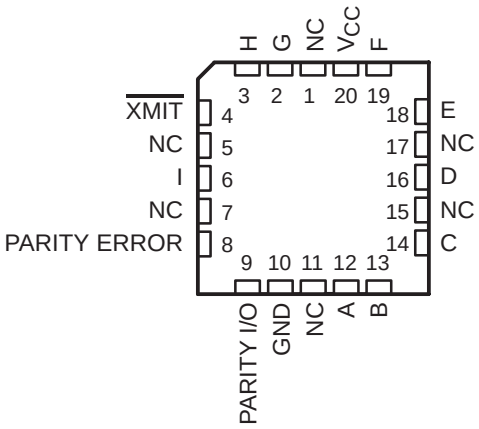
- **Generate Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bit Parity**
- **Direct Bus Connection for Parity Generation or Checking by Using the Parity I/O Port**
- **Glitch-Free Bus During Power Up/Down**
- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AS286 . . . J PACKAGE
SN74AS286 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS286 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN54AS286 and SN74AS286 universal 9-bit parity generators/checkers feature a local output for parity checking and a 48-mA bus-driving parity input/output (I/O) port for parity generation/checking. The word-length capability is easily expanded by cascading.

The transmit ($\overline{\text{XMIT}}$) control input is implemented specifically to accommodate cascading. When $\overline{\text{XMIT}}$ is low, the parity tree is disabled and PARITY ERROR remains at a high logic level regardless of the input levels. When $\overline{\text{XMIT}}$ is high, the parity tree is enabled. PARITY ERROR indicates a parity error when either an even number of inputs (A–I) are high and PARITY I/O is forced to a low logic level, or when an odd number of inputs are high and PARITY I/O is forced to a high logic level.

The I/O control circuitry was designed so that the I/O port remains in the high-impedance state during power up or power down to prevent bus glitches.

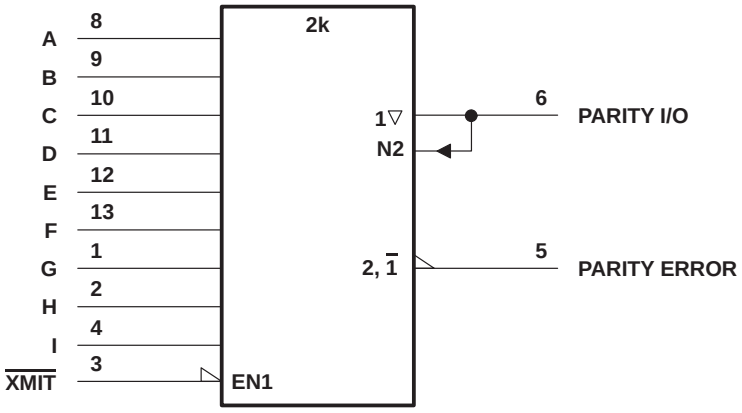
The SN54AS286 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AS286 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

NUMBER OF INPUTS (A–I) THAT ARE HIGH	$\overline{\text{XMIT}}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	L
1, 3, 5, 7, 9	h	h	L
	h	l	H

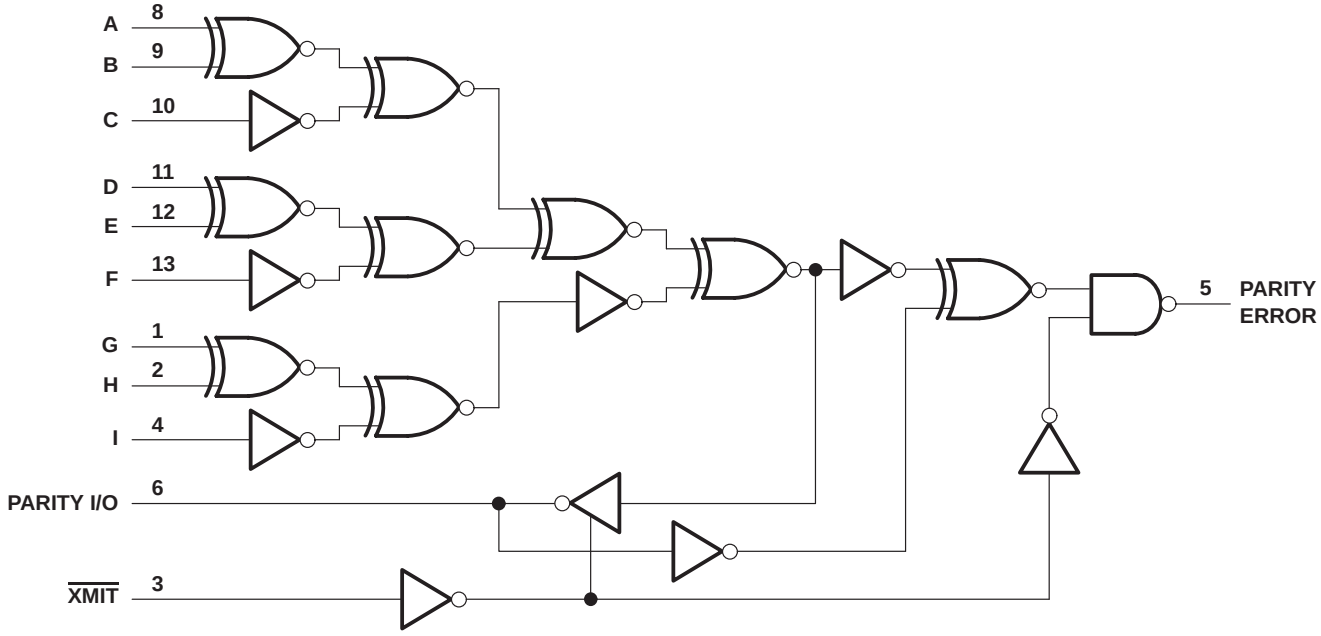
h = high input level l = low input level
H = high output level L = low output level

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54AS286 . . . . . –55°C to 125°C
SN74AS286 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54AS286			SN74AS286			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	PARITY ERROR			–2			–2	mA
		PARITY I/O			–12			–15	
I_{OL}	Low-level output current	PARITY ERROR			20			20	mA
		PARITY I/O			32			48	
T_A	Operating free-air temperature		–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS286			SN74AS286			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC} –2			V_{CC} –2			V
	PARITY I/O	V_{CC} = 4.5 V	I_{OH} = –3 mA	2.4	2.9		2.4	3		
			I_{OH} = –12 mA	2.4						
			I_{OH} = –15 mA				2.4			
V_{OL}	PARITY ERROR	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
	PARITY I/O		I_{OL} = 32 mA			0.5				
			I_{OL} = 48 mA						0.5	
I_I	PARITY I/O	V_{CC} = 5.5 V	V_I = 5.5 V			0.1			0.1	mA
	All other inputs		V_I = 7 V			0.1			0.1	
I_{IH}	PARITY I/O§	V_{CC} = 5.5 V,	V_I = 2.7 V			50			50	µA
	All other inputs					20			20	
I_{IL}	PARITY I/O§	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.5			–0.5	mA
	All other inputs					–0.5			–0.5	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	–30		–112	mA
I_{CC}	Transmit	V_{CC} = 5.5 V			30	43		30	43	mA
	Receive				35	50		35	50	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

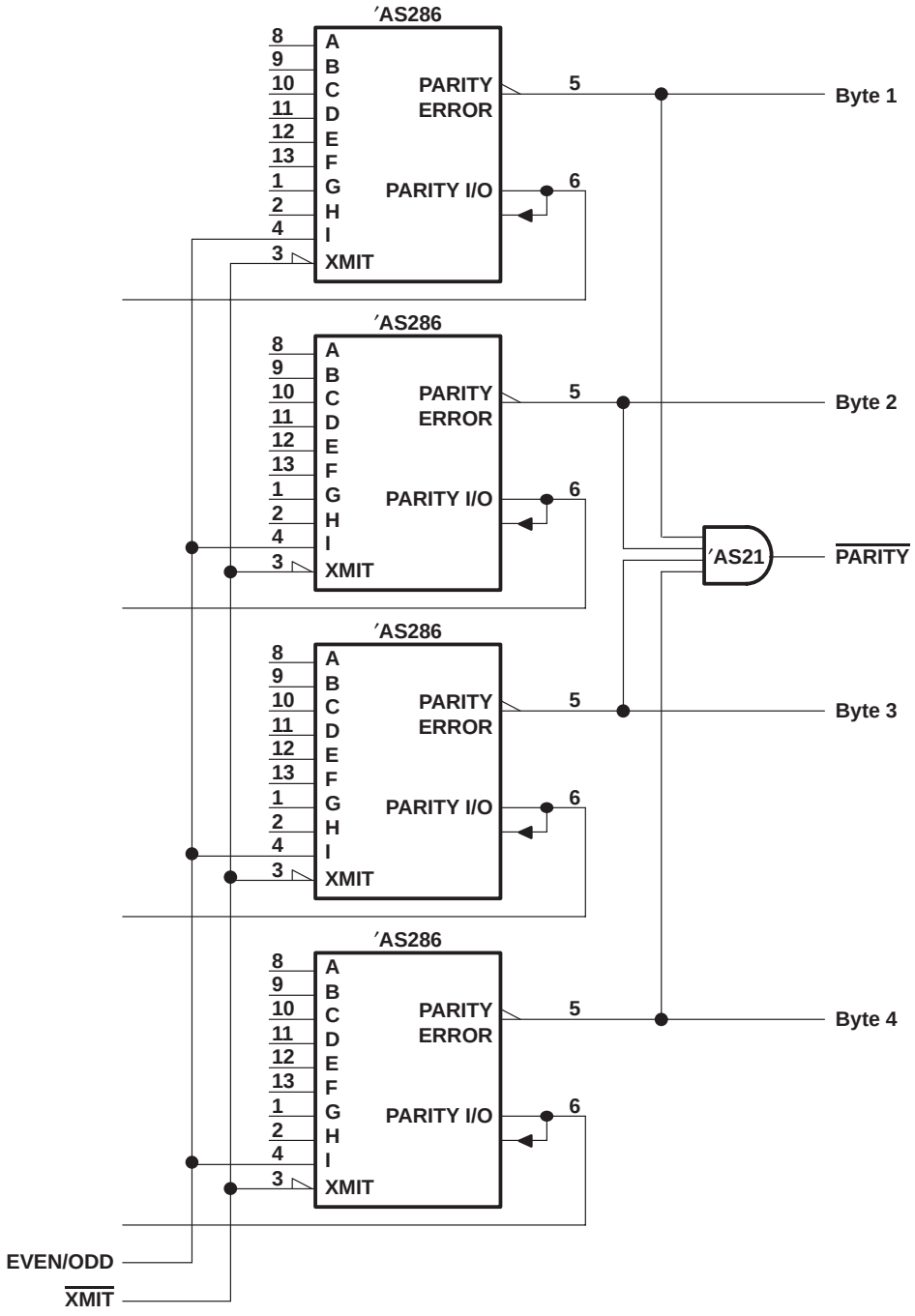
switching characteristics (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54AS286		SN74AS286		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any A – I	PARITY I/O	3	17	3	15	ns
t_{PHL}			3	15	3	14	
t_{PLH}	Any A – I	PARITY ERROR	3	20	3	16.5	ns
t_{PHL}			3	18	3	16.5	
t_{PLH}	PARITY I/O	PARITY ERROR	3	10	3	9	ns
t_{PHL}			3	10	3	9	
t_{PZH}	$\overline{XMIT}$	PARITY I/O	3	14	3	13	ns
t_{PZL}			3	17	3	16	
t_{PHZ}	$\overline{XMIT}$	PARITY I/O	3	13	3	11.5	ns
t_{PLZ}			3	11	3	10	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

APPLICATION INFORMATION

Figure 1 shows a 32-bit parity generator/checker with output polarity switching, parity-error detection, and parity on every byte.

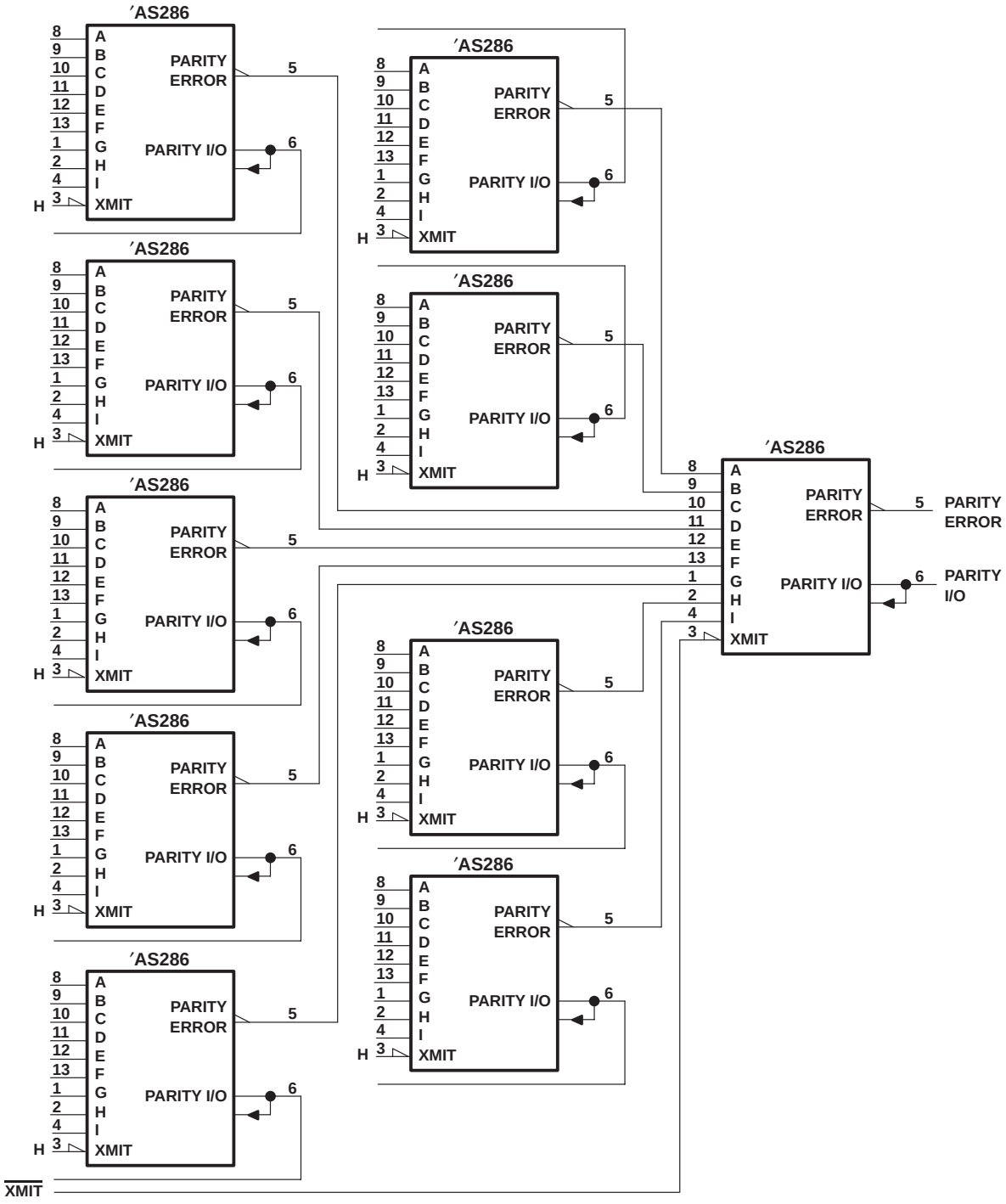


Pin numbers shown are for the D, J, and N packages.

Figure 1. 32-Bit Parity Generator/Checker

APPLICATION INFORMATION

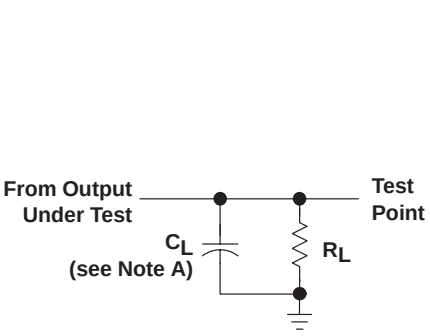
Figure 2 shows a 90-bit parity generator/checker with $\overline{\text{XMIT}}$ on the last stage available for use with parity detection.



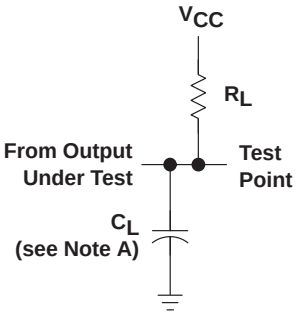
Pin numbers shown are for the D, J, and N packages.

Figure 2. 90-Bit Parity Generator/Checker With Parity-Error Detection

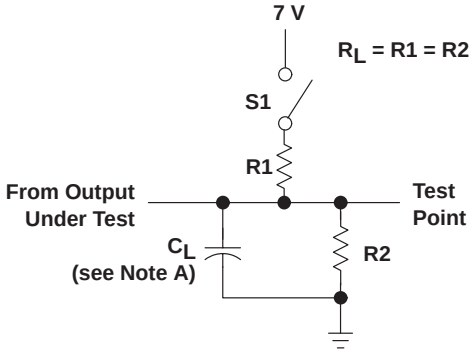
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



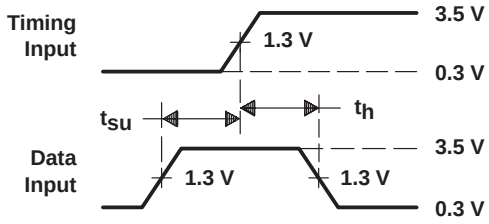
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



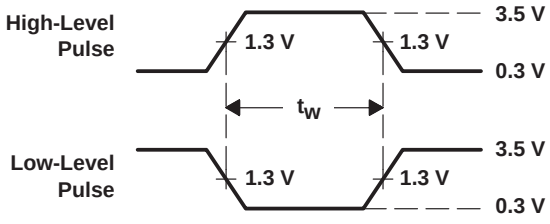
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



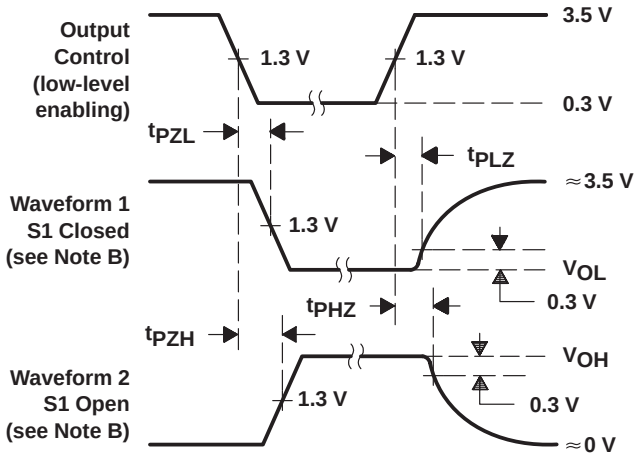
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



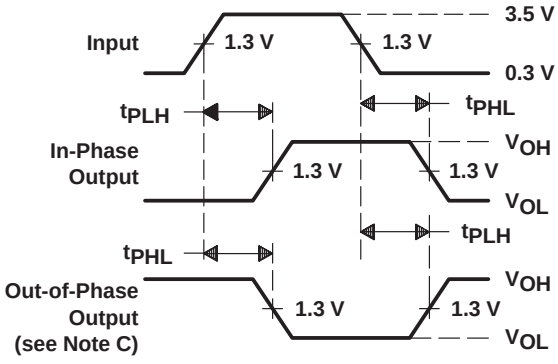
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

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