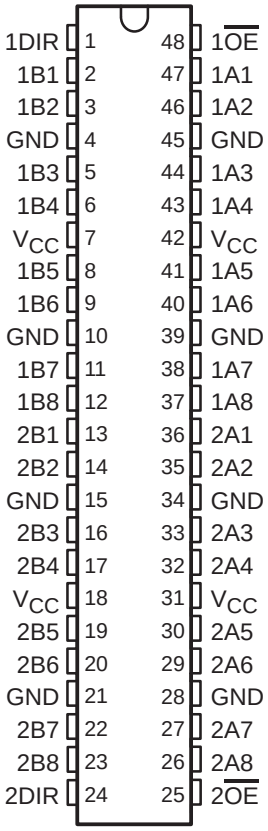
- **Members of the Texas Instruments *Widebus*™ Family**
- **A-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-833, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and Shrink Small-Outline (DL) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABTH162245 . . . WD PACKAGE
SN74ABTH162245 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The ’ABTH162245 devices are 16-bit noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

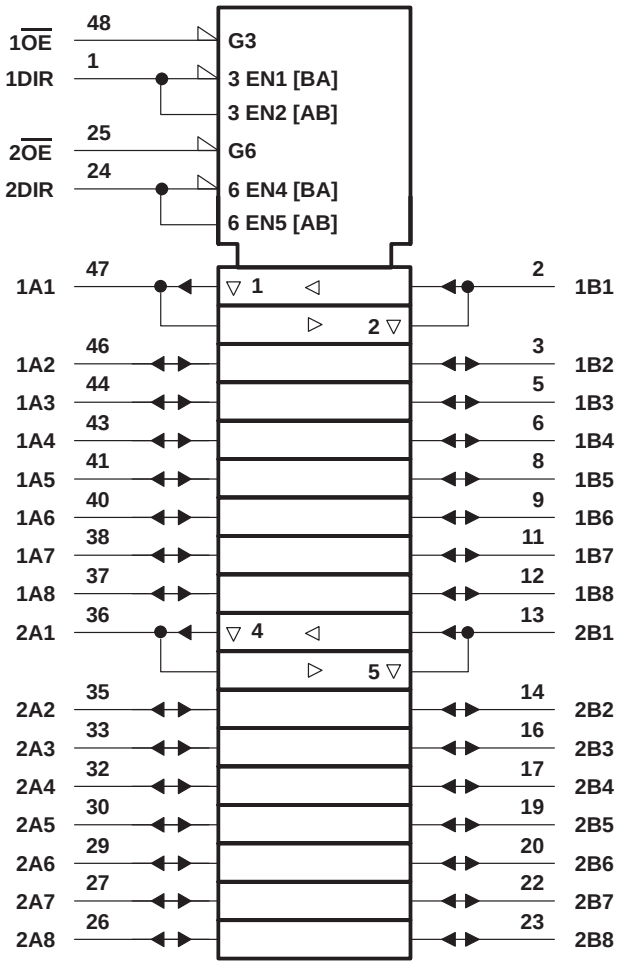
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABTH162245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABTH162245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

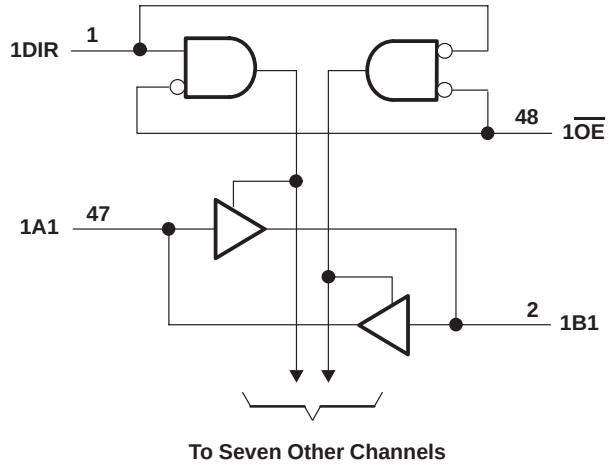
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

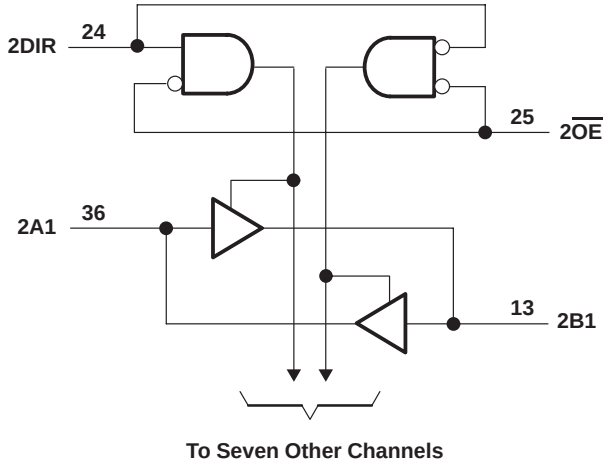
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABTH162245 (B port) . . . . . 96 mA
SN74ABTH162245 (B port) . . . . . 128 mA
SN54/74ABTH162245 (A port) . . . . . 30 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –18 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . . 89°C/W
DGV package . . . . . 93°C/W
DL package . . . . . 94°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			SN54ABTH162245		SN74ABTH162245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	B port		–24		–32	mA
		A port		–12		–12	
I_{OL}	Low-level output current	B port		48		64	mA
		A port		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

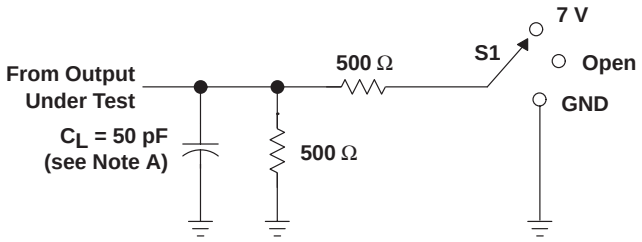
PARAMETER		TEST CONDITIONS		SN54ABTH162245			SN74ABTH162245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	A port	V_{CC} = 5 V,	I_{OH} = –1 mA	2.5			2.5			V
		V_{CC} = 4.5 V	I_{OH} = –1 mA	3			3			
			I_{OH} = –3 mA	3			3.1			
			I_{OH} = –12 mA				2.6			
	B port	V_{CC} = 5 V,	I_{OH} = –3 mA	3			3			
		V_{CC} = 4.5 V	I_{OH} = –3 mA	2.5			2.5			
			I_{OH} = –24 mA	2						
			I_{OH} = –32 mA				2			
V_{OL}	A port	V_{CC} = 4.5 V	I_{OL} = 12 mA			0.8			0.8	V
	B port		I_{OL} = 48 mA			0.45			0.45	
			I_{OL} = 64 mA						0.55	
V_{hys}					100			100		mV
I_I	Control inputs	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1			±1	µA
	A or B ports					±20			±20	
$I_{I(hold)}$		V_{CC} = 4.5 V	V_I = 0.8 V	100			100			µA
			V_I = 2 V	–100			–100			
I_{off}		V_{CC} = 0, V_I or V_O = 0 to 4.5 V							±100	µA
I_O‡	A port	V_{CC} = 5.5 V,	V_O = 2.5 V	–25		–90	–25		–100	mA
	B port			–50		–180	–50		–180	
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50			50	µA
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			2			2	mA
			Outputs low			32			32	
			Outputs disabled			2			2	
ΔI_{CC}§	Data inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				2			2	mA
	Control inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5			1.5	
C_i		V_I = 2.5 V or 0.5 V			3			3		pF
C_{io}		V_O = 2.5 V or 0.5 V			6			6		pF

† All typical values are at V_{CC} = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

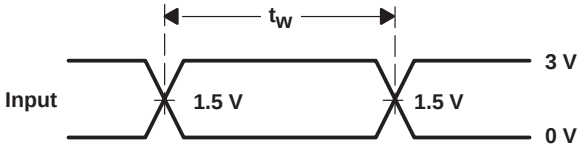
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABTH162245		SN74ABTH162245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	2.2	3.4	1	4.1	1	3.9	ns
t_{PHL}			1	2.3	3.7	1	4.4	1	4.2	
t_{PLH}	B	A	1	2.7	4.1	1	4.9	1	4.6	ns
t_{PHL}			1.5	3.1	4.6	1.5	5.2	1.5	5.1	
t_{PZH}	$\overline{OE}$	B	1	3.6	5.2	1	6.4	1	6.3	ns
t_{PZL}			1	3.7	5.4	1	6.5	1	6.4	
t_{PHZ}	$\overline{OE}$	B	2	4.4	5.8	2	6.4	2	6.3	ns
t_{PLZ}			1.5	3.3	4.7	1.5	5.6	1.5	5.2	
t_{PZH}	$\overline{OE}$	A	1.5	4.1	6	1.5	7.2	1.5	7.1	ns
t_{PZL}			1.5	4.3	6.1	1.5	7.3	1.5	7	
t_{PHZ}	$\overline{OE}$	A	2	4.5	6.1	2	6.8	2	6.6	ns
t_{PLZ}			1.5	3.7	5.1	1.5	6.1	1.5	5.7	

PARAMETER MEASUREMENT INFORMATION

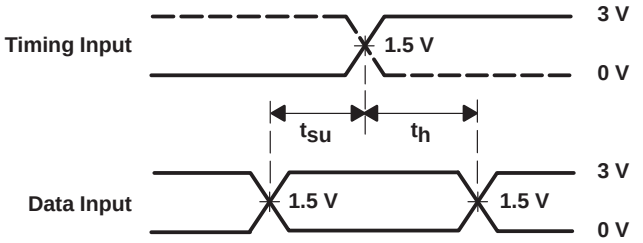


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

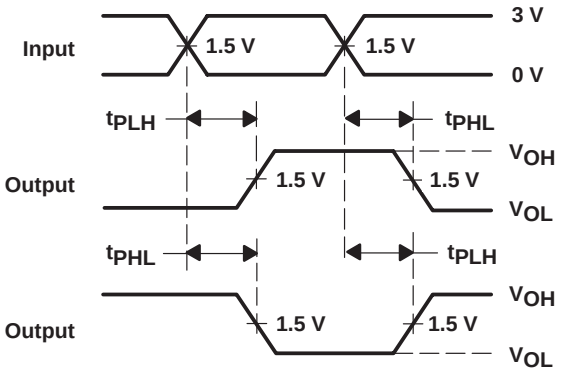
LOAD CIRCUIT



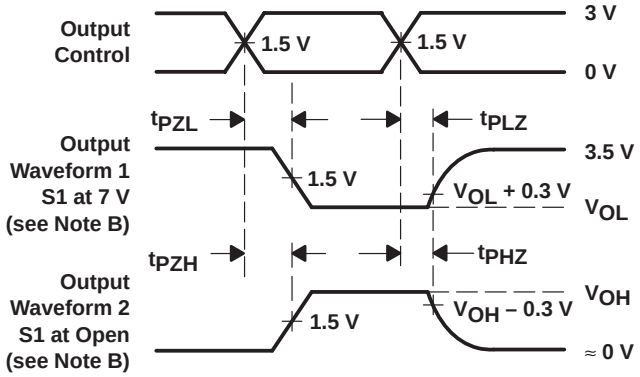
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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