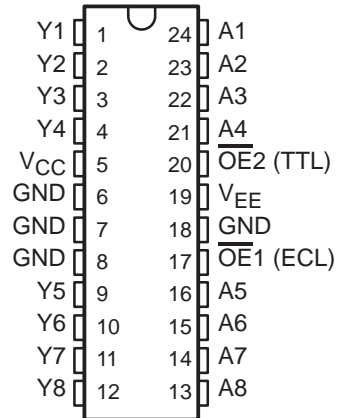


SN10KHT5539 OCTAL ECL-TO-TTL TRANSLATOR WITH OPEN-COLLECTOR OUTPUTS

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- 10KH Compatible
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- ECL and TTL Output-Enable Inputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} , V_{EE} , and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include “Small Outline” Packages and Standard Plastic 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters while eliminating the need for 3-state overlap protection.

Two pins $\overline{OE1}$ and $\overline{OE2}$ are provided for output-enable control. These control inputs are ANDed together with $\overline{OE1}$ being ECL-compatible and $\overline{OE2}$ being TTL-compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN10KHT5539 is characterized for operation from 0°C to 75°C.

FUNCTION TABLE

OUTPUT ENABLE		DATA INPUT	OUTPUT (TTL)
OE1	OE2	A	Y
X	H	X	H
H	X	X	H
L	L	L	L
L	L	H	H

recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	TTL supply voltage	4.5	5	5.5	V
V _{EE}	ECL supply voltage	-4.94	-5.2	-5.46	V
V _{IH}	TTL high-level input voltage	2			V
V _{IL}	TTL low-level input voltage			0.8	V
V _{IH}	ECL high-level input voltage†	T _A = 0°C	-1170	-840	mV
		T _A = 25°C	-1130	-810	
		T _A = 75°C	-1070	-735	
V _{IL}	ECL low-level input voltage†	T _A = 0°C	-1950	-1480	mV
		T _A = 25°C	-1950	-1480	
		T _A = 75°C	-1950	-1450	
V _{OH}	TTL high-level output voltage			5.5	V
I _{IK}	TTL input clamp current			-18	mA
I _{OL}	Low-level output current			48	mA
T _A	Operating free-air temperature range	0		75	°C

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V _{IK}	OE2 only	V _{CC} = 4.5 V,	V _{EE} = -4.94 V,	I _I = -18 mA			-1.2	V
I _{OH}		V _{CC} = 4.5 V,	V _{EE} = -4.94 V,	V _{OH} = 5.5 V			250	μA
V _{OL}		V _{CC} = 4.5 V,	V _{EE} = -5.2 V ± 5%,	I _{OL} = 48 mA		0.38	0.55	V
I _I	OE2 only	V _{CC} = 5.5 V,	V _{EE} = -5.46 V,	V _I = 7 V			0.1	mA
I _{IH}	OE2 only	V _{CC} = 5.5 V,	V _{EE} = -5.46 V,	V _I = 2.7 V			20	μA
I _{IL}	OE2 only	V _{CC} = 5.5 V,	V _{EE} = -5.46 V,	V _I = 0.5 V			-0.5	mA
I _{IH}	A inputs and $\overline{OE}1$	V _{CC} = 5.5 V,	V _{EE} = -5.46 V,	V _I = -840 mV	T _A = 0°C		350	μA
		V _{CC} = 5.5 V,	V _{EE} = -5.46 V,	V _I = -810 mV	T _A = 25°C		350	
		V _{CC} = 5.5 V,	V _{EE} = -5.46 V,	V _I = -735 mV	T _A = 75°C		350	
I _{IL}	A inputs and $\overline{OE}1$	V _{CC} = 5.5 V,	V _{EE} = -5.46 V,	V _I = -1950 mV	T _A = 0°C	0.5		μA
					T _A = 25°C	0.5		
					T _A = 75°C	0.5		
I _{CCH}		V _{CC} = 5.5 V,	V _{EE} = -5.46 V			63	91	mA
I _{CCL}		V _{CC} = 5.5 V,	V _{EE} = -5.46 V			79	114	mA
I _{EE}		V _{CC} = 5.5 V,	V _{EE} = -5.46 V			-22	-32	mA
C _i		V _{CC} = 5 V,	V _{EE} = -5.2 V			6		pF
C _o		V _{CC} = 5 V,	V _{EE} = -5.2 V			5		pF

‡ All typical values are at V_{CC} = 5 V, V_{EE} = -5.2 V, T_A = 25°C.

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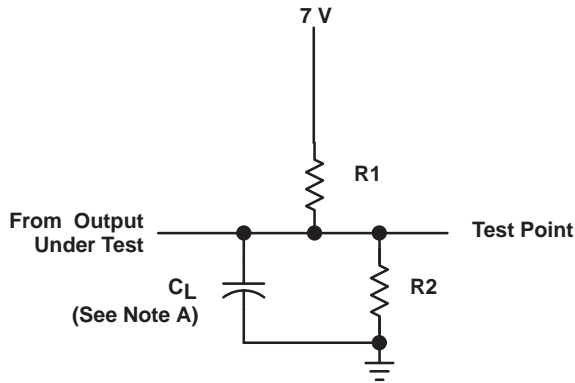
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switching characteristics over recommended ranges of operating supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)

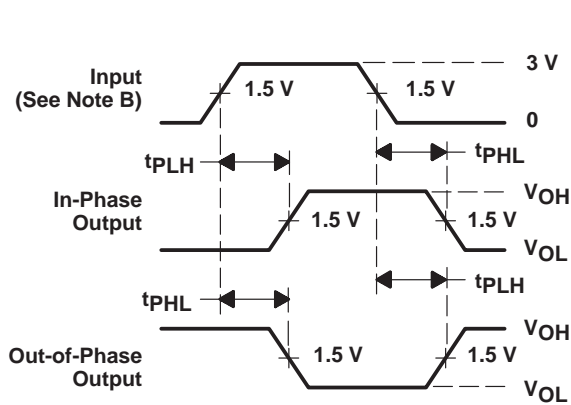
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
t _{PLH}	Any A	Y	6.2	9.3	12.4	ns
t _{PHL}			2.6	4.9	7.3	
t _{PLH}	$\overline{OE}1$ (ECL)	Y	7.1	10.3	13.5	ns
t _{PHL}			3.2	5.8	8.4	
t _{PLH}	$\overline{OE}2$ (TTL)	Y	6.5	9.5	12.4	ns
t _{PHL}			2.7	5.3	8	

† All typical values are at V_{CC} = 5 V, V_{EE} = -5.2 V, T_A = 25°C.

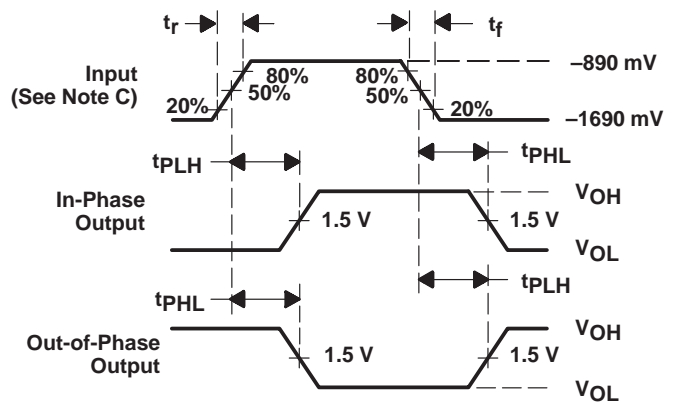
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



TTL-INPUT PROPAGATION DELAY TIMES



ECL-INPUT PROPAGATION DELAY TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq 1.5$ ns, $t_f \leq 1.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. load circuit and voltage waveforms

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