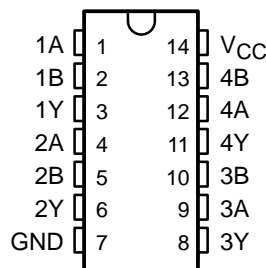


CD54AC00, CD74AC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

SCHS303C – JANUARY 2001 – REVISED JUNE 2002

- AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ±24-mA Output Drive Current
– Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

CD54AC00 . . . F PACKAGE
CD74AC00 . . . E OR M PACKAGE
(TOP VIEW)



description

The 'AC00 devices contain four independent 2-input NAND gates. Each gate performs the Boolean function of $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	PDIP – E	Tube	CD74AC00E	CD74AC00E
	SOIC – M	Tube	CD74AC00M	AC00M
		Tape and reel	CD74AC00M96	
	CDIP – F	Tube	CD54AC00F3A	CD54AC00F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic diagram, each gate (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
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CD54AC00, CD74AC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2): E package	80°C/W
M package	86°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		$T_A = 25^\circ\text{C}$		$-40^\circ\text{C TO } 85^\circ\text{C}$		$-55^\circ\text{C TO } 125^\circ\text{C}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	1.5	5.5	1.5	5.5	1.5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 1.5\text{ V}$		1.2		1.2		V
		$V_{CC} = 3\text{ V}$		2.1		2.1		
		$V_{CC} = 4.5\text{ V}$		3.15		3.15		
		$V_{CC} = 5.5\text{ V}$		3.85		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 1.5\text{ V}$		0.3		0.3		V
		$V_{CC} = 3\text{ V}$		0.9		0.9		
		$V_{CC} = 4.5\text{ V}$		1.35		1.35		
		$V_{CC} = 5.5\text{ V}$		1.65		1.65		
V_I	Input voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$	-24		-24		mA
I_{OL}	Low-level output current		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$	24		24		mA
$\Delta t/\Delta v$	Input transition rise or fall rate		$V_{CC} = 1.5\text{ V to } 3\text{ V}$	50		50		ns/V
			$V_{CC} = 3.6\text{ V to } 5.5\text{ V}$	20		20		

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



CD54AC00, CD74AC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C		-40°C TO 85°C		-55°C TO 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -50 μA	1.5 V	1.4	1.4	1.4			V	
			3 V	2.9	2.9	2.9				
			4.5 V	4.4	4.4	4.4				
		I _{OH} = -4 mA	3 V	2.58	2.48	2.4				
		I _{OH} = -24 mA	4.5 V	3.94	3.8	3.7				
		I _{OH} = -50 mA†	5.5 V			3.85				
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 50 μA	1.5 V	0.1	0.1	0.1		V		
			3 V	0.1	0.1	0.1				
			4.5 V	0.1	0.1	0.1				
		I _{OL} = 12 mA	3 V	0.36	0.44	0.5				
		I _{OL} = 24 mA	4.5 V	0.36	0.44	0.5				
		I _{OL} = 50 mA†	5.5 V			1.65				
I _I	V _I = V _{CC} or GND	5.5 V		±0.1	±1	±1	μA			
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		4	40	80	μA			
C _i				10	10	10	pF			

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 1.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-40°C TO 85°C		-55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y		83		91	ns
t _{PHL}			83	91			

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-40°C TO 85°C		-55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	2.7	9.3	2.6	10.2	ns
t _{PHL}			2.7	9.3	2.6	10.2	



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QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-40°C TO 85°C		-55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	1.9	6.6	1.8	7.3	ns
t _{PHL}			1.9	6.6	1.8	7.3	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TYP	UNIT
C _{pd} Power dissipation capacitance	45	pF



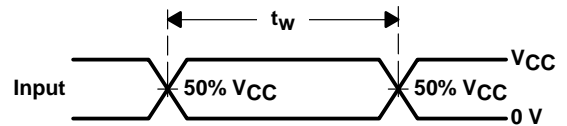
PARAMETER MEASUREMENT INFORMATION



† When $V_{CC} = 1.5\text{ V}$, $R_1 = R_2 = 1\text{ k}\Omega$

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



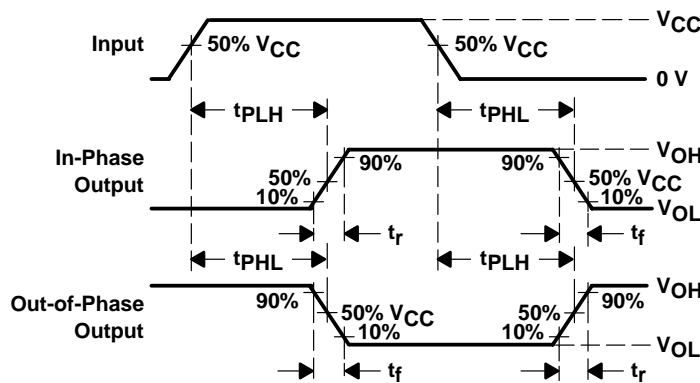
VOLTAGE WAVEFORMS
 PULSE DURATION



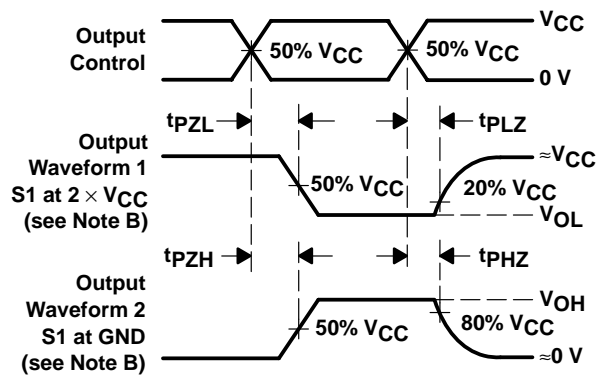
VOLTAGE WAVEFORMS
 RECOVERY TIME



VOLTAGE WAVEFORMS
 SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
 OUTPUT ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$. Phase relationships between waveforms are arbitrary.
 D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 E. The outputs are measured one at a time with one input transition per measurement.
 F. t_{PLH} and t_{PHL} are the same as t_{pd} .
 G. t_{PZL} and t_{PZH} are the same as t_{en} .
 H. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

Figure 1. Load Circuit and Voltage Waveforms

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