



14-Bit, 125MSPS Analog-to-Digital Converter

FEATURES

- 14-Bit Resolution
- 125MSPS Sample Rate
- High SNR: 70.5dBFS at 100MHz f_{IN}
- High SFDR: 82dBc at 100MHz f_{IN}
- 2.3V_{PP} Differential Input Voltage
- Internal Voltage Reference
- 3.3V Single-Supply Voltage
- Analog Power Dissipation: 578mW
– Total Power Dissipation: 780mW
- Serial Programming Interface
- TQFP-64 PowerPAD™ Package

- Recommended Amplifiers:
OPA695, OPA847, THS3201, THS3202,
THS4503, THS9001

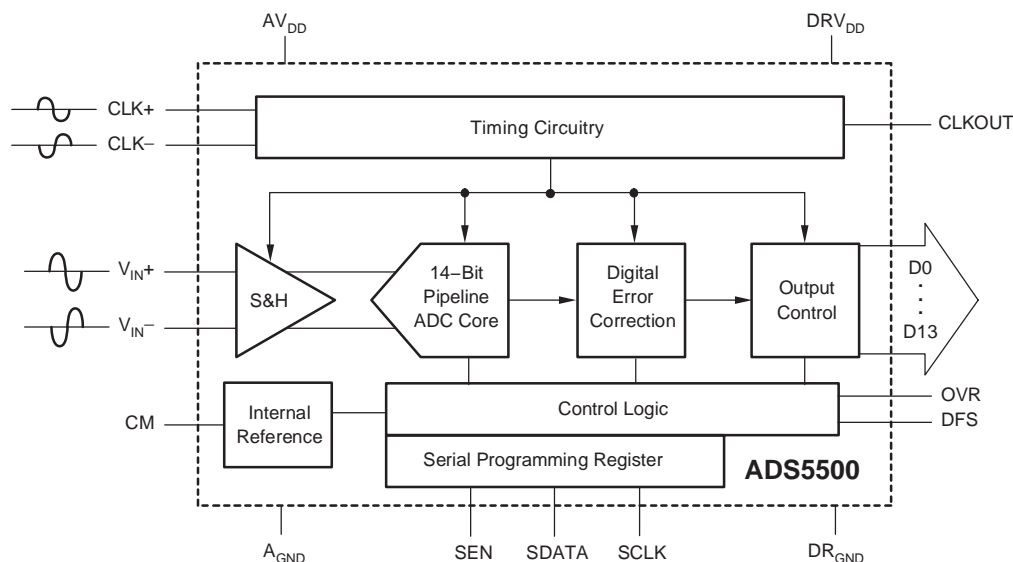
APPLICATIONS

- Wireless Communication
 - Communication Receivers
 - Base Station Infrastructure
- Test and Measurement Instrumentation
- Single and Multichannel Digital Receivers
- Communication Instrumentation
 - Radar, Infrared
- Video and Imaging
- Medical Equipment

DESCRIPTION

The ADS5500 is a high-performance, 14-bit, 125MSPS analog-to-digital converter (ADC). To provide a complete converter solution, it includes a high-bandwidth linear sample-and-hold stage (S&H) and internal reference. Designed for applications demanding the highest speed and highest dynamic performance in very little space, the ADS5500 has excellent power consumption of 780mW at 3.3V single-supply voltage. This allows an even higher system integration density. The provided internal reference simplifies system design requirements. Parallel CMOS-compatible output ensures seamless interfacing with common logic.

The ADS5500 is available in a 64-pin TQFP PowerPAD package and is specified over the full temperature range of -40°C to +85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5500	HTQFP-64(2) PowerPAD	PAP	-40°C to +85°C	ADS5500I	ADS5500IPAP	Tray, 160
					ADS5500IPAPR	Tape and Reel, 1000

(1) For the most current product and ordering information, see the Package Option Addendum located at the end of this data sheet.

(2) Thermal pad size: 3.5mm x 3.5mm (min), 4mm x 4mm (max).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		ADS5500	UNIT
Supply Voltage	AVDD to AGND, DRVDD to DRGND	-0.3 to +3.7	V
	AGND to DRGND	±0.1	V
Analog input to AGND		-0.15 to +2.5	V
Logic input to DRGND		-0.3 to DRVDD + 0.3	V
Digital data output to DRGND		-0.3 to DRVDD + 0.3	V
Input current (any input)		30	mA
Operating temperature range		-40 to +85	°C
Junction temperature		+105	°C
Storage temperature range		-65 to +150	°C

(1) Stresses above these ratings may cause permanent damage.

Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
Supplies				
Analog supply voltage, AVDD	3.0	3.3	3.6	V
Output driver supply voltage, DRVDD	3.0	3.3	3.6	V
Analog Input				
Differential input range	2.3			Vpp
Input common-mode voltage, VCM(1)	1.5		1.6	V
Digital Output				
Maximum output load	10			pF
Clock Input				
ADCLK input sample rate (sine wave) 1/tC	DLL ON	60	125	MSPS
	DLL OFF	10	80	MSPS
Clock amplitude, sine wave, differential(2)	3			Vpp
Clock duty cycle(3)	50			%
Open free-air temperature range	-40		+85	°C

(1) Input common-mode should be connected to CM.

(2) See Figure 13 for more information.

(3) See Figure 12 for more information.

ELECTRICAL CHARACTERISTICS

Typ, min, and max values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $t_{\text{MAX}} = +85^\circ\text{C}$, sampling rate = 125MSPS, 50% clock duty cycle, $AV_{\text{DD}} = DRV_{\text{DD}} = 3.3\text{V}$, DLL On, -1dBFS differential input, and $3V_{\text{PP}}$ differential clock, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT	
Resolution				14 Tested		Bits	
Analog Inputs							
Differential input range				2.3		V_{PP}	
Differential input impedance	See Figure 4			6.6		$k\Omega$	
Differential input capacitance	See Figure 4			4		pF	
Total analog input common-mode current				4(1)		mA	
Analog input bandwidth	Source impedance = 50Ω			750		MHz	
Conversion Characteristics							
Maximum sample rate			see note (2)		125	MSPS	
Data latency	See timing diagram, Figure 1			16.5		Clock Cycles	
Internal Reference Voltages							
Reference bottom voltage, V_{REFM}				0.97		V	
Reference top voltage, V_{REFP}				2.11		V	
Reference error			-4	± 0.9	+4	%	
Common-mode voltage output, V_{CM}				1.55 ± 0.05		V	
Dynamic DC Characteristics and Accuracy							
No missing codes				Tested			
Differential linearity error, DNL	$f_{\text{IN}} = 10\text{MHz}$		-0.9	± 0.75	+1.1	LSB	
Integral linearity error, INL	$f_{\text{IN}} = 10\text{MHz}$		-5	± 2.5	+5	LSB	
Offset error				± 1.5		mV	
Offset temperature coefficient				0.0007		$\% / ^\circ\text{C}$	
Gain error				± 0.45		%FS	
Gain temperature coefficient				0.01		$\Delta\% / ^\circ\text{C}$	
Dynamic AC Characteristics							
Signal-to-noise ratio, SNR	$f_{\text{IN}} = 10\text{MHz}$	Room temp	70.5	71.5		dBFS	
		Full temp range	69	71.5		dBFS	
	$f_{\text{IN}} = 30\text{MHz}$				71.5		dBFS
	$f_{\text{IN}} = 55\text{MHz}$				71.5		dBFS
	$f_{\text{IN}} = 70\text{MHz}$	Room temp	70	71.2		dBFS	
		Full temp range	68.5	71		dBFS	
	$f_{\text{IN}} = 100\text{MHz}$				70.5		dBFS
	$f_{\text{IN}} = 150\text{MHz}$				70.1		dBFS
$f_{\text{IN}} = 225\text{MHz}$				69.1		dBFS	
RMS Output noise	Input tied to common-mode			1.1		LSB	
Spurious-free dynamic range, SFDR	$f_{\text{IN}} = 10\text{MHz}$	Room temp	82	84		dBc	
		Full temp range	78	84		dBc	
	$f_{\text{IN}} = 30\text{MHz}$				84		dBc
	$f_{\text{IN}} = 55\text{MHz}$				79		dBc
	$f_{\text{IN}} = 70\text{MHz}$	Room temp	80	83		dBc	
		Full temp range	77	82		dBc	
	$f_{\text{IN}} = 100\text{MHz}$				82		dBc
	$f_{\text{IN}} = 150\text{MHz}$				78		dBc
$f_{\text{IN}} = 225\text{MHz}$				74		dBc	

(1) 2mA per input.

(2) See Recommended Operating Conditions on page 2.

ELECTRICAL CHARACTERISTICS (continued)

Typ, min, and max values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $t_{\text{MAX}} = +85^\circ\text{C}$, sampling rate = 125MSPS, 50% clock duty cycle, $AV_{\text{DD}} = DRV_{\text{DD}} = 3.3\text{V}$, DLL On, -1dBFS differential input, and 3Vpp differential clock, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Second-harmonic, HD2	$f_{\text{IN}} = 10\text{MHz}$	Room temp	82	91		dBc
		Full temp range	78	86		dBc
	$f_{\text{IN}} = 30\text{MHz}$			86		dBc
	$f_{\text{IN}} = 55\text{MHz}$			84		dBc
	$f_{\text{IN}} = 70\text{MHz}$	Room temp	80	87		dBc
		Full temp range	77	83		dBc
	$f_{\text{IN}} = 100\text{MHz}$			84		dBc
	$f_{\text{IN}} = 150\text{MHz}$			78		dBc
$f_{\text{IN}} = 225\text{MHz}$			74		dBc	
Third-harmonic, HD3	$f_{\text{IN}} = 10\text{MHz}$	Room temp	82	89		dBc
		Full temp range	78	88		dBc
	$f_{\text{IN}} = 30\text{MHz}$			90		dBc
	$f_{\text{IN}} = 55\text{MHz}$			79		dBc
	$f_{\text{IN}} = 70\text{MHz}$	Room temp	80	85		dBc
		Full temp range	77	82		dBc
	$f_{\text{IN}} = 100\text{MHz}$			82		dBc
	$f_{\text{IN}} = 150\text{MHz}$			80		dBc
$f_{\text{IN}} = 225\text{MHz}$			76		dBc	
Worst-harmonic/spur (other than HD2 and HD3)	$f_{\text{IN}} = 10\text{MHz}$	Room temp		88		dBc
	$f_{\text{IN}} = 70\text{MHz}$	Room temp		86		dBc
Signal-to-noise + distortion, SINAD	$f_{\text{IN}} = 10\text{MHz}$	Room temp	69	70		dBc
		Full temp range	67.5	70		dBc
	$f_{\text{IN}} = 30\text{MHz}$			70		dBc
	$f_{\text{IN}} = 55\text{MHz}$			69.5		dBc
	$f_{\text{IN}} = 70\text{MHz}$	Room temp	68.5	69		dBc
		Full temp range	67	69.5		dBc
	$f_{\text{IN}} = 100\text{MHz}$			69		dBc
	$f_{\text{IN}} = 150\text{MHz}$			69		dBc
$f_{\text{IN}} = 225\text{MHz}$			66.4		dBc	
Total harmonic distortion, THD	$f_{\text{IN}} = 10\text{MHz}$	Room temp	80	85		dBc
		Full temp range	78	83		dBc
	$f_{\text{IN}} = 30\text{MHz}$			82		dBc
	$f_{\text{IN}} = 55\text{MHz}$			77		dBc
	$f_{\text{IN}} = 70\text{MHz}$	Room temp	77.5	81		dBc
		Full temp range	76	79.5		dBc
	$f_{\text{IN}} = 100\text{MHz}$			79		dBc
	$f_{\text{IN}} = 150\text{MHz}$			75		dBc
$f_{\text{IN}} = 225\text{MHz}$			71.8		dBc	

ELECTRICAL CHARACTERISTICS (continued)

Typ, min, and max values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $t_{\text{MAX}} = +85^\circ\text{C}$, sampling rate = 125MSPS, 50% clock duty cycle, $AV_{\text{DD}} = DRV_{\text{DD}} = 3.3\text{V}$, DLL On, -1dBFS differential input, and 3V_{pp} differential clock, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Effective number of bits, ENOB	$f_{\text{IN}} = 70\text{MHz}$		11.3		Bits
Two-tone intermodulation distortion, IMD	$f = 10.1\text{MHz}, 15.1\text{MHz}$ (-7dBFS each tone)		85		dBc
	$f = 30.1\text{MHz}, 35.1\text{MHz}$ (-7dBFS each tone)		85		dBc
	$f = 50.1\text{MHz}, 55.1\text{MHz}$ (-7dBFS each tone)		88		dBc
Power Supply					
Total supply current, I_{CC}	$V_{\text{IN}} = \text{full-scale}, f_{\text{IN}} = 55\text{MHz}$ $AV_{\text{DD}} = DRV_{\text{DD}} = 3.3\text{V}$		236	265	mA
Analog supply current, I_{AVDD}	$V_{\text{IN}} = \text{full-scale}, f_{\text{IN}} = 55\text{MHz}$ $AV_{\text{DD}} = DRV_{\text{DD}} = 3.3\text{V}$		175	190	mA
Output buffer supply current, I_{DRVDD}	$V_{\text{IN}} = \text{full-scale}, f_{\text{IN}} = 55\text{MHz}$ $AV_{\text{DD}} = DRV_{\text{DD}} = 3.3\text{V}$		61	75	mA
Power dissipation	Analog only		578	627	mW
	Total power with 10pF load on digital output to ground		780	875	mW
Standby power	With clocks running		181	250	mW

DIGITAL CHARACTERISTICS

Typ, min, and max values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $t_{\text{MAX}} = +85^\circ\text{C}$, sampling rate = 125MSPS, 50% clock duty cycle, $AV_{\text{DD}} = DRV_{\text{DD}} = 3.3\text{V}$, DLL On, -1dBFS differential input, and 3V_{pp} differential clock, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs					
High-level input voltage		2.4			V
Low-level input voltage				0.8	V
High-level input current				10	μA
Low-level input current				10	μA
Input current for RESET			-20		μA
Input capacitance			4		pF
Digital Outputs⁽¹⁾					
Low-level output voltage	$C_{\text{LOAD}} = 10\text{pF}^{(2)}, f_{\text{S}} = 125\text{MSPS}$		0.3		V
High-level output voltage	$C_{\text{LOAD}} = 10\text{pF}^{(2)}, f_{\text{S}} = 125\text{MSPS}$		3.0		V
Output capacitance			3		pF

(1) For optimal performance, all digital output lines (D0:D13), including the output clock, should see a similar load.

(2) Equivalent capacitance to ground of (load + parasitics of transmission lines).

TIMING CHARACTERISTICS

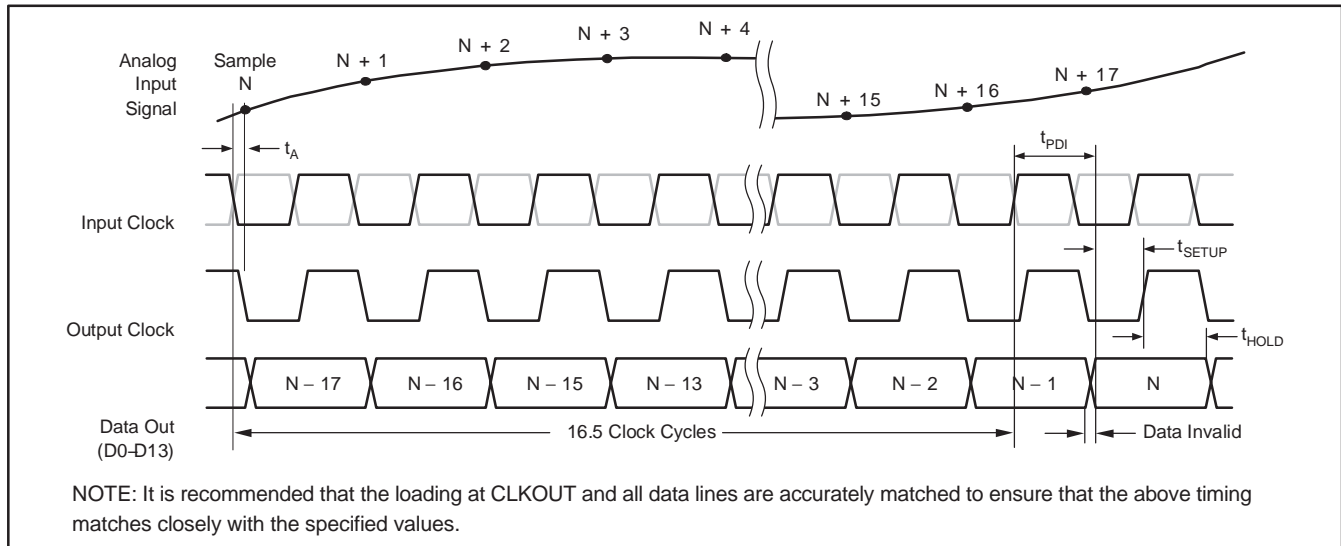


Figure 1. Timing Diagram

TIMING CHARACTERISTICS

Typ, min, and max values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $t_{\text{MAX}} = +85^\circ\text{C}$, sampling rate = 125MSPS, 50% clock duty cycle, $AV_{\text{DD}} = DRV_{\text{DD}} = 3.3\text{V}$, DLL On, -1dBFS differential input, and 3Vpp differential clock, unless otherwise noted.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Switching Specification					
Aperture delay, t_A	Input CLK falling edge to data sampling point		1		ns
Aperture jitter (uncertainty)	Uncertainty in sampling instant		300		fs
Data setup time, t_{SETUP}	Data valid to 50% of CLKOUT rising edge		2		ns
Data hold time, t_{HOLD}	CLKOUT rising edge to data becoming invalid		1.7		ns
Data latency, $t_{\text{D(Pipe)}}$	Input clock falling edge (on which sampling takes place) to input clock rising edge (on which the corresponding data is given out)		16.5		Clock Cycles
Propagation delay, t_{PDI}	Input clock rising edge to data valid		7.5		ns
Data rise time	Data out 20% to 80%		2.5		ns
Data fall time	Data out 80% to 20%		2.5		ns
Output enable (OE) to output stable delay			2		ms

SERIAL PROGRAMMING INTERFACE CHARACTERISTICS

The device has a three-wire serial interface. The device latches the serial data SDATA on the falling edge of serial clock SCLK when SEN is active.

- Serial shift of bits is enabled when SEN is low. SCLK shifts serial data at falling edge.
- Minimum width of data stream for a valid loading is 16 clocks.

- Data is loaded at every 16th SCLK falling edge while SEN is low.
- In case the word length exceeds a multiple of 16 bits, the excess bits are ignored.
- Data can be loaded in multiple of 16-bit words within a single active SEN pulse.

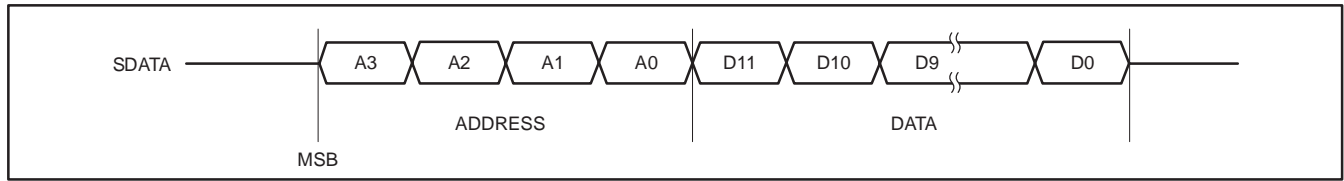


Figure 2. DATA Communication is 2-Byte, MSB First

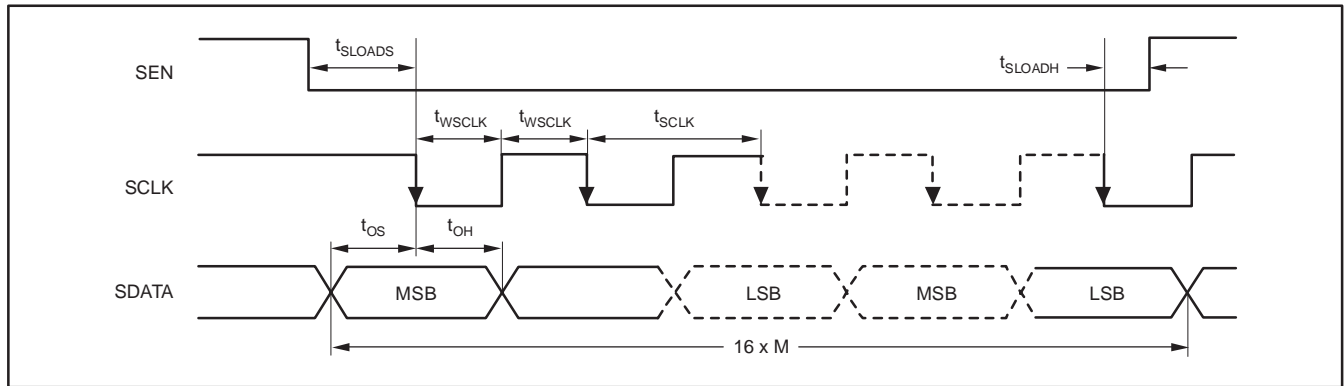


Figure 3. Serial Programming Interface Timing Diagram

Table 1. Serial Programming Interface Timing Characteristics

SYMBOL	PARAMETER	MIN(1)	TYP(1)	MAX(1)	UNIT
tSCLK	SCLK Period	50			ns
tWSCLK	SCLK Duty Cycle	25	50	75	%
tSLOADS	SEN to SCLK setup time	8			ns
tSLOADH	SCLK to SEN hold time	6			ns
tDS	Data Setup Time	8			ns
tDH	Data Hold Time	6			ns

(1) Min, typ, and max values are characterized, but not production tested.

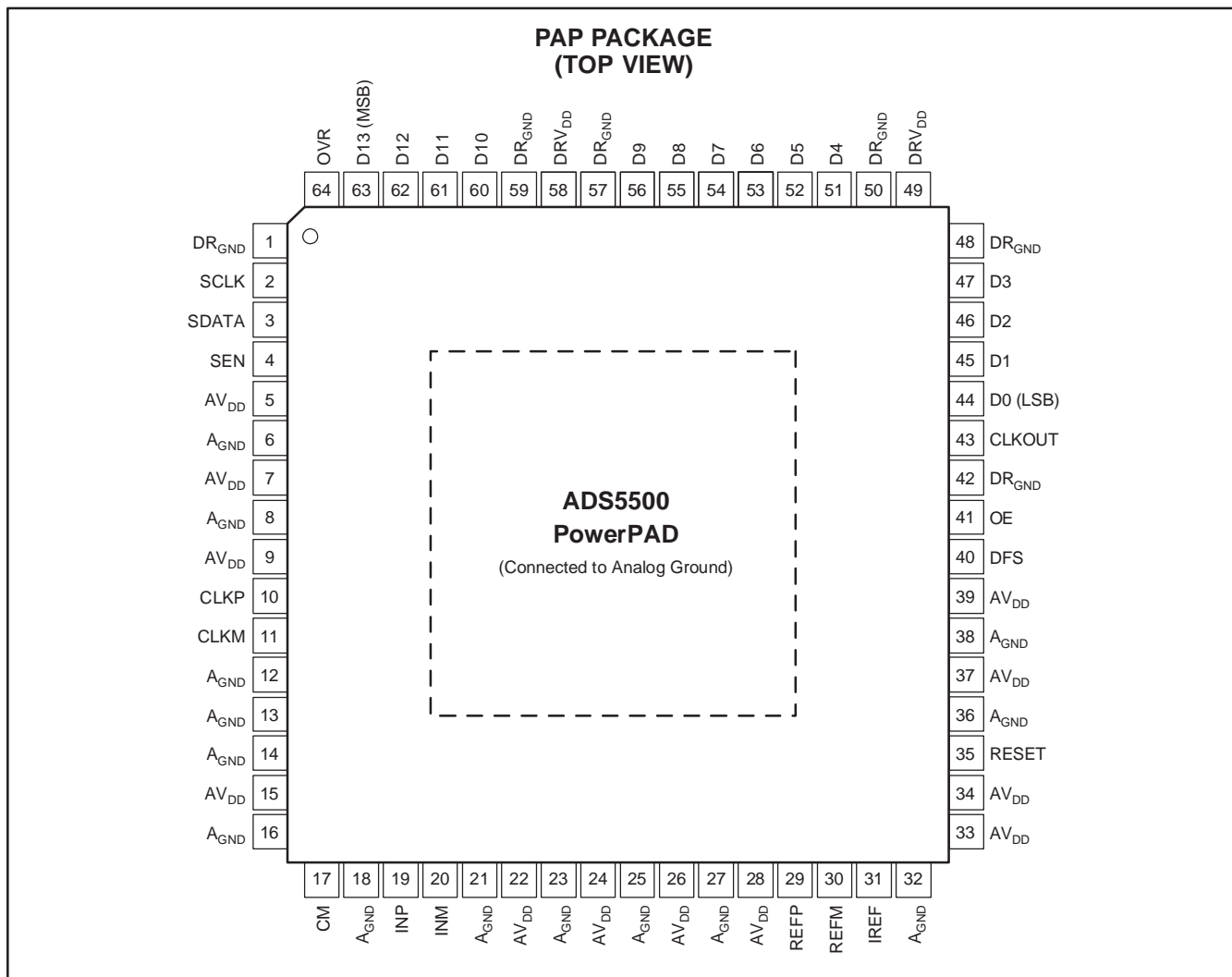
Table 2. Serial Register Table

A3	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	1	0	1	0	0	0	0	0	0	0	0	0	0	DLL OFF	0	DLL OFF = 0 : internal DLL is on, recommended for 60–125MSPS clock speed DLL OFF = 1 : internal DLL is off, recommended for 10–80MSPS clock speed
1	1	1	0	0	TP<1>	TP<0>	0	0	0	0	0	0	0	0	0	TP<1:0> – Test modes for output data capture TP<1> = 0, TP<0> = 0 : Normal mode of operation, TP<1> = 0 TP<0> = 1 : All output lines are pulled to '0', TP<1> = 1 TP<0> = 0 : All output lines are pulled to '1', TP<1> = 1 TP<0> = 1 : A continuous stream of '10' comes out on all output lines
1	1	1	1	PDN	0	0	0	0	0	0	0	0	0	0	0	PDN = 0 : Normal mode of operation, PDN = 1 : Device is put in power down (low current) mode

Table 3. DATA FORMAT SELECT (DFS TABLE)

DFS-PIN VOLTAGE (V_{DFS})	DATA FORMAT	CLOCK OUTPUT POLARITY
$V_{DFS} < \frac{1}{6} \times AV_{DD}$	Straight Binary	Data valid on rising edge
$\frac{5}{12} \times AV_{DD} > V_{DFS} > \frac{1}{3} \times AV_{DD}$	Two's Complement	Data valid on rising edge
$\frac{2}{3} \times AV_{DD} > V_{DFS} > \frac{7}{12} \times AV_{DD}$	Straight Binary	Data valid on falling edge
$V_{DFS} > \frac{5}{6} \times AV_{DD}$	Two's Complement	Data valid on falling edge

PIN CONFIGURATION



PIN ASSIGNMENTS

NAME	TERMINAL NO.	NO. OF PINS	I/O	DESCRIPTION
AV _{DD}	5, 7, 9, 15, 22, 24, 26, 28, 33, 34, 37, 39	12	I	Analog power supply
AGND	6, 8, 12, 13, 14, 16, 18, 21, 23, 25, 27, 32, 36, 38	14	I	Analog ground
DRV _{DD}	49, 58	2	I	Output driver power supply
DRGND	1, 42, 48, 50, 57, 59	6	I	Output driver ground
INP	19	1	I	Differential analog input (positive)
INM	20	1	I	Differential analog input (negative)
REFP	29	1	O	Reference voltage (positive); 0.1μF capacitor in series with a 1Ω resistor to GND
REFM	30	1	O	Reference voltage (negative); 0.1μF capacitor in series with a 1Ω resistor to GND
IREF	31	1	I	Current set; 56kΩ resistor to GND; do not connect capacitors
CM	17	1	O	Common-mode output voltage
RESET	35	1	I	Reset (active high), 200kΩ resistor to AV _{DD}
OE	41	1	I	Output enable (active high)
DFS	40	1	I	Data format and clock out polarity select ⁽¹⁾
CLKP	10	1	I	Data converter differential input clock (positive)
CLKM	11	1	I	Data converter differential input clock (negative)
SEN	4	1	I	Serial interface chip select
SDATA	3	1	I	Serial interface data
SCLK	2	1	I	Serial interface clock
D0 (LSB)–D13 (MSB)	44–47, 51–56, 60–63	14	O	Parallel data output
OVR	64	1	O	Over-range indicator bit
CLKOUT	43	1	O	CMOS clock out in sync with data

NOTE: PowerPAD is connected to analog ground.

(1) The DFS pin is programmable to four discrete voltage levels: 0, 3/8 AV_{DD}, 5/8 AV_{DD}, and AV_{DD}. The thresholds are centered. More details are listed in Table 3 on page 8.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3dB.

Aperture Delay

The delay in time between the falling edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle

A perfect differential sine wave clock results in a 50% clock duty cycle on the internal conversion clock. Pulse width high is the minimum amount of time that the ENCODE pulse should be left in logic '1' state to achieve rated performance. Pulse width low is the minimum time that the ENCODE pulse should be left in a low state (logic '0'). At a given clock rate, these specifications define an acceptable clock duty cycle.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation of any single LSB transition at the digital output from an ideal 1 LSB step at the analog input. If a device claims to have no missing codes, it means that all possible codes (for a 14-bit converter, 16384 codes) are present over the full operating range.

Effective Number of Bits (ENOB)

The effective number of bits for a sine wave input at a given input frequency can be calculated directly from its measured SINAD using the following formula:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02}$$

If SINAD is not known, SNR can be used exceptionally to calculate ENOB (ENOB_{SNR}).

Effective Resolution Bandwidth

The highest input frequency where the SNR (dB) is dropped by 3dB for a full-scale input amplitude.

Gain Error

The amount of deviation between the ideal transfer function and the measured transfer function (with the offset error removed) when a full-scale analog input voltage is applied to the ADC, resulting in all 1s in the digital code. Gain error is usually given in LSB or as a percent of full-scale range (%FSR).

Integral Nonlinearity (INL)

INL is the deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" or "best fit" determined by a least square curve fit. INL is independent from effects of offset, gain or quantization errors.

Maximum Conversion Rate

The encode rate at which parametric testing is performed. This is the maximum sampling rate where certified operation is given.

Minimum Conversion Rate

This is the minimum sampling rate where the ADC still works.

Nyquist Sampling

When the sampled frequencies of the analog input signal are below $f_{\text{CLOCK}}/2$, it is called Nyquist sampling. The Nyquist frequency is $f_{\text{CLOCK}}/2$, which can vary depending on the sample rate (f_{CLOCK}).

Offset Error

Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

Propagation Delay

This is the delay between the input clock rising edge and the time when all data bits are within valid logic levels.

Signal-to-Noise and Distortion (SINAD)

The RMS value of the sine wave f_{IN} (input sine wave for an ADC) to the RMS value of the noise of the converter from DC to the Nyquist frequency, including harmonic content. It is typically expressed in decibels (dB). SINAD includes harmonics, but excludes DC.

$$\text{SINAD} = 20\text{Log}_{(10)} \frac{\text{Input}(V_s)}{\text{Noise} + \text{Harmonics}}$$

Signal-to-Noise Ratio (without harmonics)

SNR is a measure of signal strength relative to background noise. The ratio is usually measured in dB. If the incoming signal strength in μV is V_s , and the noise level (also in μV) is V_N , then the SNR in dB is given by the formula:

$$\text{SNR} = 20\text{Log}_{(10)} \frac{V_s}{V_N}$$

This is the ratio of the RMS signal amplitude, V_s (set 1dB below full-scale), to the RMS value of the sum of all other spectral components, V_N , excluding harmonics and DC.

Spurious-Free Dynamic Range (SFDR)

The ratio of the RMS value of the analog input sine wave to the RMS value of the peak spur observed in the frequency domain. It may be reported in dBc (that is, it degrades as signal levels are lowered), or in dBFS (always related back to converter full-scale). The peak spurious component may or may not be a harmonic.

Temperature Drift

Temperature drift (for offset error and gain error) specifies the maximum change from the initial temperature value to the value at T_{MIN} or T_{MAX} .

Total Harmonic Distortion (THD)

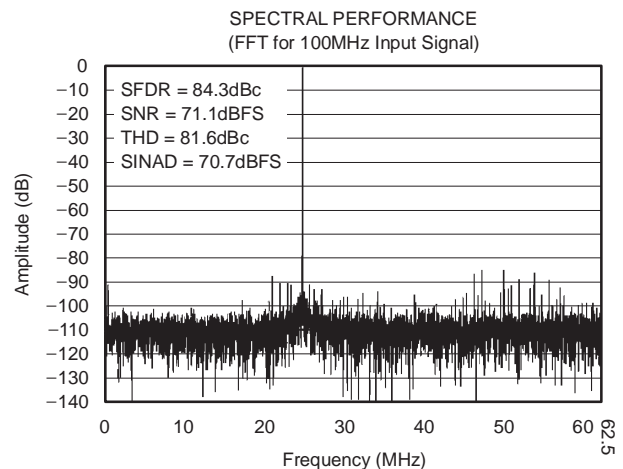
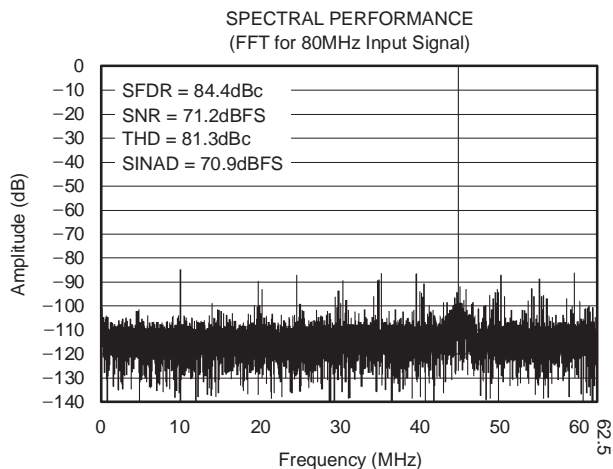
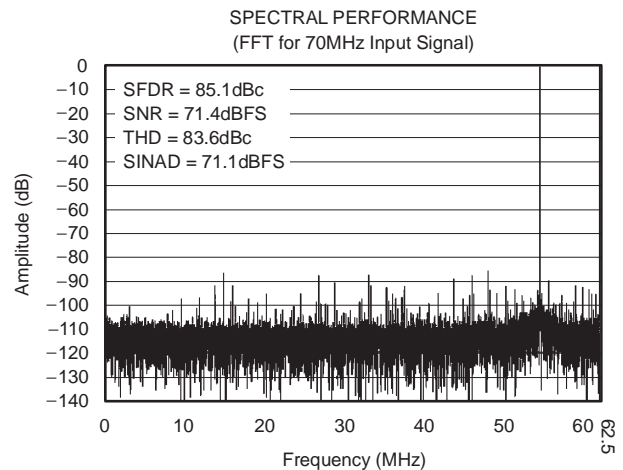
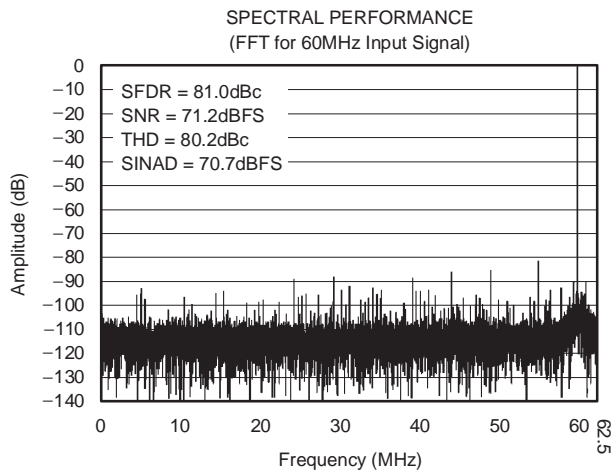
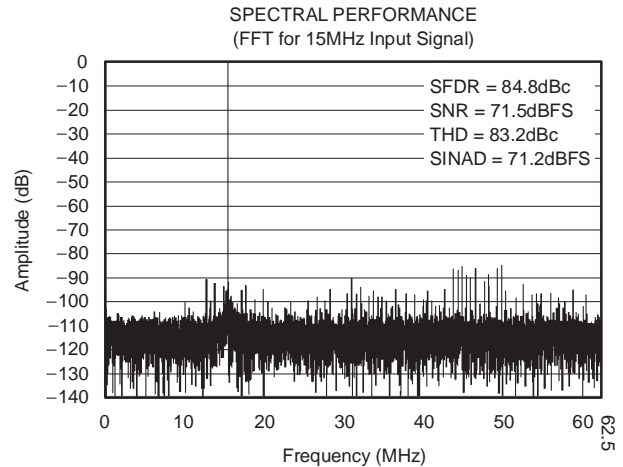
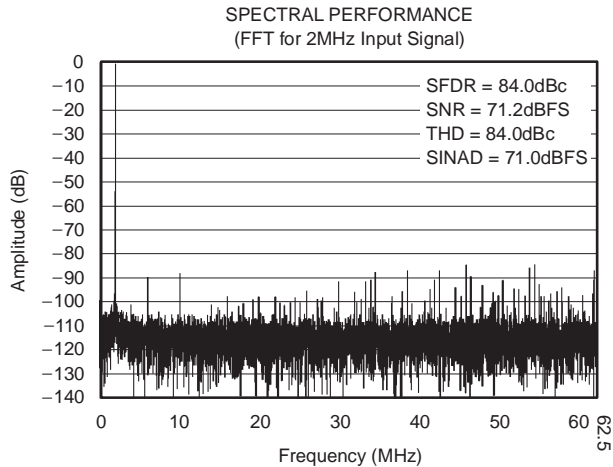
THD is the ratio of the RMS signal amplitude of the input sine wave to the RMS value of distortion appearing at multiples (harmonics) of the input, typically given in dBc.

Two-Tone Intermodulation Distortion Rejection

The ratio of the RMS value of either input tone (f_1, f_2) to the RMS value of the worst third-order intermodulation product ($2f_1 - f_2; 2f_2 - f_1$). It is reported in dBc.

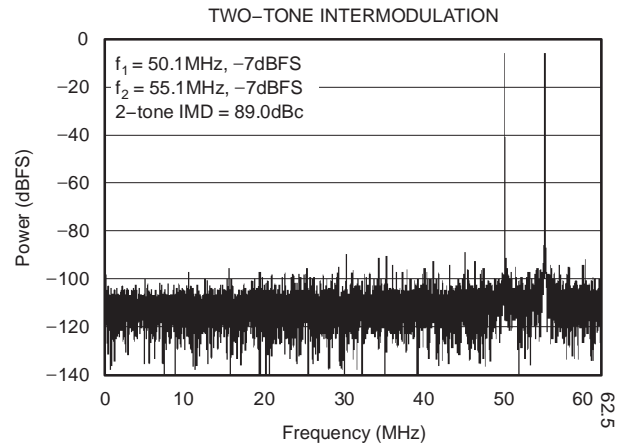
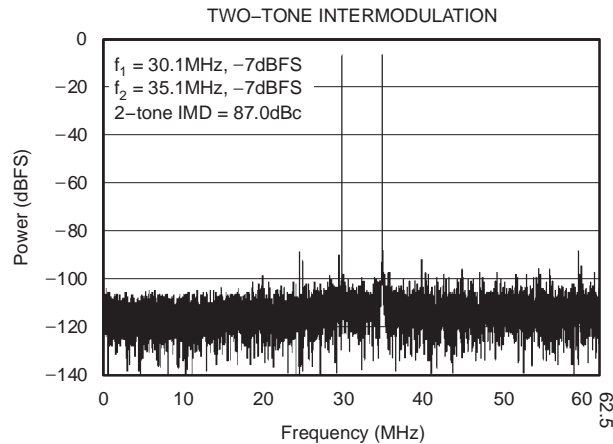
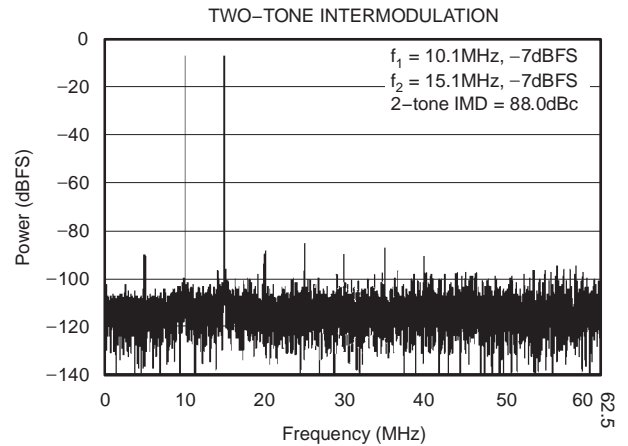
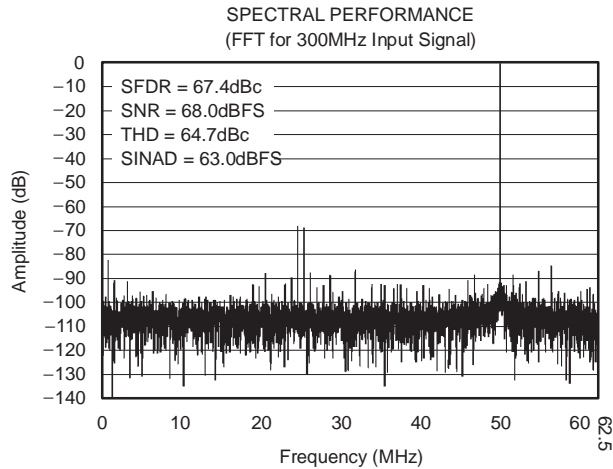
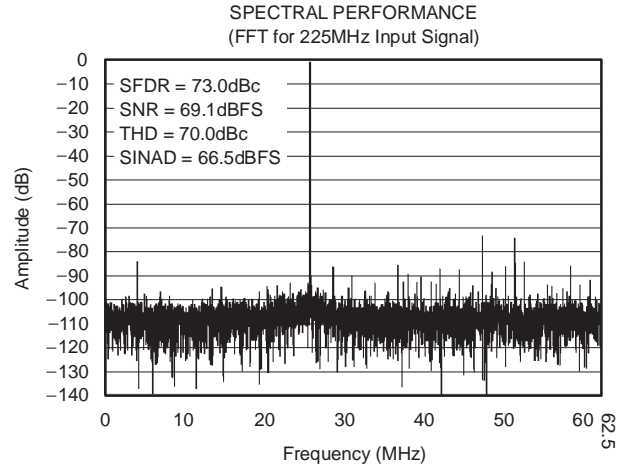
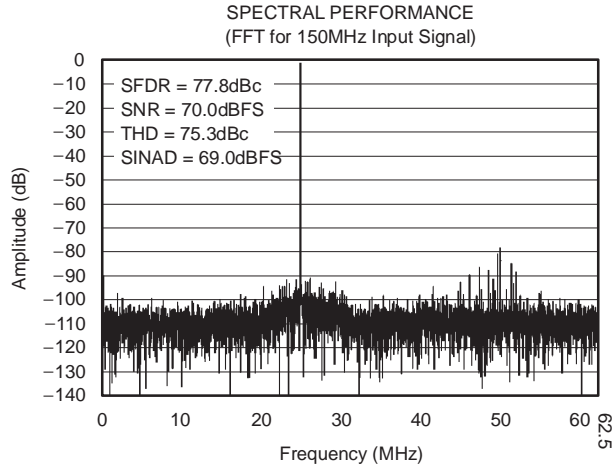
TYPICAL CHARACTERISTICS

Typical values are at $T_A = 25^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, differential input amplitude = -1dBFS , sampling rate = 125MSPS , and DLL On, unless otherwise noted.



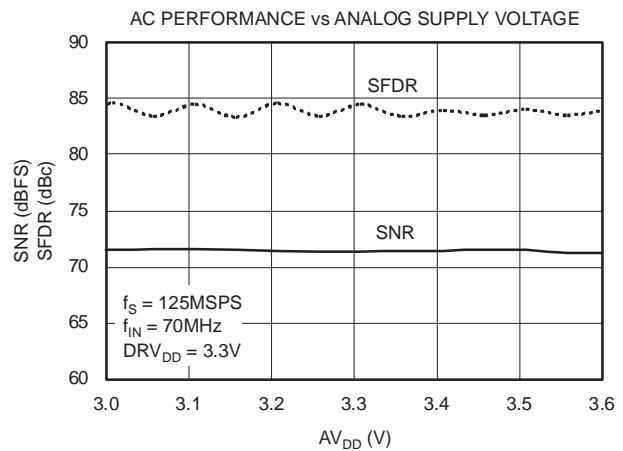
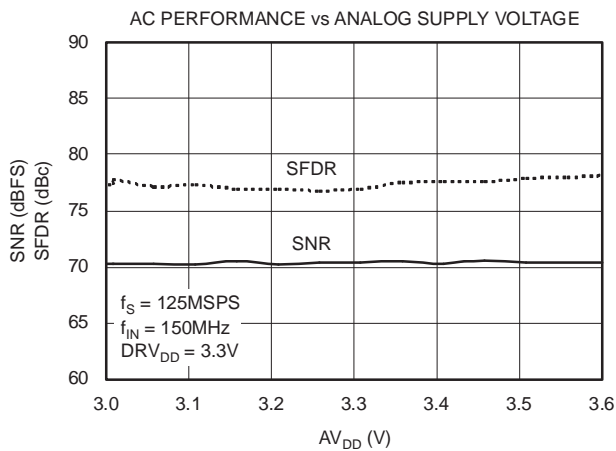
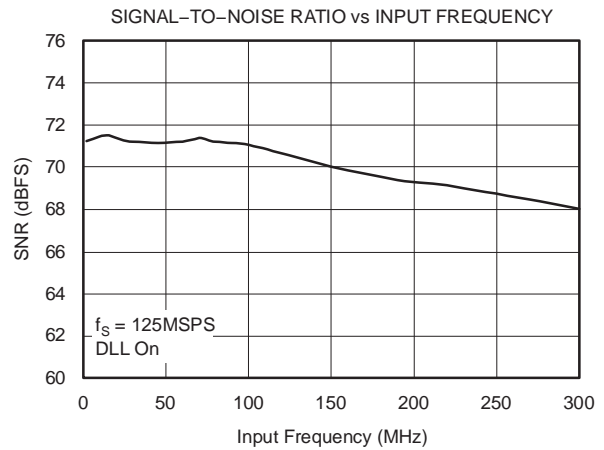
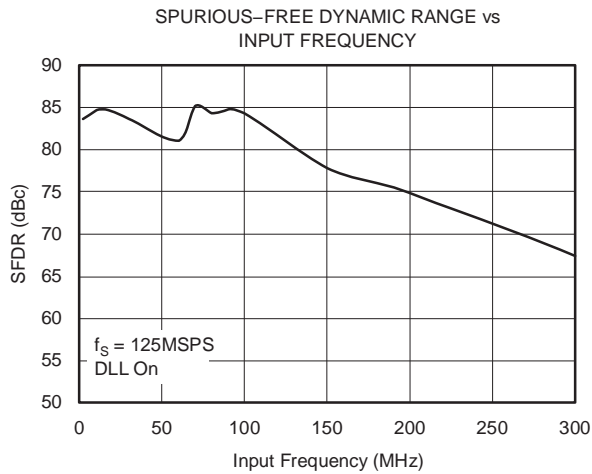
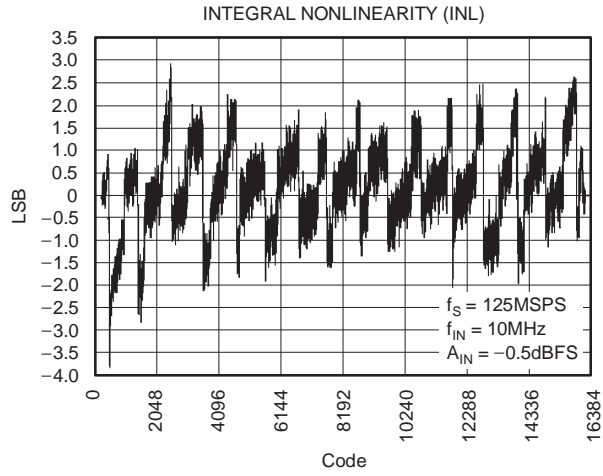
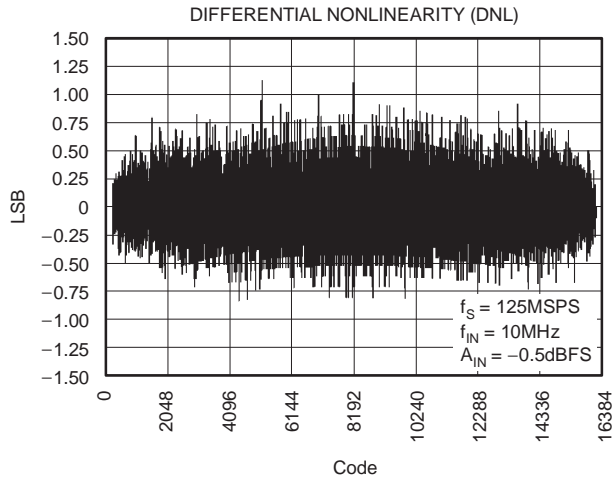
TYPICAL CHARACTERISTICS (continued)

Typical values are at $T_A = 25^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, differential input amplitude = -1dBFS , sampling rate = 125MSPS , and DLL On, unless otherwise noted.



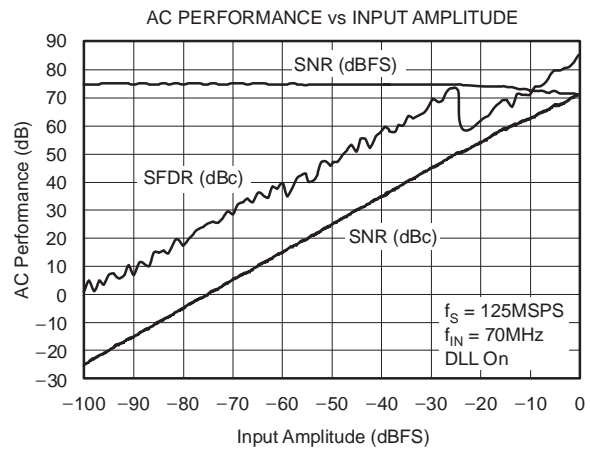
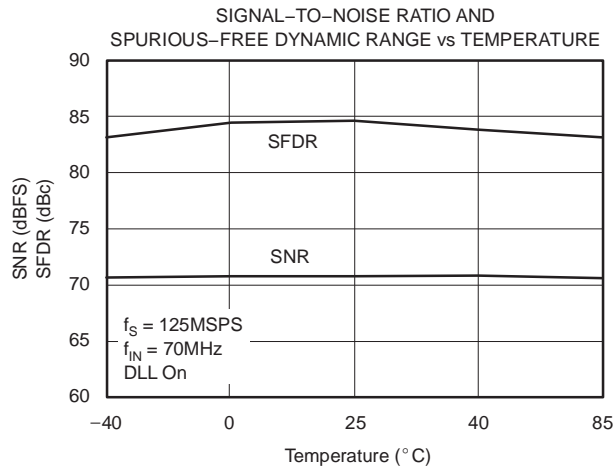
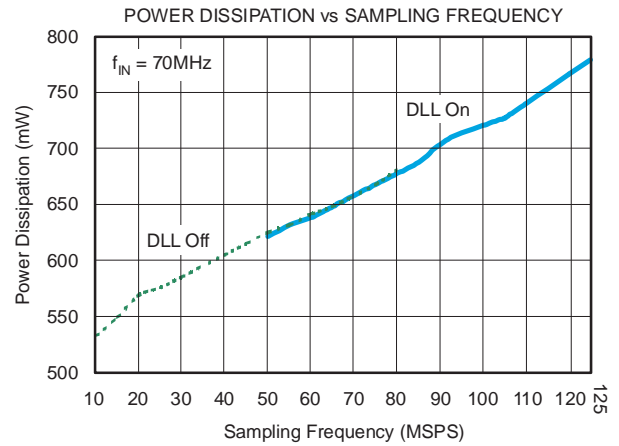
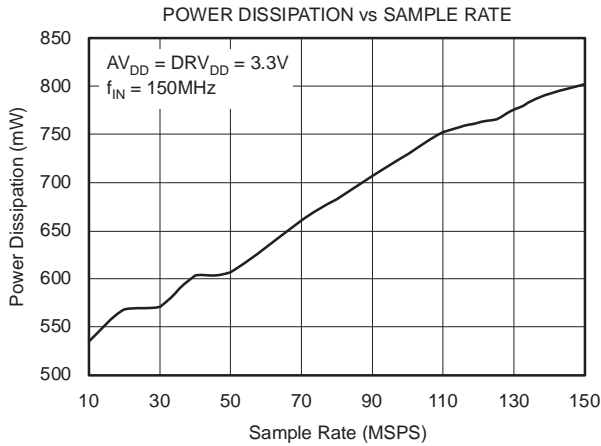
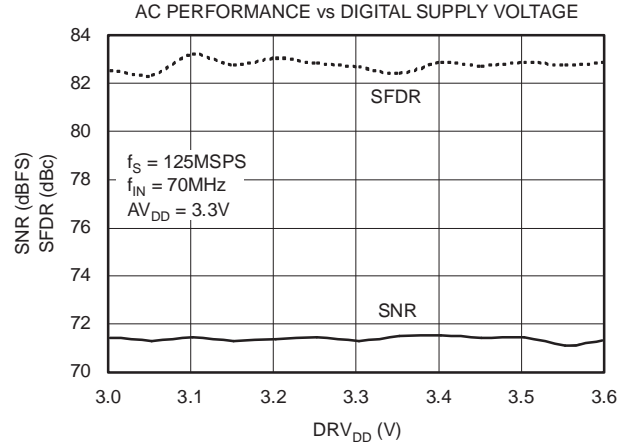
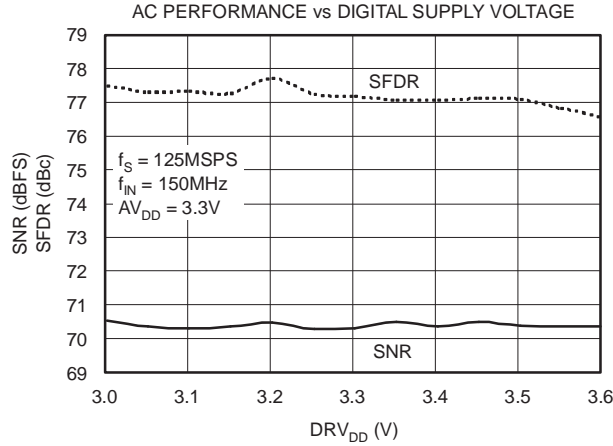
TYPICAL CHARACTERISTICS (continued)

Typical values are at $T_A = 25^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, differential input amplitude = -1dBFS , sampling rate = 125MSPS , and DLL On, unless otherwise noted.



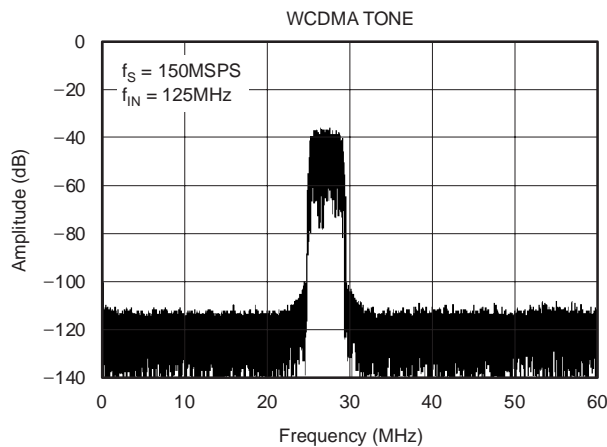
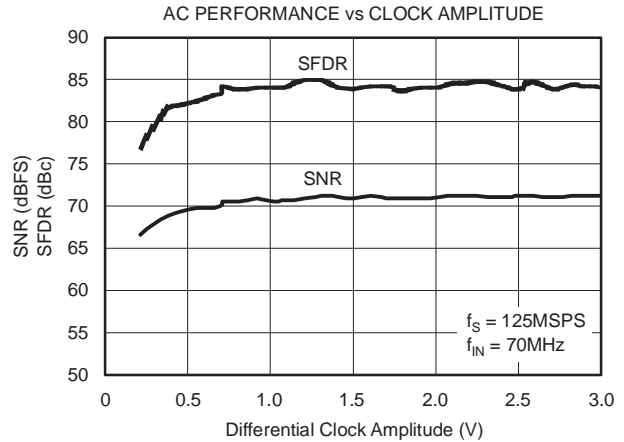
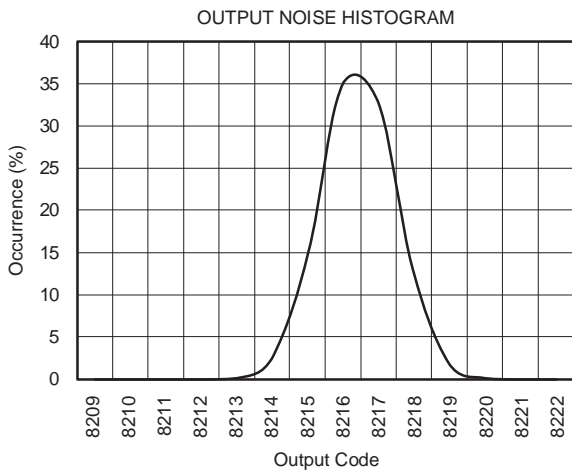
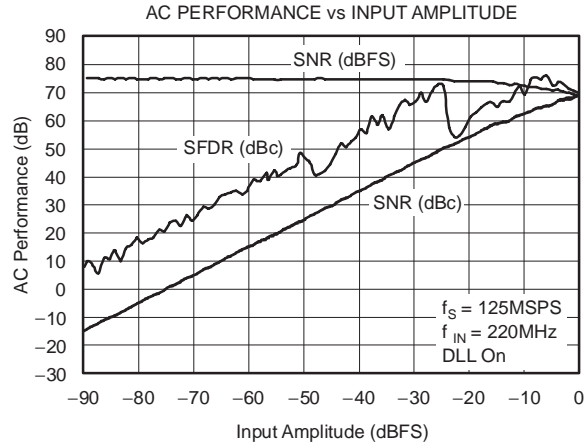
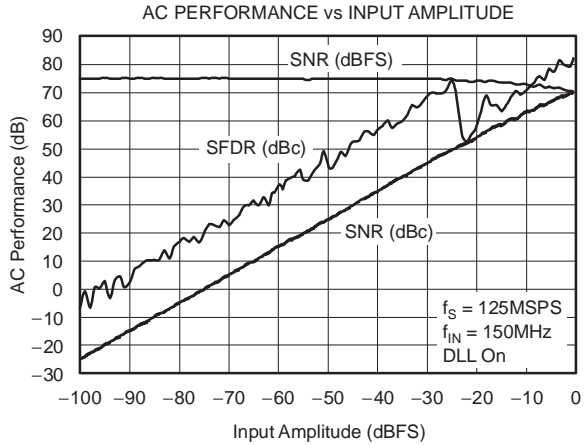
TYPICAL CHARACTERISTICS (continued)

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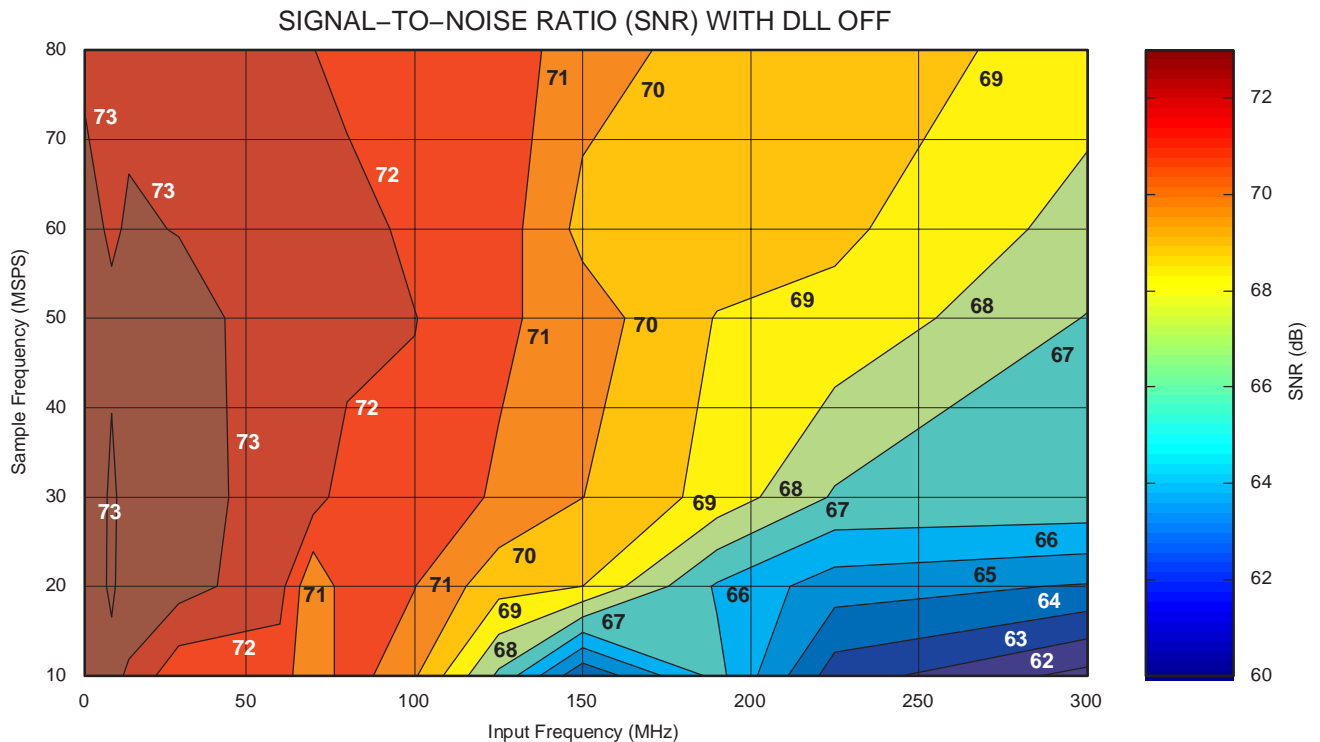
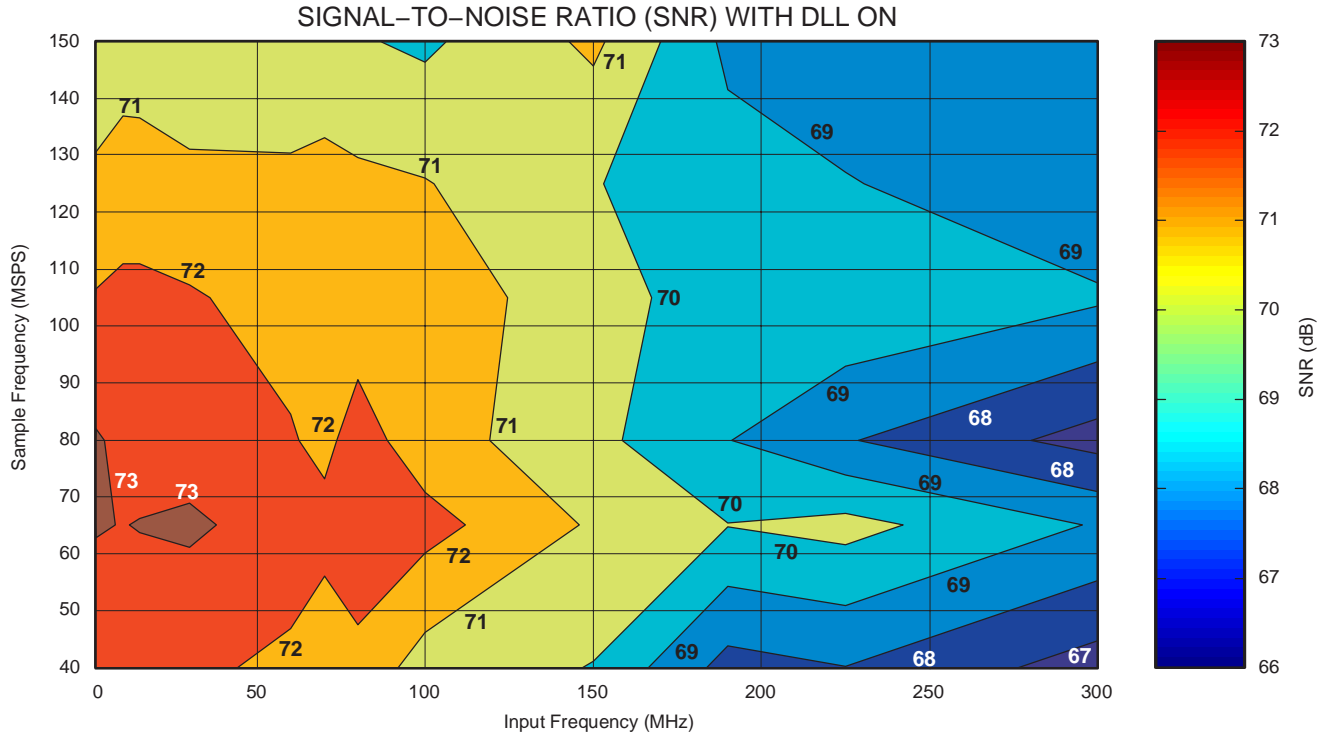
TYPICAL CHARACTERISTICS (continued)

Typical values are at $T_A = 25^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, differential input amplitude = -1dBFS , sampling rate = 125MSPS , and DLL On, unless otherwise noted.



TYPICAL CHARACTERISTICS (continued)

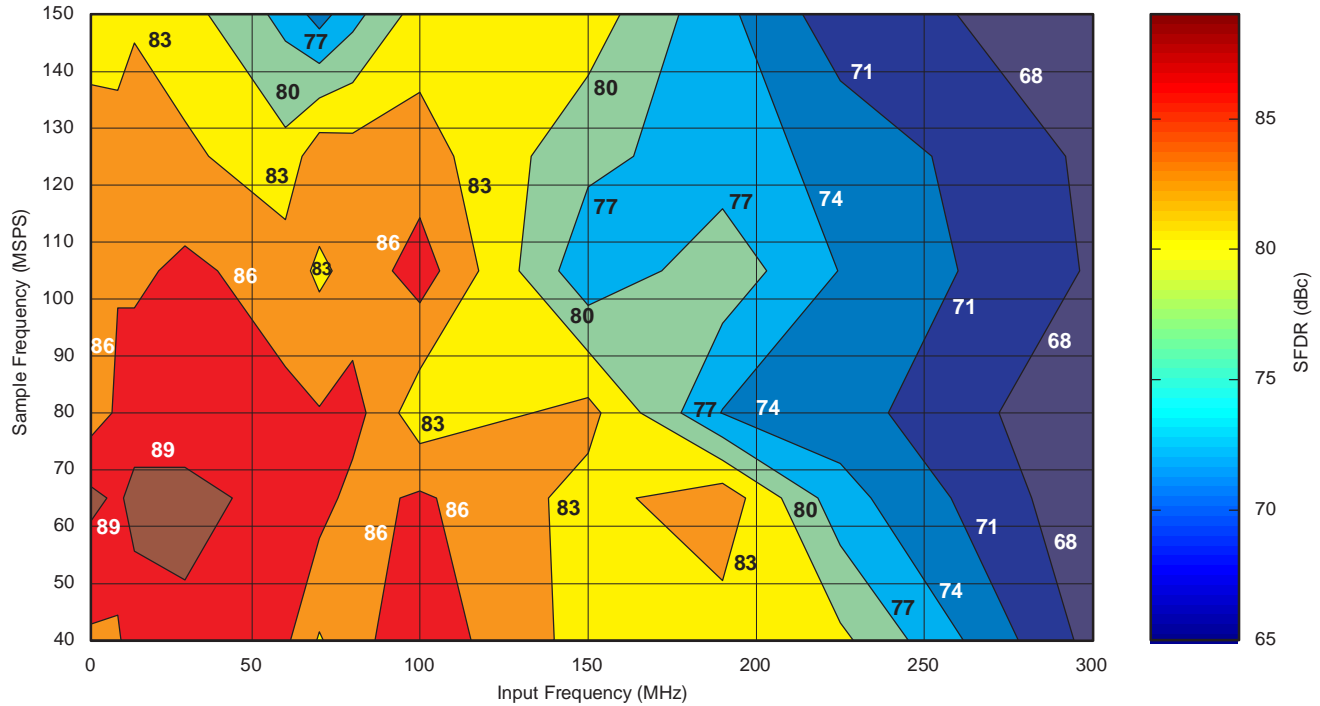
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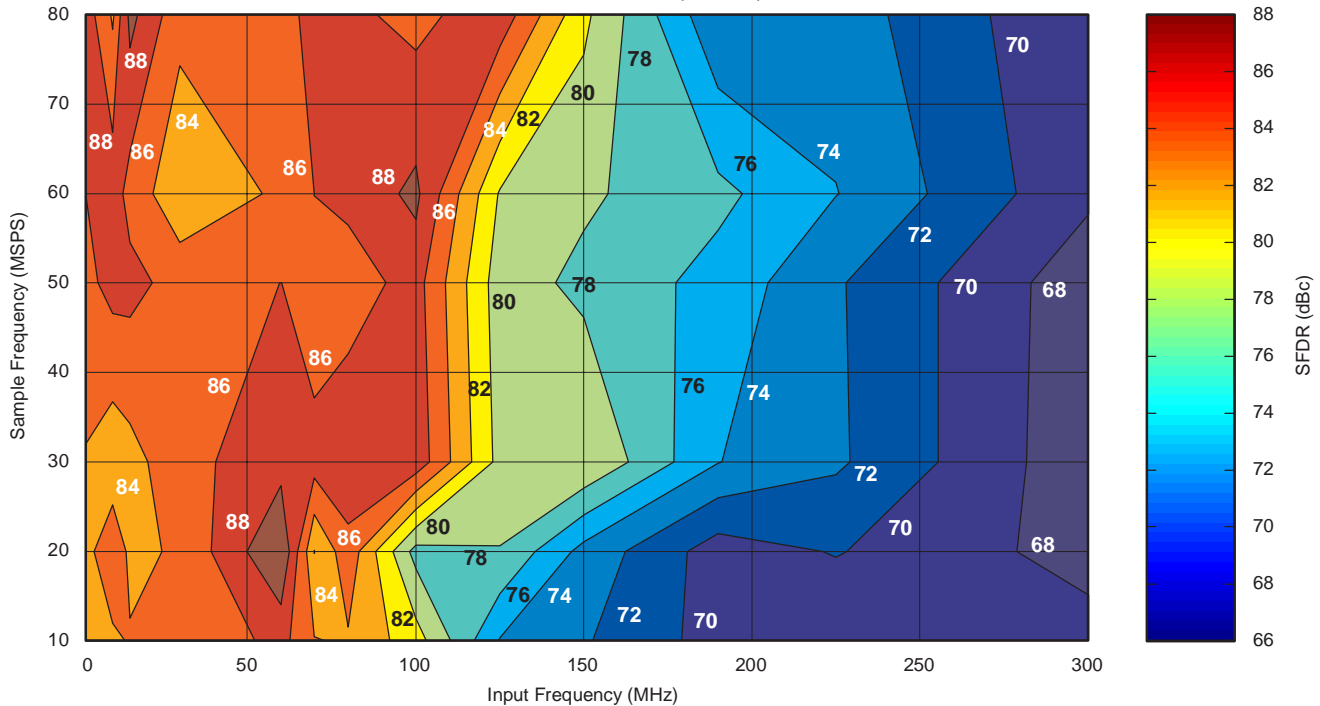
TYPICAL CHARACTERISTICS (continued)

Typical values are at $T_A = 25^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, differential input amplitude = -1dBFS , sampling rate = 125MSPS , and DLL On, unless otherwise noted.

SPURIOUS-FREE DYNAMIC RANGE (SFDR) WITH DLL ON

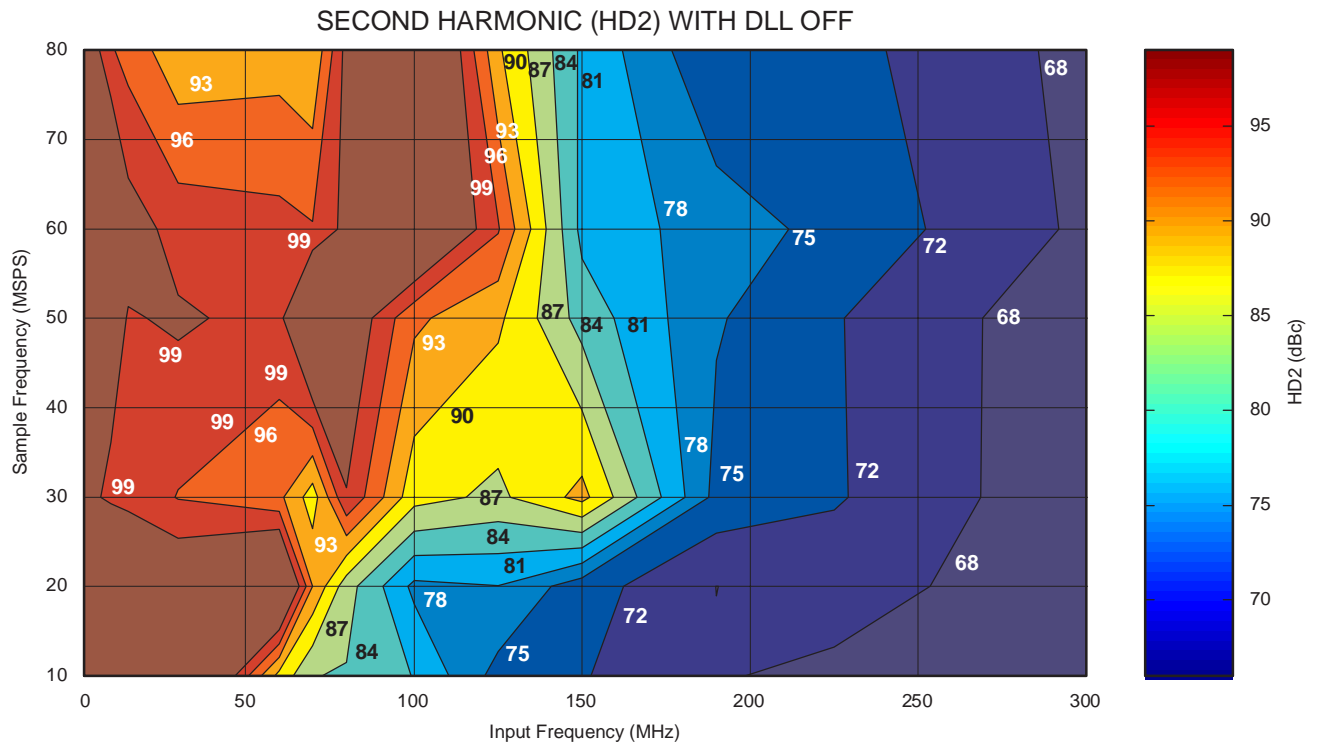
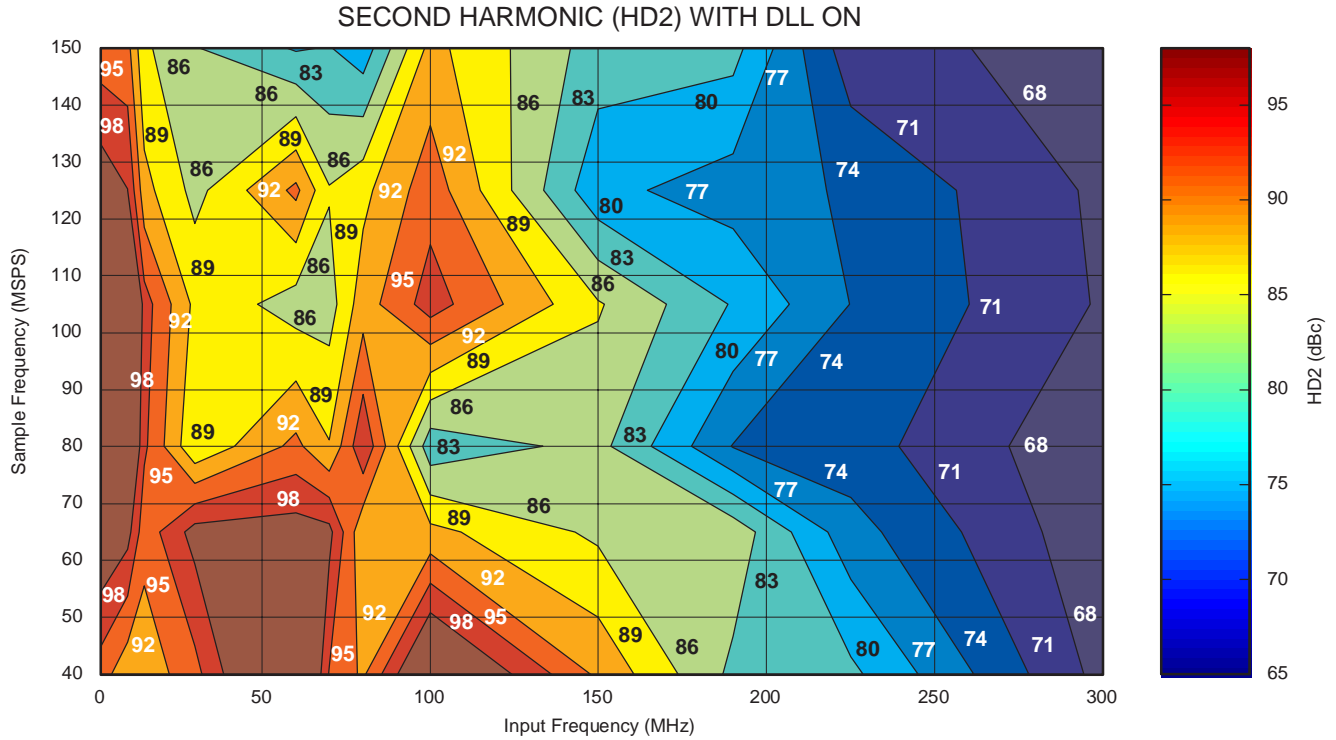


SPURIOUS-FREE DYNAMIC RANGE (SFDR) WITH DLL OFF



TYPICAL CHARACTERISTICS (continued)

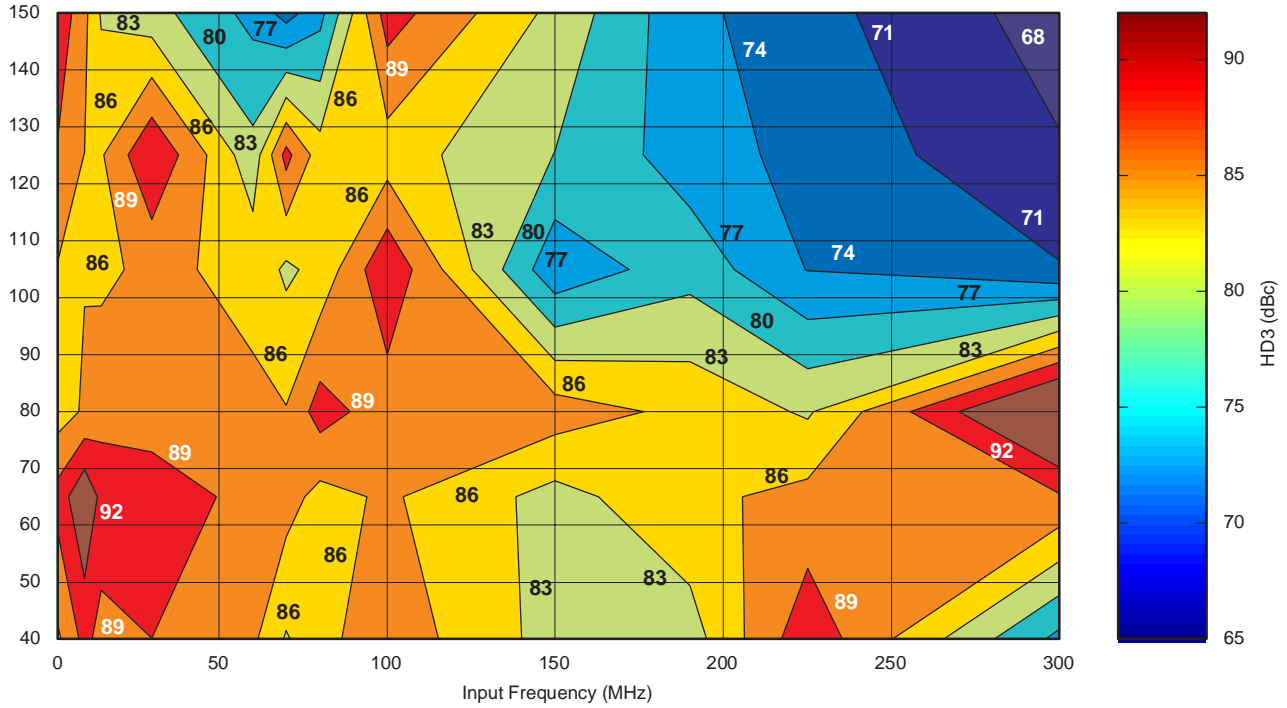
Typical values are at $T_A = 25^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, differential input amplitude = -1dBFS , sampling rate = 125MSPS , and DLL On, unless otherwise noted.



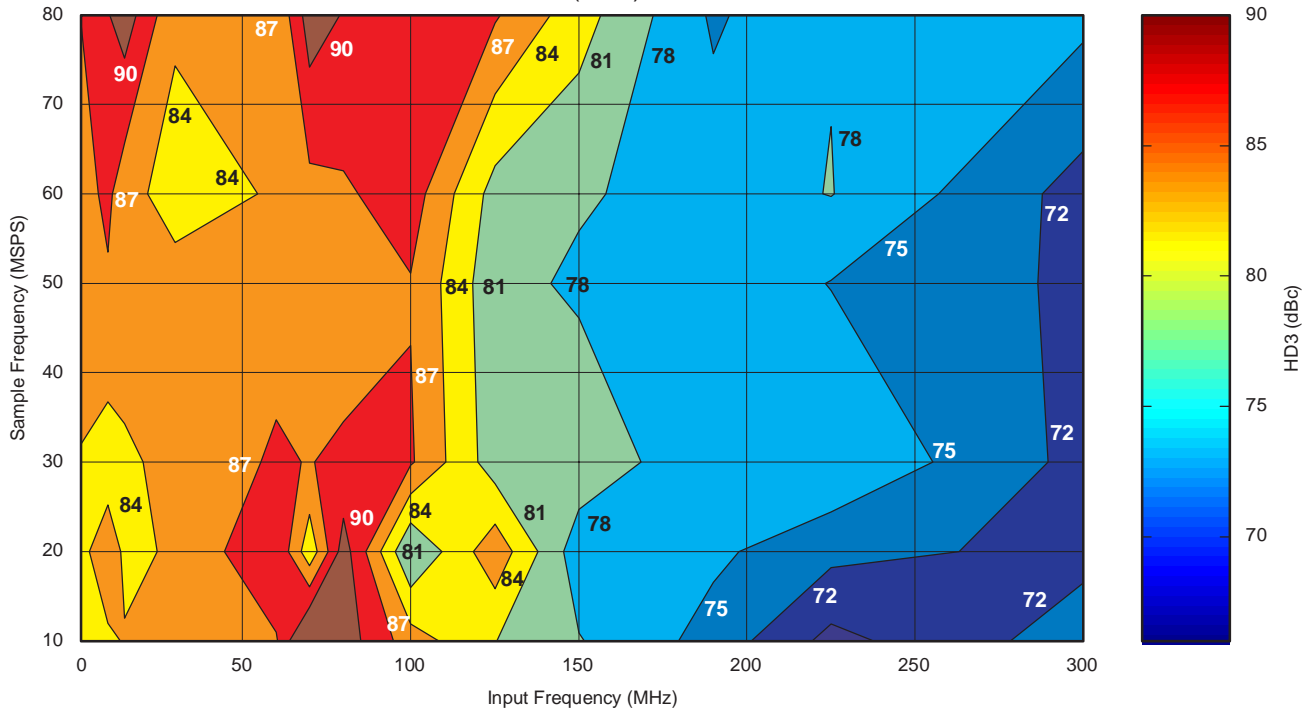
TYPICAL CHARACTERISTICS (continued)

Typical values are at $T_A = 25^\circ\text{C}$, $AV_{DD} = DRV_{DD} = 3.3\text{V}$, differential input amplitude = -1dBFS , sampling rate = 125MSPS , and DLL On, unless otherwise noted.

THIRD HARMONIC (HD3) WITH DLL ON



THIRD HARMONIC (HD3) WITH DLL OFF



APPLICATION INFORMATION

THEORY OF OPERATION

The ADS5500 is a low-power, 14-bit, 125MSPS, CMOS, switched capacitor, pipeline ADC that operates from a single 3.3V supply. The conversion process is initiated by a falling edge of the external input clock. Once the signal is captured by the input S&H, the input sample is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results

in a data latency of 16.5 clock cycles, after which the output data is available as a 14-bit parallel word, coded in either straight offset binary or binary two's complement format.

INPUT CONFIGURATION

The analog input for the ADS5500 consists of a differential sample-and-hold architecture implemented using a switched capacitor technique, shown in Figure 4.

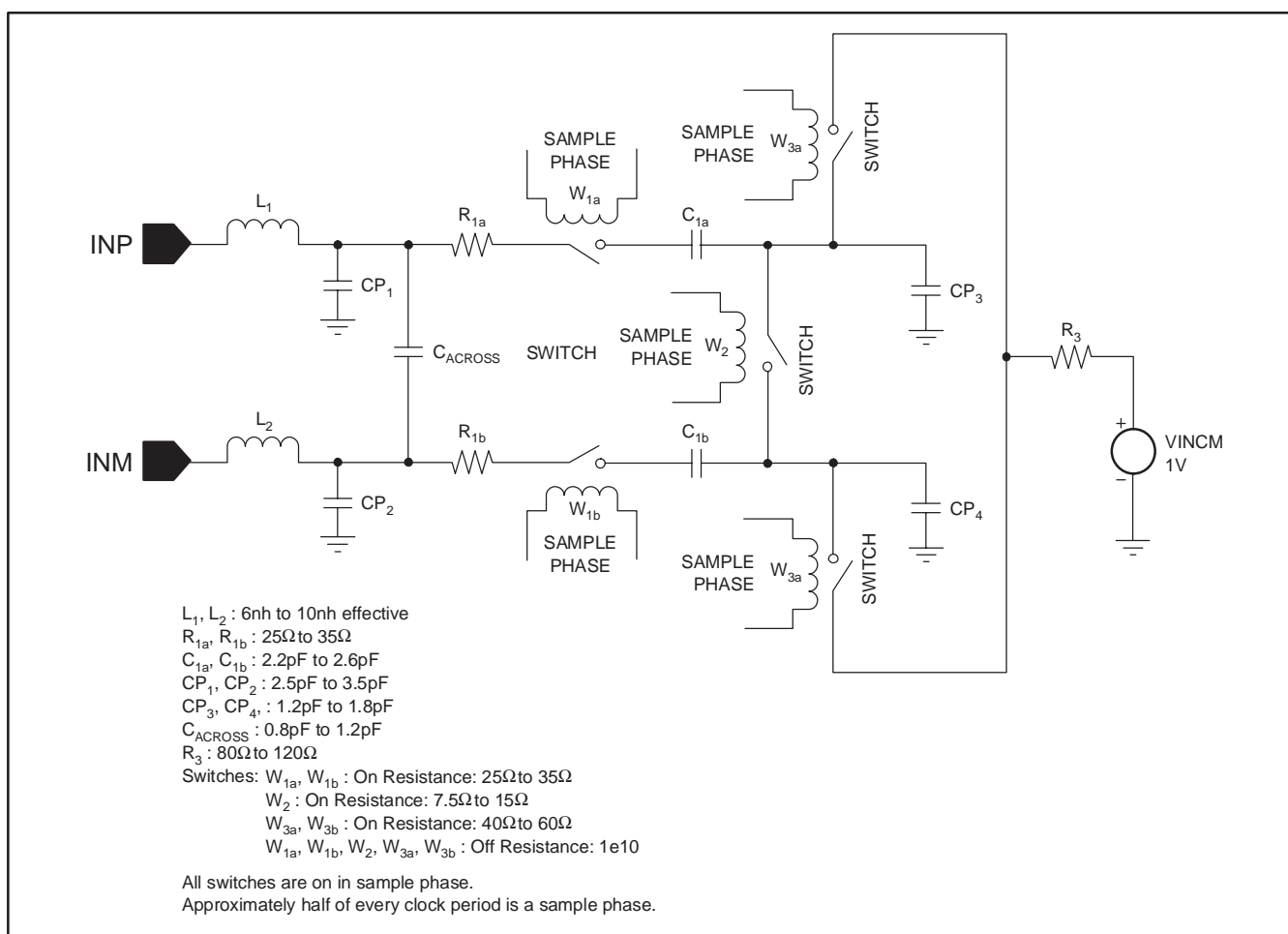


Figure 4. Analog Input Stage

This differential input topology produces a high level of AC performance for high sampling rates. It also results in a very high usable input bandwidth, especially important for high intermediate-frequency (IF) or undersampling applications. The ADS5500 requires each of the analog inputs (INP, INM) to be externally biased around the common-mode level of the internal circuitry (CM, pin 17). For a full-scale differential input, each of the differential lines of the input signal (pins 19 and 20) swings symmetrically between $CM + 0.575V$ and $CM - 0.575V$. This means that each input is driven with a signal of up to $CM \pm 0.575V$, so that each input has a maximum differential signal of $1.15V_{PP}$ for a total differential input signal swing of $2.3V_{PP}$. The maximum swing is determined by the two reference voltages, the top reference (REFP, pin 29), and the bottom reference (REFM, pin 30).

The ADS5500 obtains optimum performance when the analog inputs are driven differentially. The circuit shown in Figure 5 shows one possible configuration using an RF transformer.

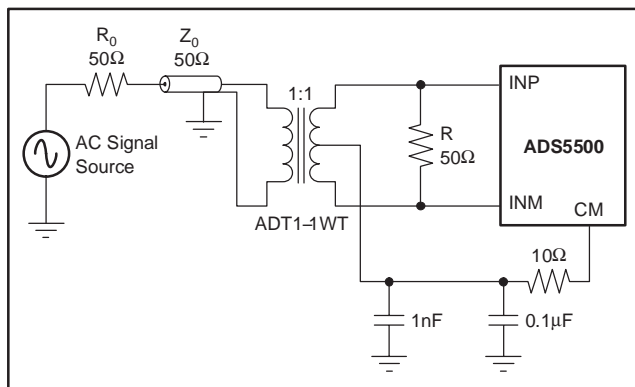


Figure 5. Transformer Input to Convert Single-Ended Signal to Differential Signal

The single-ended signal is fed to the primary winding of an RF transformer. Since the input signal must be biased around the common-mode voltage of the internal circuitry, the common-mode voltage (V_{CM}) from the ADS5500 is connected to the center-tap of the secondary winding. To ensure a steady low-noise V_{CM} reference, best performance is obtained when the CM (pin 17) output is filtered to ground with $0.1\mu F$ and $0.01\mu F$ low-inductance capacitors.

Output V_{CM} (pin 17) is designed to directly drive the ADC input. When providing a custom CM level, be aware that the input structure of the ADC sinks a common-mode current in the order of 4mA (2mA per input). Equation (1) describes the dependency of the common-mode current and the sampling frequency:

$$\frac{4mA \times f_s}{125MSPS} \tag{1}$$

Where:

$$f_s > 60MSPS.$$

This equation helps to design the output capability and impedance of the driving circuit accordingly.

When it is necessary to buffer or apply a gain to the incoming analog signal, it is possible to combine single-ended operational amplifiers with an RF transformer, or to use a differential input/output amplifier without a transformer, to drive the input of the ADS5500. TI offers a wide selection of single-ended operational amplifiers (including the THS3201, THS3202, OPA847, and OPA695) that can be selected depending on the application. An RF gain block amplifier, such as TI's THS9001, can also be used with an RF transformer for very high input frequency applications. The THS4503 is a recommended differential input/output amplifier. Table 4 lists the recommended amplifiers.

When using single-ended operational amplifiers (such as the THS3201, THS3202, OPA847, or OPA695) to provide gain, a three-amplifier circuit is recommended with one amplifier driving the primary of an RF transformer and one amplifier in each of the legs of the secondary driving the two differential inputs of the ADS5500. These three amplifier circuits minimize even-order harmonics. For very high frequency inputs, an RF gain block amplifier can be used to drive a transformer primary; in this case, the transformer secondary connections can drive the input of the ADS5500 directly, as shown in Figure 5, or with the addition of the filter circuit shown in Figure 6.

Figure 6 illustrates how R_{IN} and C_{IN} can be placed to isolate the signal source from the switching inputs of the ADC and to implement a low-pass RC filter to limit the input noise in the ADC. It is recommended that these components be included in the ADS5500 circuit layout when any of the amplifier circuits discussed previously are used. The components allow fine-tuning of the circuit performance. Any mismatch between the differential lines of the ADS5500 input produces a degradation in performance at high input frequencies, mainly characterized by an increase in the even-order harmonics. In this case, special care should be taken to keep as much electrical symmetry as possible between both inputs.

Another possible configuration for lower-frequency signals is the use of differential input/output amplifiers that can simplify the driver circuit for applications requiring DC coupling of the input. Flexible in their configurations (see Figure 7), such amplifiers can be used for single-ended-to-differential conversion, signal amplification.

Table 4. Recommended Amplifiers to Drive the Input of the ADS5500

INPUT SIGNAL FREQUENCY	RECOMMENDED AMPLIFIER	TYPE OF AMPLIFIER	USE WITH TRANSFORMER?
DC to 20MHz	THS4503	Differential In/Out Amp	No
DC to 50MHz	OPA847	Operational Amp	Yes
10MHz to 120MHz	OPA695	Operational Amp	Yes
	THS3201	Operational Amp	Yes
	THS3202	Operational Amp	Yes
Over 100MHz	THS9001	RF Gain Block	Yes

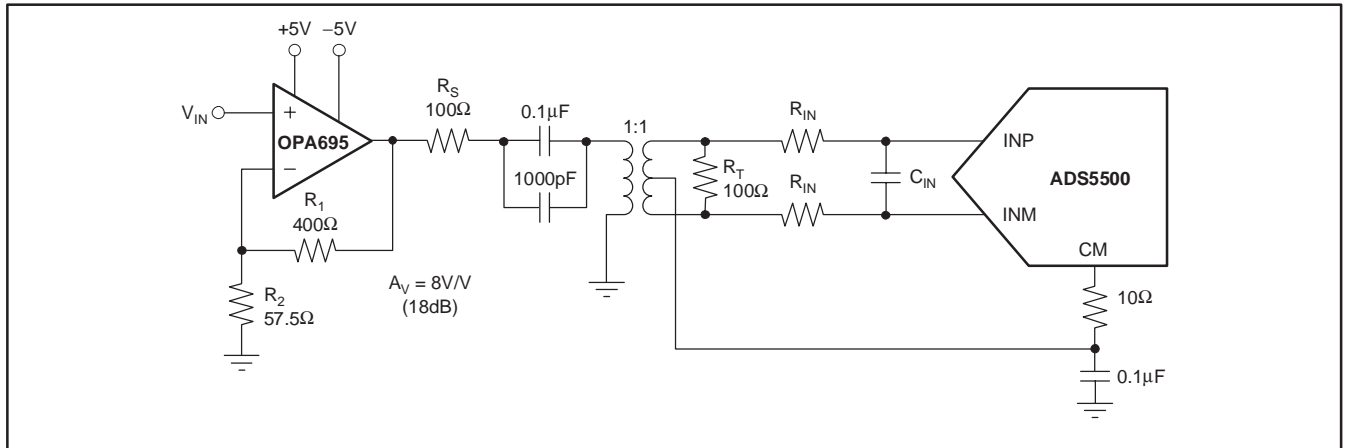


Figure 6. Converting a Single-Ended Input Signal to a Differential Signal Using an RF Transformer

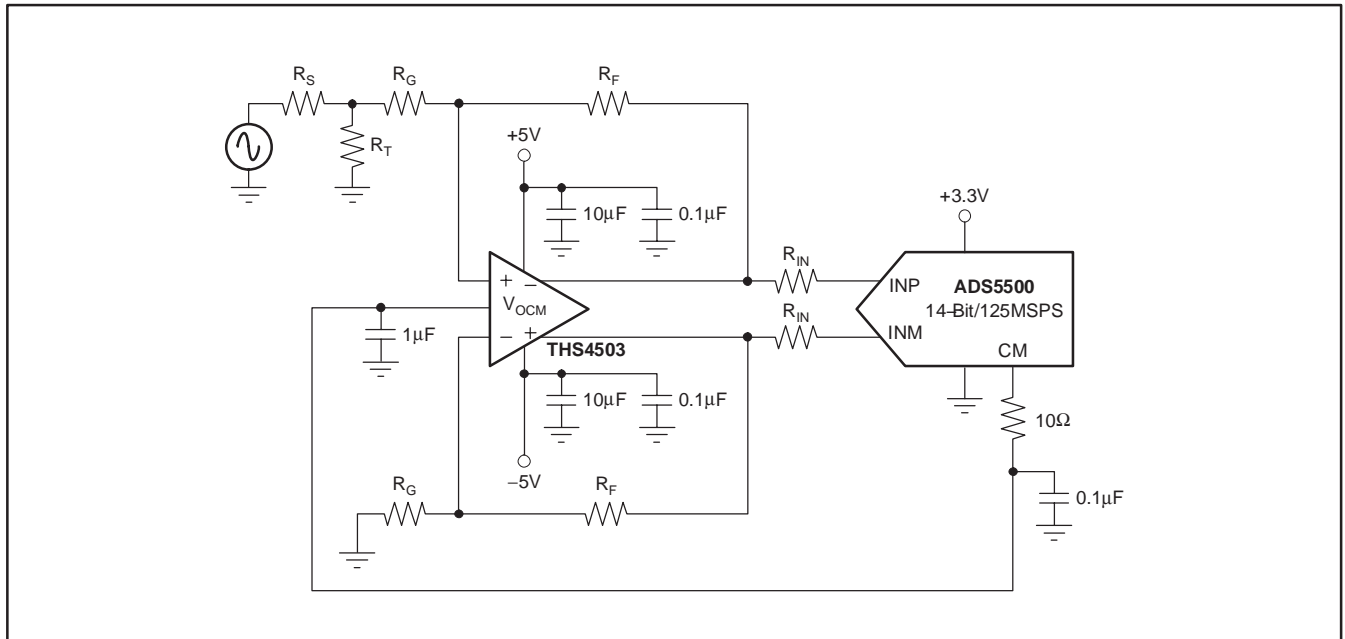


Figure 7. Using the THS4503 with the ADS5500

POWER SUPPLY SEQUENCE

The ADS5500 requires a power-up sequence where the DRV_{DD} supply must be at least 0.4V by the time the AV_{DD} supply reaches 3.0V. Powering up both supplies at the same time will work without any problem. If this sequence is not followed, the device may stay in power-down mode.

POWER DOWN

The device will enter power-down in one of two ways: either by reducing the clock speed to between DC and 1MHz, or by setting a bit through the serial programming interface. Using the reduced clock speed, the power-down may be initiated for clock frequencies below 10MHz. For clock frequencies between 1MHz and 10MHz, this can vary from device to device, but will power-down for clock speeds below 1MHz.

The device can be powered down by programming the internal register (see *Serial Programming Interface* section). The outputs become tri-stated and only the internal reference is powered up to shorten the power-up time. The Power-Down mode reduces power dissipation to a minimum of 180mW.

REFERENCE CIRCUIT

The ADS5500 has built-in internal reference generation, requiring no external circuitry on the printed circuit board (PCB). For optimum performance, it is best to connect both REFP and REFM to ground with a $1\mu\text{F}$ decoupling capacitor in series with a 1Ω resistor, as shown in Figure 8. In addition, an external $56.2\text{k}\Omega$ resistor should be connected from IREF (pin 31) to AGND to set the proper current for the operation of the ADC, as shown in Figure 8. No capacitor should be connected between pin 31 and ground; only the $56.2\text{k}\Omega$ resistor should be used.

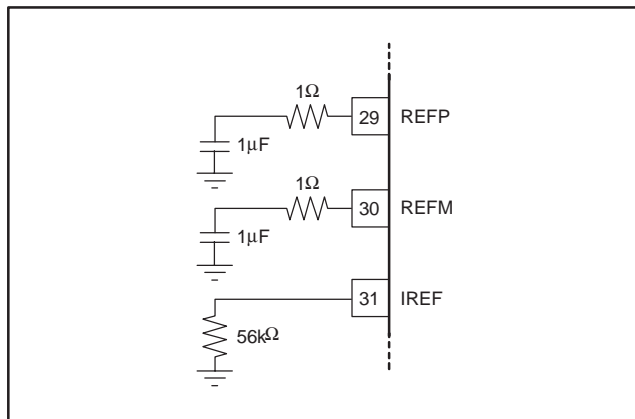


Figure 8. REFP, REFM, and IREF Connections for Optimum Performance

CLOCK INPUT

The ADS5500 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. The common-mode voltage of the clock inputs is set internally to CM (pin 17) using internal $5\text{k}\Omega$ resistors that connect CLKP (pin 10) and CLKM (pin 11) to CM (pin 17), as shown in Figure 9.

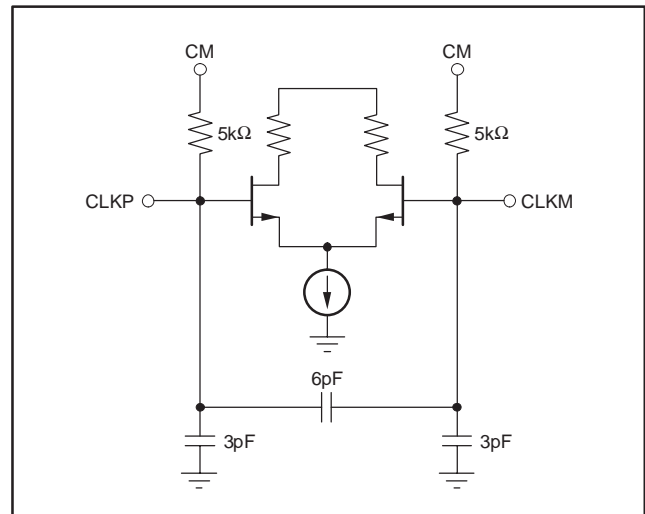


Figure 9. Clock Inputs

When driven with a single-ended CMOS clock input, it is best to connect CLKM (pin 11) to ground with a $0.01\mu\text{F}$ capacitor, while CLKP is AC-coupled with a $0.01\mu\text{F}$ capacitor to the clock source, as shown in Figure 10.

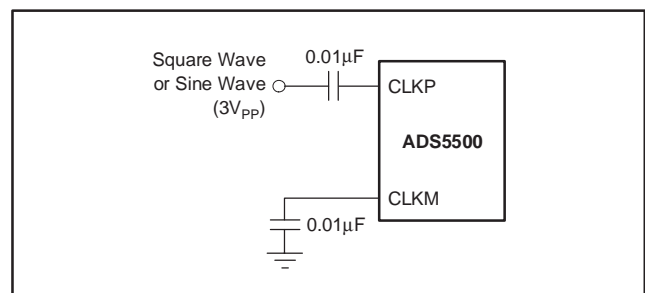


Figure 10. AC-Coupled, Single-Ended Clock Input

The ADS5500 clock input can also be driven differentially, reducing susceptibility to common-mode noise. In this case, it is best to connect both clock inputs to the differential input clock signal with $0.01\mu\text{F}$ capacitors, as shown in Figure 11.

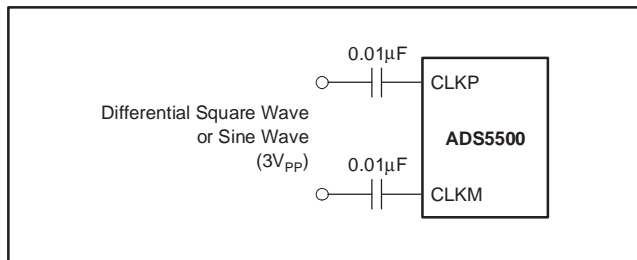


Figure 11. AC-Coupled, Differential Clock Input

For high input frequency sampling, it is recommended to use a clock source with very low jitter. Additionally, the internal ADC core uses both edges of the clock for the conversion process. This means that, ideally, a 50% duty cycle should be provided. Figure 12 shows the performance variation of the ADC versus clock duty cycle.

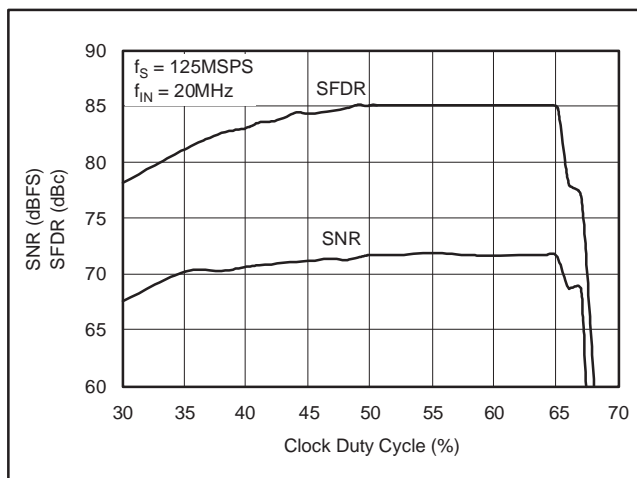


Figure 12. AC Performance vs Clock Duty Cycle

Bandpass filtering of the source can help produce a 50% duty cycle clock and reduce the effect of jitter. When using a sinusoidal clock, the clock jitter will further improve as the amplitude is increased. In that sense, using a differential clock allows for the use of larger

amplitudes without exceeding the supply rails and absolute maximum ratings of the ADC clock input. Figure 13 shows the performance variation of the device versus input clock amplitude. For detailed clocking schemes based on transformer or PECL-level clocks, refer to the ADS5500EVM User's Guide (SLWU010), available for download from www.ti.com.

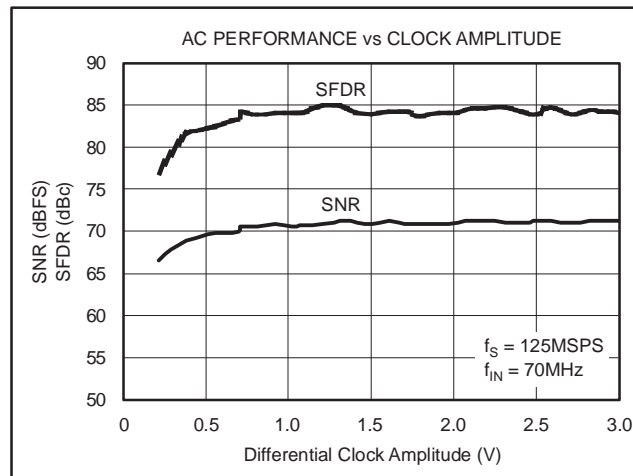


Figure 13. AC Performance vs Clock Amplitude

INTERNAL DLL

In order to obtain the fastest sampling rates achievable with the ADS5500, the device uses an internal digital phase lock loop (DLL). Nevertheless, the limited frequency range of operation of DLL degrades the performance at clock frequencies below 60MSPS. In order to operate the device below 60MSPS, the internal DLL must be shut off using the DLL OFF mode described in the *Serial Interface Programming* section. The Typical Performance Curves show the performance obtained in both modes of operation: DLL ON (default), and DLL OFF. In either of the two modes, the device will enter power down mode if no clock or slow clock is provided. The limit of the clock frequency where the device will function properly is ensured to be over 10MHz.

OUTPUT INFORMATION

The ADC provides 14 data outputs (D13 to D0, with D13 being the MSB and D0 the LSB), a data-ready signal (CLKOUT, pin 43), and an out-of-range indicator (OVR, pin 64) that equals 1 when the output reaches the full-scale limits.

Two different output formats (straight offset binary or two's complement) and two different output clock polarities (latching output data on rising or falling edge of the output clock) can be selected by setting DFS (pin 40) to one of four different voltages. Table 3 details the four modes. In addition, output enable control (OE, pin 41, active high) is provided to tri-state the outputs.

The output circuitry of the ADS5500 has been designed to minimize the noise produced by the transients of the data switching, and in particular its coupling to the ADC analog circuitry. Output D4 (pin 51) senses the load capacitance and adjusts the drive capability of all the output pins of the ADC to maintain the same output slew rate described in the timing diagram of Figure 1, as long as all outputs (including CLKOUT) have a similar load as the one at D4 (pin 51). This circuit also reduces the sensitivity of the output timing versus supply voltage or temperature. External series resistors with the output are not necessary.

SERIAL PROGRAMMING INTERFACE

The ADS5500 has internal registers for the programming of some of the modes described in the previous sections. The registers should be reset after power-up by applying a 2 μ s (minimum) high pulse on RESET (pin 35); this also resets the entire ADC and sets the data outputs to low. This pin has a 200k Ω internal pull-up resistor to AV_{DD}. The programming is done through a three-wire interface. The timing diagram and serial register setting in the *Serial Programming Interface* section describe the programming of this register.

Table 2 shows the different modes and the bit values to be written on the register to enable them.

Note that some of these modes may modify the standard operation of the device and possibly vary the performance with respect to the typical data shown in this data sheet.

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
ADS5500IPAP	ACTIVE	HTQFP	PAP	64	160
ADS5500IPAPR	ACTIVE	HTQFP	PAP	64	1000

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

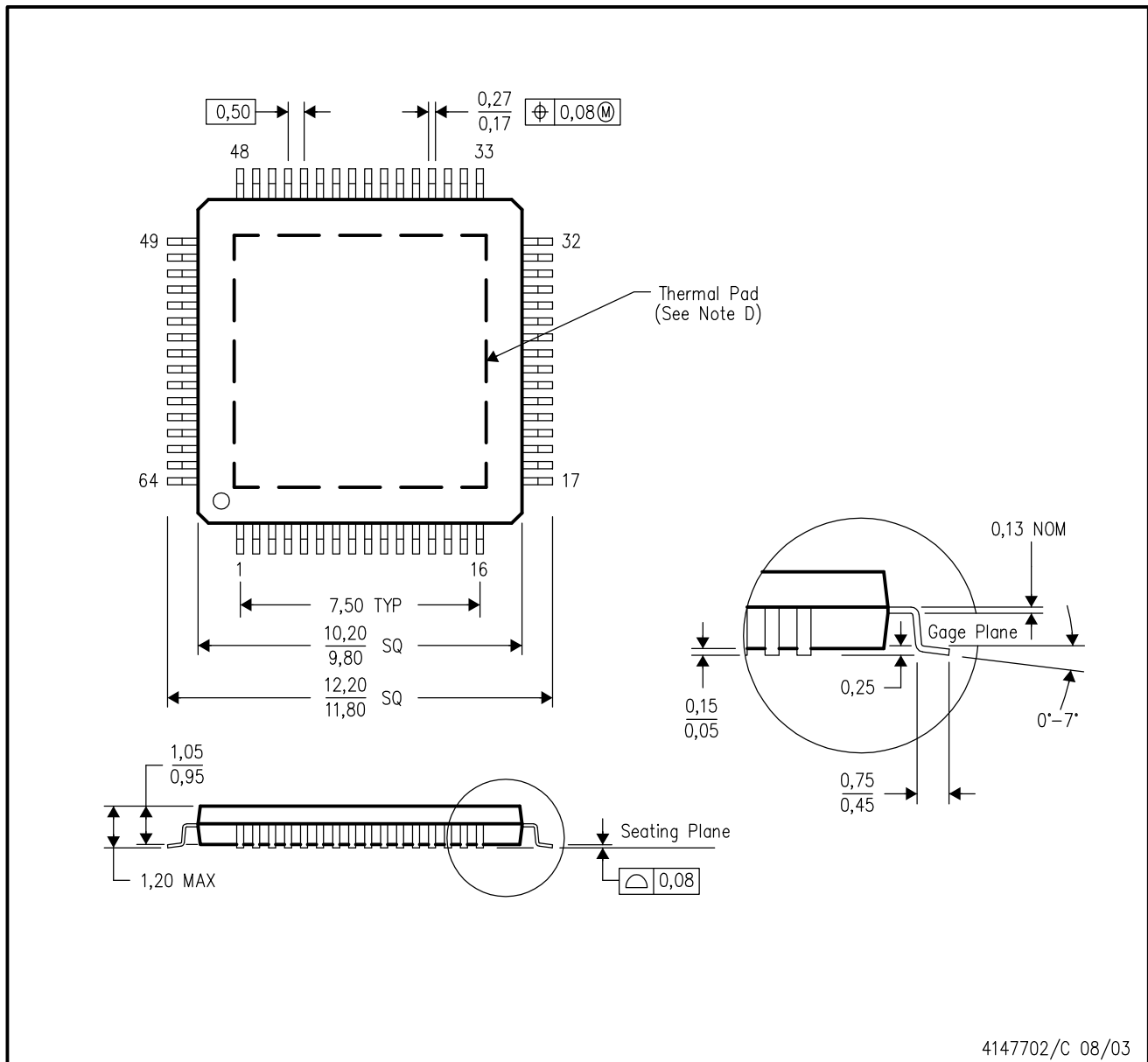
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

PAP (S-PQFP-G64)

PowerPAD™ PLASTIC QUAD FLATPACK



4147702/C 08/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. Falls within JEDEC MS-026

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