- ● Members of the Texas Instruments *Widebus*™ Family

- ● Inputs Are TTL-Voltage Compatible

- ● 3-State Outputs Drive Bus Lines Directly

- ● Flow-Through Architecture Optimizes PCB Layout

- ● Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise

- ● *EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process

- ● 500-mA Typical Latch-Up Immunity at 125°C

- ● Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

54ACT16863 . . . WD PACKAGE
74ACT16863 . . . DL PACKAGE
(TOP VIEW)

1OEAB	1	56	1OEBA
1B1	2	55	1A1
1B2	3	54	1A2
GND	4	53	GND
1B3	5	52	1A3
1B4	6	51	1A4
V_{CC}	7	50	V_{CC}
1B5	8	49	1A5
1B6	9	48	1A6
1B7	10	47	1A7
GND	11	46	GND
1B8	12	45	1A8
1B9	13	44	1A9
GND	14	43	GND
GND	15	42	GND
2B1	16	41	2A1
2B2	17	40	2A2
GND	18	39	GND
2B3	19	38	2A3
2B4	20	37	2A4
2B5	21	36	2A5
V_{CC}	22	35	V_{CC}
2B6	23	34	2A6
2B7	24	33	2A7
GND	25	32	GND
2B8	26	31	2A8
2B9	27	30	2A9
2OEAB	28	29	2OEBA
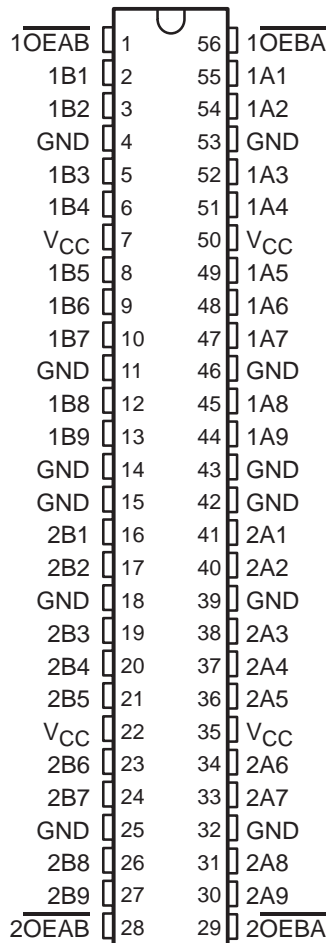
description

The 'ACT16863 are 18-bit noninverting transceivers designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

The 'ACT16863 can be used as two 9-bit transceivers or one 18-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs.

The 74ACT16863 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16863 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16863 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 9-bit section)

INPUTS		OPERATION
$\overline{OEAB}$	$\overline{OEBA}$	
H	L	B data to A bus
L	H	A data to B bus
H	H	Isolation

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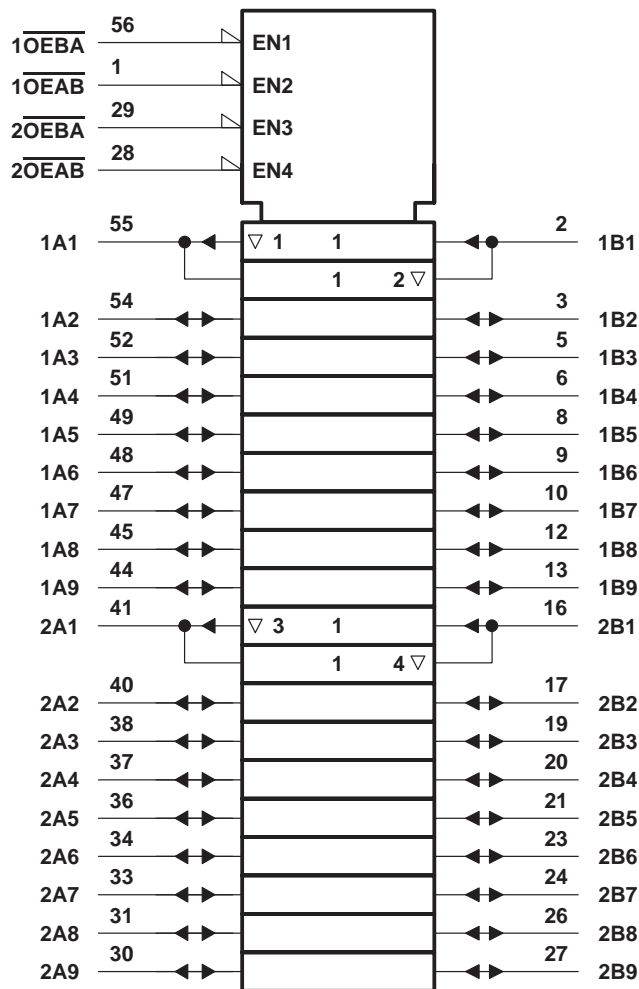
logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)
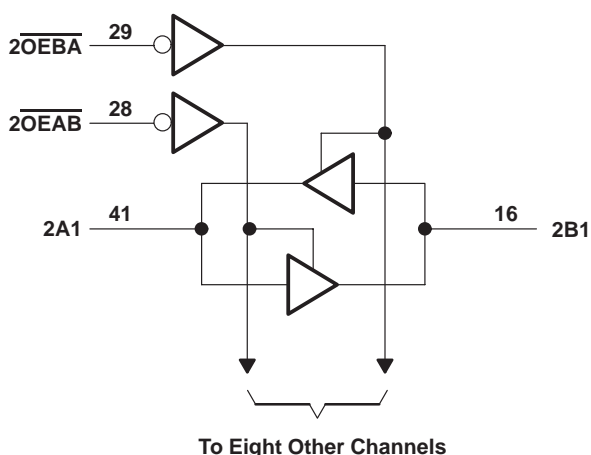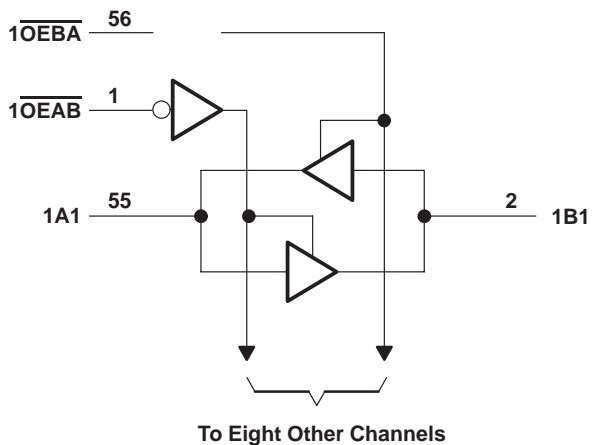
To Eight Other Channels

To Eight Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . ±450 mA
Maximum package power dissipation at T_A = 55°C (in still air) (see Note 2): DL package . . . . 1.4 W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
　　　　 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 2)

		54ACT16863			74ACT16863			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			–24			–24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25°C$			54ACT16863		74ACT16863		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		$I_{OH} = -50\ \mu A$	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		$I_{OH} = -24\ mA$	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		$I_{OH} = -50\ mA†$	5.5 V				3.85				
		$I_{OH} = -75\ mA†$	5.5 V						3.85		
V_{OL}		$I_{OL} = 50\ \mu A$	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		$I_{OL} = 24\ mA$	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		$I_{OL} = 50\ mA†$	5.5 V					1.65			
		$I_{OL} = 75\ mA†$	5.5 V							1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
$I_{OZ}‡$	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, $\quad I_O = 0$	5.5 V			8		160		80	μA
$\Delta I_{CC}§$		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		17						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\ V \pm 0.5\ V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			54ACT16863		74ACT16863		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	4.1	7	9.9	4.1	12.1	4.1	11.1	ns
t_{PHL}			3.1	6.4	10.6	3.1	12.5	3.1	11.8	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	3	5.9	9.6	3	11.5	3	10.6	ns
t_{PZL}			3.9	7.4	12.3	3.9	14.7	3.9	13.6	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	5.7	8.2	10.6	5.7	12.3	5.7	11.6	ns
t_{PLZ}			5.4	7.7	10	5.4	11.6	5.4	11	

operating characteristics, $V_{CC} = 5\ V$, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50\ pF$, $\quad f = 1\ MHz$	62	pF

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PARAMETER MEASUREMENT INFORMATION
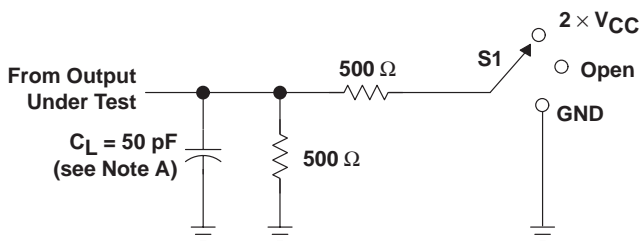
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT
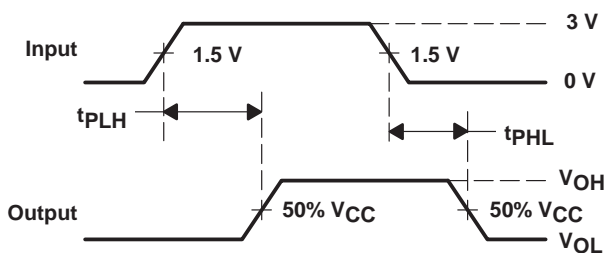
VOLTAGE WAVEFORMS
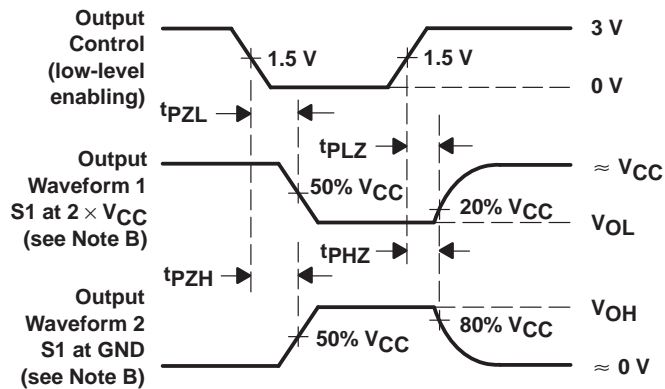
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50\ \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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