Programmable Adaptive Laser Power Controller with Dual Lookup Tables

Preliminary Information[1] *(See Last Page)*

FEATURES AND APPLICATIONS

Features:

- **Integrated Automatic Power Control (APC) circuit**
- **100 mA bias current sink capability**
- **Dual low-current outputs (up to 2.5 mA) based on two independent 256x8 Lookup Table values**
- **Bias current and/or temperature monitoring capability**
- **Dual high/low alert registers**
- **Advanced lookup algorithm eliminates unnecessary output changes**
- **Flexible voltage operation;**
  0 to 5V, 0 to 3.3V, or -5.2V to +3.3V
- **I^2C 2-wire serial bus interface for programming configuration, control values, monitoring, and operational status - 100KHz and 400KHz**
- **Small 5X5 28-Pin QFN Package**

Applications:

- **Laser power management for Telecom/Datacom motherboards**
- **Direct modulation and electro-absorptive modulation applications**

INTRODUCTION

The SML2120 is an advanced, programmable laser diode power controller ideal for optical networking applications. The integrated automatic power control (APC) circuit adapts to variations in the laser's power output as detected by a photo diode.

The SML2120 drives two low current outputs derived from values stored in independent 256x8 Lookup Tables. The low current outputs are suitable for controlling the MODSET input of typical laser driver IC's. The input stimulus for each Lookup Table can be configured as the laser temperature, the bias current, or an external signal. Characteristics of the laser's performance over time and temperature are stored in the lookup tables, allowing the outputs to adapt to system conditions and optimize overall performance.

Programming of configuration and control values by the user are simplified with the I^2C interface adapter (SMX3200) and Windows Programming software available from Summit Microelectronics.

SIMPLIFIED APPLICATION DRAWING

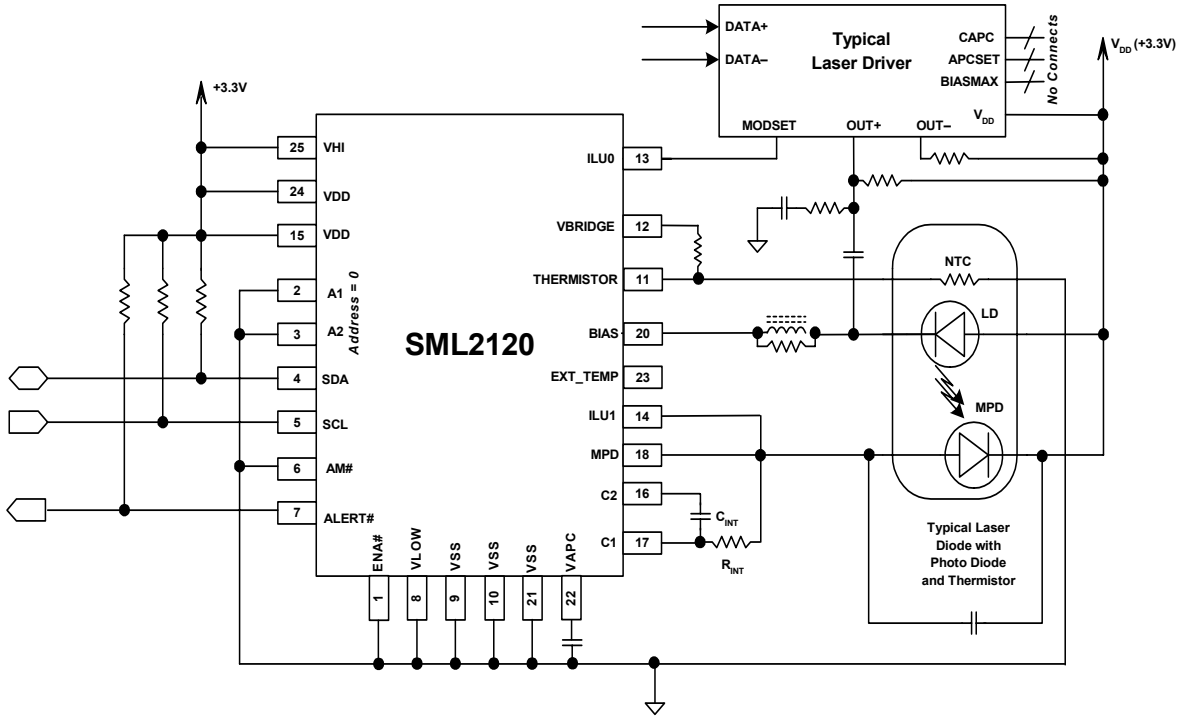


Figure 1. Typical SML2120 Connections to a Laser Driver and Laser Diode

Note: This is an applications example only. Some pins, components and values are not shown.

FUNCTIONAL DESCRIPTION

The SML2120 is an adaptive power controller for laser diodes. The device contains an active feedback loop used to calibrate and control the mean and modulation power of high-speed high-power laser diodes.

Inherent manufacturing tolerances introduce variations of performance in laser diodes. These variations, combined with parametric changes over the laser's extreme operating temperature range and laser aging, require an efficient compensation solution. The SML2120, together with a minimum number of external components, is designed to compensate for these variations using a digital control loop and dual programmable nonvolatile calibration lookup tables.

Figure 2 shows the output light power of a typical laser diode versus its operating current. Depicted in the graph are laser diode characteristics at two different temperatures. At the first temperature (T_{Cold}), the laser requires an average bias current of I_{BIAS1}. The modulation current required to switch the laser between its ON and OFF states is labeled I_{MOD1}.

The ratio of light power of its ON state divided by the light power of its OFF state is referred to as the extinction ratio. Ideally the laser requires a constant extinction ratio over its entire operating temperature range, as the receiver module is calibrated to this level. Operating the laser driver at a higher extinction ratio indicates that power is being wasted, whereas operating at a lower extinction ratio indicates that data may possibly be lost.

The required bias current increases to I_{BIAS2} when the laser is operated at a second temperature (T_{Hot}). The laser requires a modulation of I_{MOD2} to maintain a constant extinction ratio as in the T_{Cold} curve. The SML2120, with its dual lookup table architecture (Figure 3), is capable of providing variable output currents based on a function of either the bias current or the external temperature, and thereby enables the system designer to optimize the extinction ratio of the laser driver module.

The SML2120 eliminates the need for any manual calibration of the laser control circuit. All calibration values are programmed through the I^2C industry-standard 2-wire communication interface whose protocol and functions can be controlled by automated test equipment (ATE).

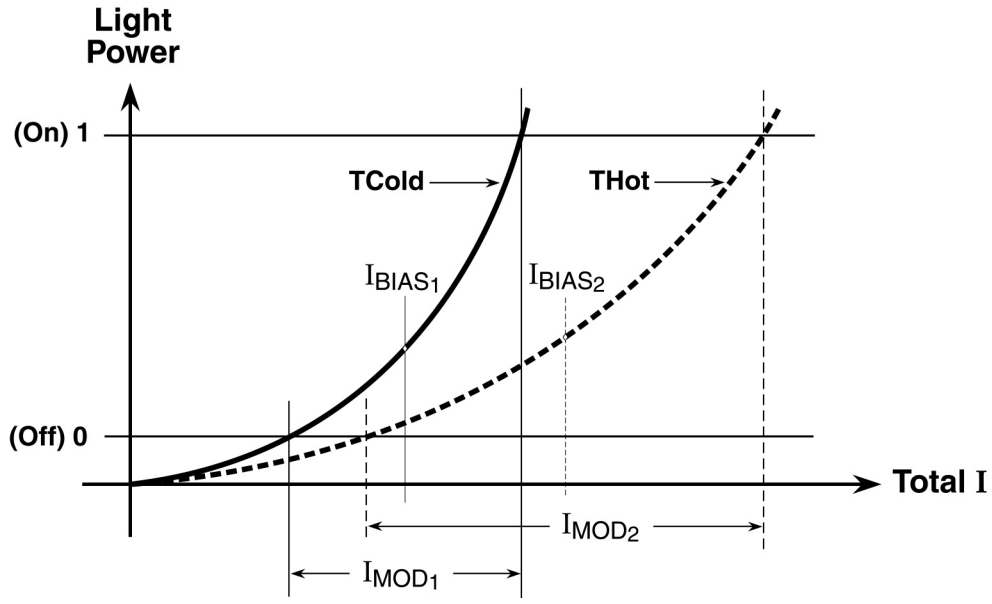


Figure 2. Laser Current Increase Caused by Temperature Increase, Constant Light Power Out

FUNCTIONAL BLOCK DIAGRAM

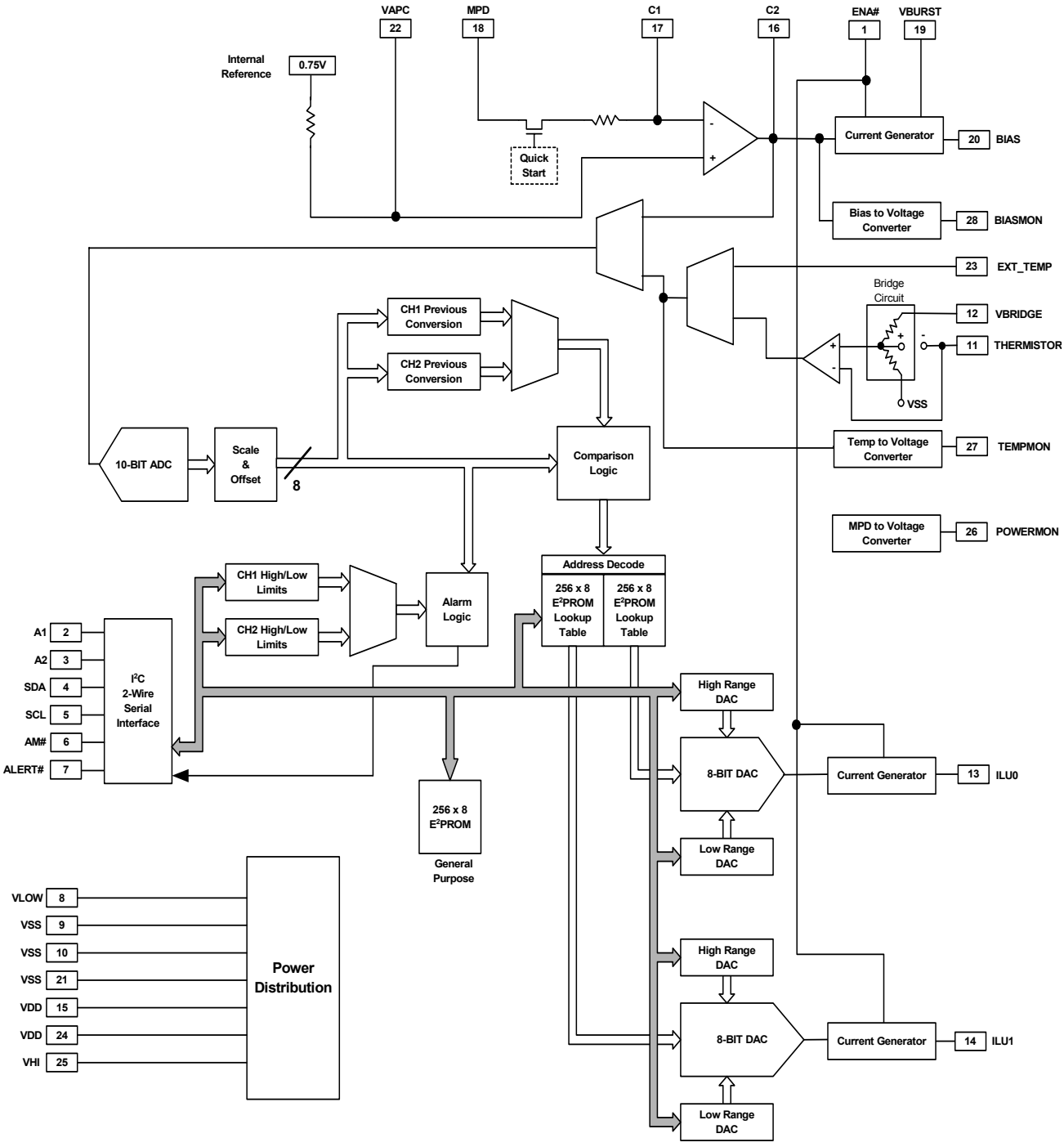


Figure 3. SML2120 Block Diagram

PACKAGE AND PIN DESCRIPTIONS

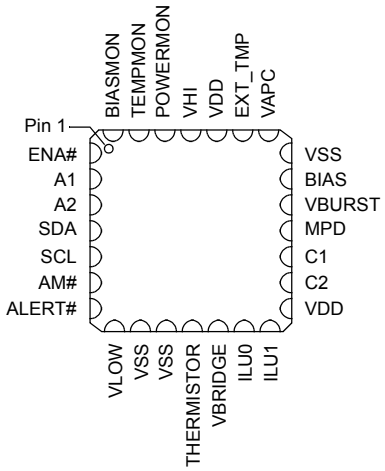


Figure 4. 28-Pin QFN Package Pinout (top view)

PIN DESCRIPTIONS

Pin Number	Pin Type	Pin Name	Description
1	I	ENA#*	Active low input enables the BIAS, ILU0 and ILU1 output currents.
2	I	A1*	The address pins are connected to either the VHI or VLOW pins to provide a mechanism for assigning a unique I^2C bus address to the SML2120.
3	I	A2*	
4	I/O	SDA*	Bi-directional I^2C serial data pin
5	I	SCL*	I^2C serial clock input
6	I	AM#*	AM# is an active low input, when asserted the SML2120 is placed in the Auto-Monitor mode. AM# must be high for programming the Configuration registers and the Lookup Tables, ILU0 and ILU1 and the general purpose E^2PROM.
7	O	ALERT#*	Active low, open-drain output indicates when one of the monitored inputs exceeds its user-programmable high or low alert levels.
8	PWR	VLOW	In dual-rail supply voltage systems, VLOW is tied to the system logic low potential. It is a logic low reference for all pins marked with an asterisk (*).
9	PWR	VSS	VSS must be tied to the lowest system voltage potential.
10	PWR	VSS	
11	I	THERMISTOR	Connect a thermistor to this pin to provide an alternative source of temperature sensing (see VBRIDGE description).
* See VLOW and VHI pin descriptions.			

Pin Number	Pin Type	Pin Name	Description
12	O	VBRIDGE	Connection to an external Full-Bridge Sensor when used with the Thermistor pin. Two of the full-bridge resistors are internal. See the Bridge Circuit Diagram in Figure 1 and 3. Voltage level is 0.2V with respect to VSS.
13	I/O	ILU0	Current output resulting from Lookup Table 0. User-programmable to either sink (to VSS) or source (to VDD) up to 2.5mA.
14	I/O	ILU1	Current output resulting from Lookup Table 1. User-programmable to either sink (to VSS) or source (to VDD) up to 2.5mA.
15	PWR	VDD	VDD is the positive rail for most internal functions.
16	I	C2	Place a capacitor (C_{INT}) between C1 and C2 to increase the time constant for the APC integrator.
17	I	C1	
18	I	MPD	Monitor Photo Diode anode input. Connect a resistor between MPD and C1 to work in conjunction with C_{INT} to establish the integrator time constant.
19	I	VBURST	In burst mode, this input supplies a ballast current that allows the SML2120 to quickly restart when ENA# is asserted.
20	I	BIAS	Supplies the main laser current as controlled by the APC circuit; capable of sinking up to 100mA to VSS.
21	PWR	VSS	VSS must be tied to the lowest system voltage potential.
22	I/O	VAPC	APC Override pin.
23	I	EXT_TEMP	This input can be configured to sense either a voltage or current generated from an external temperature monitoring device.
24	PWR	VDD	VDD is the positive rail for most internal functions.
25	PWR	VHI	In dual-voltage rail systems, VHI is tied to the system logic high potential. It is the logic high reference for all pins marked with an asterisk (*).
26	O	POWERMON*	Analog output voltage indicating the state of the Monitor Photo Diode (MPD) input.
27	O	TEMPMON*	Analog output voltage proportional to the temperature as sensed by the EXT_TEMP or THERMISTOR input.
28	O	BIASMON*	Analog output voltage proportional to BIAS current.
* See VLOW and VHI pin descriptions.			

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... –55°C to 125°C

Power Supply Current (I_{DD}) ..... 115 mA

Storage Temperature ..... –65°C to 150°C

Solder Temperature (10 seconds) ..... 300 °C

Terminal Voltage with Respect to V_{SS}:

All inputs ..... -0.3V to 6.0V

Open Drain Output Short Circuit Current ..... 100 mA

Junction Temperature ..... 150°C

ESD Rating per JEDEC 2000V

Latch-Up testing per JEDEC ..... ± 100mA

RECOMMENDED OPERATING CONDITIONS

Temperature Range (Ambient) ..... -40° C to +85° C

Supply Voltage(V_{DD}) ..... 3.135V to 5.5V

Package Thermal Resistance (θ_{JA}) 28-pin QFN..... 80°C/W

Moisture Classification Level 1 (MSL 1) per J-STD-020

Reliability Characteristics

Data Retention ..... 100 Years

Endurance[1] ..... 100,000 Cycles

Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

DC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to V_{SS}.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	Max bias and modulation current	3.135		5.5	V
I_{DD3}	Power supply current	V_{DD}=3.3V, Bias and Mod open		2	2.5	mA
I_{DD5}	Power supply current	V_{DD}=5.5V, Bias and Mod open		2	5.0	mA
I_{SB3}	Stand-by supply current	V_{DD}=3.3V, ENA#,AM#=V_{IH}			2.0	mA
I_{SB5}	Stand-by supply current	V_{DD}=5.5V, ENA#,AM#=V_{IH}			5.0	mA
I_{LI}	Input leakage current	Vin = 0V to Vdd			1	µA
I_{LO}	Output leakage current	Vout = 0V to Vdd			1	µA
V_{OL}	Output low voltage	I_{OL} = 2 mA			0.4	V
V_{IL}	Input low voltage		-0.1		0.3 x Vdd	V
V_{IH}	Input high voltage		0.7 x Vdd		Vdd	V
Analog Inputs						
V_{MPD}	MPD input active range		0		2	V
I_{EXT_TEMP}	Full Scale Input Current range	Note [1]	0		78.1	µA
V_{EXT_TEMP}	Full Scale Input Voltage range	V_{DD}=3.3V to 5V	0		3.3	V
Analog Outputs						
I_{LUNMAX}	Maximum full-scale sink modulation current	I_{LU0}, I_{LU1}	-2.350		-2.650	mA
I_{LUPMAX}	Maximum full-scale source modulation current	I_{LU0}, I_{LU1}	2.280		2.720	mA
$I_{BIASMAX}$	Maximum full-scale bias current		-90		-110	mA

1. Guaranteed by design.

DC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to V_{SS}.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog Outputs						
V_{APC}	Automatic power control loop default voltage		0.735		0.765	V
V_{POR}	Supply voltage level required to guarantee register readout		2.9			V
V_{BRIDGE}	V_{BRIDGE} output voltage		0.19		0.21	V
$V_{BIASMON}$	BIASMON Full Scale Accuracy (see page 13)	I_{LOAD} = ±10µA	-2		+2	%
$V_{POWERMON}$	POWERMON Full Scale Accuracy (see page 13)		-4		+4	%
$V_{TEMPMON}$	TEMPMON Full Scale Accuracy (see page 13)		-4		+4	%
V_{MONZSO}	BIASMON, POWERMON, TEMPMON Zero Scale Offset				40	mV

AC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to V_{SS}.)

Symbol	Description	Conditions	Min	Typ	Max	Unit
t_{POR}	Power-On-Reset Time	Time when VDD reaches VPOR threshold to when the device is ready			5	ms
$t_{HOLDOFF}$	Holdoff timeout period		-20	$t_{HOLDOFF}$	+20	%
t_{SAMPLE}	Sample Time Interval		-20	t_{SAMPLE}	+20	%

ADC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to V_{SS}.)

Symbol	Description	Conditions	Min	Typ	Max	Unit
N	Resolution	Note [1]	8			Bits
MC	Missing Codes	Minimum resolution for which no missing codes are guaranteed	8			Bits
S/N	Signal to Noise Ratio	Note [1]	50			db
INL	Relative accuracy	EXT_TEMP voltage input; 0 to 3.3V	-1		+1	LSB
DNL	Differential nonlinearity		-1/2		+1/2	LSB

1. Guaranteed by design.

DAC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to V_{SS}.)

Symbol	Description	Conditions	Min	Typ	Max	Unit
8-bit Current DAC Accuracy (When configured to sink current to VSS, V_{ILU}=1V)						
N	Resolution		8			bits
INL	Relative accuracy	Note [1], 10% to 90% of current scale	-3		+3	LSB
		Note [2], 10% to 90% of current scale	-7		+7	LSB
DNL	Differential nonlinearity		-1		+1	LSB
Gain	Positive full scale gain error		-2		+2	%
Offset	Offset error	Note [1]	-4		+4	LSB
		Note [2]	-10		+10	LSB
I_{ZSE}[3]	Zero-scale error current	V_{DD}=5.5V, Note [1]	0		25	µA
		V_{DD}=5.5V, Note [2]	0		50	µA
		V_{DD}=3.135V, Note [2]	0		165	µA
I_{FSE}[3]	Full-scale error current		-150		+150	µA
8-bit Current DAC Accuracy (When configured to source current from VDD, V_{ILU}=1V)						
N	Resolution		8			bits
INL	Relative accuracy	10% to 90% of current scale	-7		+7	LSB
DNL	Differential nonlinearity		-1		+1	LSB
Gain	Positive full scale gain error		-2		+2	%
Offset	Offset error		-12		+12	LSB
I_{ZSE}[3]	Zero-scale error current	V_{DD}=5.5V, Note [1]	-30		0	µA
		V_{DD}=5.5V, Note [2]	-50		0	µA
		V_{DD}=3.135V, Note [2]	165		0	µA
I_{FSE}[3]	Full-scale error current		-220		+220	µA

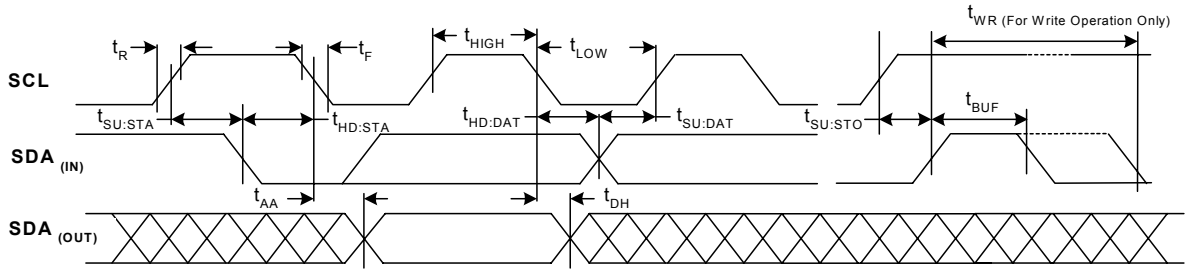
1. Low Range DAC at lowest value; High Range DAC at highest value.
2. Any Combination of DAC settings.
3. I_{ZSE} and I_{FSE} not adjusted for Gain and Offset.

I²C 2-WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to V_{SS}.)

			100kHz			400kHz		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Units**	**Min**	**Max**	**Units**
f_{SCL}	SCL clock frequency		0	100	kHz	0	400	kHz
t_{LOW}	Clock period low		4.7		µs	1.3		µs
t_{HIGH}	Clock period high		4.0		µs	0.6		µs
t_{BUF}	Bus free time[1]	Before new transmission	4.7		µs	1.3		µs
$t_{SU:STA}$	Start condition setup time		4.7		µs	0.6		µs
$t_{HD:STA}$	Start condition hold time		4.0		µs	0.6		µs
$t_{SU:STO}$	Stop condition setup time		4.0		µs	0.6		µs
t_{AA}	Clock edge to valid output	SCL low to valid SDA (cycle n)	0.3	3.5	µs	0.3	0.9	µs
t_{DH}	Data out hold time	SCL low (cycle n+1) to SDA change	0.3		µs	0.3		µs
t_R	SCL and SDA rise time[1]			1000	ns		1000	ns
t_F	SCL and SDA fall time[1]			300	ns		300	ns
$t_{SU:DAT}$	Data in setup time		250		ns	150		ns
$t_{HD:DAT}$	Data in hold time		0		ns	0		ns
t_I	Noise filter SCL and SDA[1]	Noise suppression		100	ns		100	ns
t_{WR}	Write cycle time			10	ms		10	ms

1. Guaranteed by the design.



Basic I²C Timing Diagram

APPLICATIONS INFORMATION

Power-Up Sequence

When power is first applied to the SML2120, the device reads configuration register information from the array and loads it to volatile latches. This procedure begins once the supply voltage exceeds the power-on reset voltage (VPOR) and requires about 3 ms to complete. During this initialization period, all current outputs (BIAS, ILU0, ILU1) are placed into a high impedance state.

At the conclusion of the initialization period, the ENA# pin determines the state of the current output. However, the autonomous monitoring (auto-monitor) function is not yet allowed to activate, regardless of the state of the AM# pin. A holdoff timer period ($t_{HOLDOFF}$) is counted off at the conclusion of the initialization period to allow the laser control loop to stabilize. After $t_{HOLDOFF}$, the AM# pin determines whether the device begins its auto-monitor sequence or not. If AM# is asserted, the device enters auto-monitor mode.

Automatic Power Control (APC) Loop

The SML2120 provides an efficient feedback mechanism for controlling the light output of the laser. Once the power-on initialization period has expired, current to the laser is driven by the BIAS pin, which can sink up to 100 mA of current to Vss. An on-board amplifier controls the bias output circuitry. The Monitor Photo Diode (MPD) pin is driven from the anode of a photo-diode that monitors the light power being given off by the laser. Adding an integration capacitor between C1 and C2, and a corresponding resistor between MPD and C1, completes and stabilizes the loop, as is shown in Figure 5.

The APC loop attempts to drive the C1 node to the internal VAPC voltage reference of 0.75V. If the voltage on the MPD pin exceeds VAPC, the SML2120 reduces the amount of current on the BIAS pin accordingly, thereby reducing the amount of current to the laser. Conversely, if the voltage on MPD falls below VAPC, the amount of current supplied to the laser is increased. Note that the VAPC pin may be over-driven using an external reference if a different steady state value is desired.

The integration time constant of the APC loop is typically set to a relatively long period (such as 1ms) in order to reduce pattern dependent jitter. Unfortunately, a long time constant also leads to a long start-up time. The SML2120 provides an internal 'Quick Start' transistor, shown in Figure 5, that can be used to accelerate the turn-on time of the laser. When this feature is enabled, the Quick Start transistor effectively shorts out the external resistor for a brief time period after the outputs are first enabled.

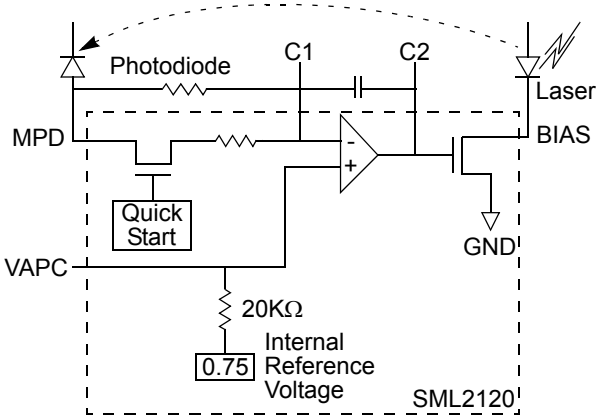


Figure 5. Bias Control Circuit

Bias Output

The user may limit the maximum BIAS current in increments of 12.5mA (up to a maximum of 100mA), using register 14 bits 2:0. This feature is useful in preventing damage to the laser even during start-up or open-loop conditions.

Additionally, the BIAS output may be configured to provide a fixed current. The value of current is based on the ILU1 output and scales proportionally. This fixed bias current may be configured so that it is available at power-up only, or whenever ENA# is disabled. This feature is useful in systems without a monitor diode, or in systems where feed-forward current is desired. A fixed current is also useful for providing reasonable BIAS when no data is yet flowing, and for diagnostics and board debugging.

Autonomous Monitoring Function (Auto-Monitor)

The Autonomous Monitoring (Auto-Monitor) Function provides a control loop for setting two independent output currents (ILU0 and ILU1) based on various programmable input stimuli within the system. For each channel, the user selects: 1) an input stimulus for the Analog/Digital Converter (ADC), 2) scale and offset values for the conversion to maximize the usable input range, 3) lookup table values that translate the resulting ADC conversion to an output current, and 4) minimum and maximum limits for the output current driver. Refer to Figure 6.

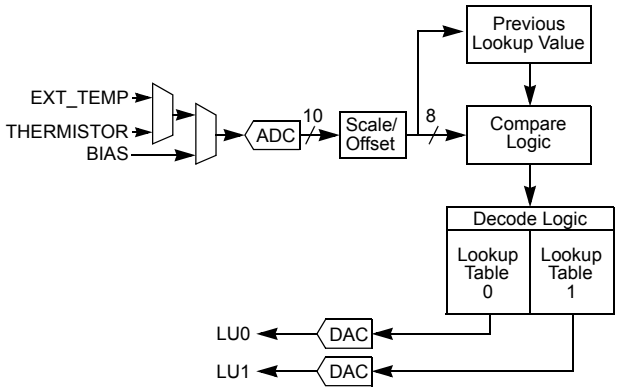


Figure 6. Simplified Autonomous Monitoring Diagram

The Lookup (translation) Table (LUT) values are generally loaded once during test and calibration using ATE equipment. More sophisticated systems may periodically take the system off-line, take some measurements, and update the table throughout the life of the laser module. Well characterized phenomenon may be ordered from Summit Microelectronics with table values pre-programmed. One advantage of a LUT is that arbitrary, or nth-order, functions may be easily mapped. Also, table values may be tweaked late in the design stage to improve or modify performance characteristics.

As the name implies, the Auto-Monitor function requires no input from external controllers or processors. This function may be initiated by pulling the AM# pin low, or by addressing the SML2120 through the Status Register. On power-up, a holdoff timer prevents the auto-monitor function from commencing until the system has had time to stabilize. When the current outputs are disabled (by pulling ENA# high), the auto-monitor function is internally suspended until the outputs are once again enabled.

Analog-to-Digital Converter (ADC)

The internal analog-to-digital converter can be configured to measure various critical system parameters, which allows the SML2120 to dynamically react to changes in its operating environment. There are four different inputs that may be multiplexed to the ADC: bias current, thermistor voltage, external voltage or external current. The external voltage or current is sensed via the EXT_TEMP pin. The input range for each of the different inputs is shown in Table 1.

Table 1. Channel Configuration and Full Scale Value

CFG 6/7, Bits [6:5]	Input Stimulus	Nominal ADC Input Range
00	Thermistor	.1V - .2V
01	EXT_TEMP Voltage	0 - 3.3V
10	EXT_TEMP Current	0 - 78.125uA
11	Bias Current	0 - BIAS MAX

Each LUT is configured to be associated with any one of the four ADC inputs. The only restriction is that you may not associate one LUT to the EXT_TEMP voltage and the other LUT to EXT_TEMP current. The EXT_TEMP pin is configured to accept only one or the other.

In addition to selecting the ADC input source for each LUT, the user must also select a scale value (1x, 2x, 4x or 8x) and offset value (0 through 7 eighths of full scale) for each LUT. The purpose of the scale and offset selection is to maximize the resolution of the ADC output. In order to maintain accuracy while using scale values greater than 1x, a 10-bit ADC has been employed, even though only eight bits are used.

The following example illustrates the use of scale and offset to achieve the maximum resolution out of the ADC. Configure one LUT to be driven from the laser bias current. The laser manufacturer specs a maximum current of 90mA; the laser module has a useful bias current range that spans from a minimum of 46mA to a maximum of 83mA.

First, configure the maximum bias current to 100mA*7/8 = 87.5mA to protect the laser. Determine the proper scale factor by taking the full scale current (87.5mA) and divide by the target input range (83mA - 46mA = 37mA) and round down to the nearest scale value (87.5mA / 37mA = 2.36 -> 2x). The offset is determined by finding the highest offset value that is less than the minimum input value (46mA). Offset values are integer multiples of 1/8 of the full scale amount (87.5mA). In this example choose an offset of 43.75mA (= 4*87.5mA / 8).

By using the values for scale and offset in this example, a zero reading out of the ADC corresponds to a bias current of 43.75mA (or less), and a full scale reading (0FFh) out of the ADC corresponds to a bias current of 87.5mA (or greater).

Thermistor Interface

The SML2120 has circuits built-in to help facilitate using a thermistor to measure laser temperature. The VBRIDGE pin provides a .2V output reference to drive half of a bridge circuit that includes the thermistor and one other external resistor. The other half of the bridge is internal to the device. The external components are placed between the VBRIDGE, THERMISTOR, and VSS pins as shown in Figure 3.

Programmable Current Outputs

There are two fully independent, programmable current outputs on the SML2120: ILU0 and ILU1. The output polarity (source or sink current), as well as the upper and lower current limit may be individually programmed to meet varying output requirements. The upper and lower limits for each channel may be set between 0 and 2.5 mA in 256 steps. These limits can help prevent damage to components receiving the output current, and they increase resolution in the desired operating range. The final output current is determined by an 8-bit DAC that ranges between the upper and lower current limits (refer to Figure 7). A power-up register determines the initial DAC setting; during Auto-Monitor operation, data read out of the array is loaded into the DAC register to determine the output current.

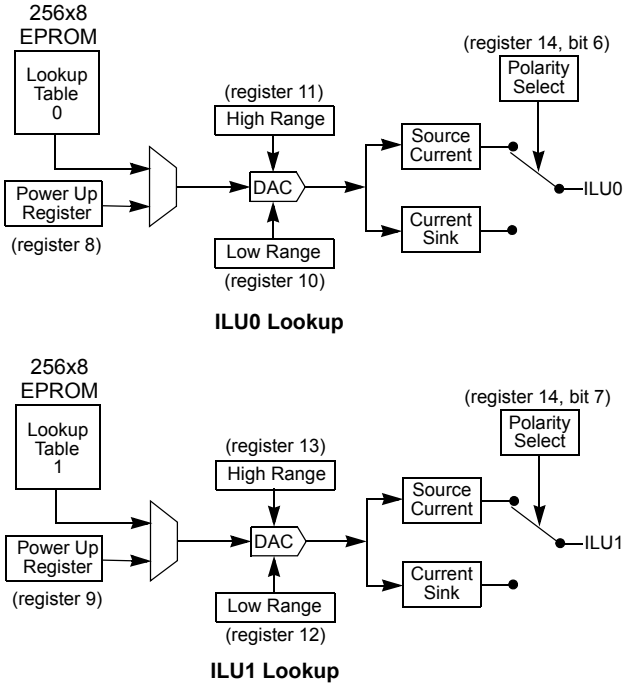


Figure 7. Independent Lookup Tables

Burst Mode

The SML2120 is designed to work in applications that require burst mode operation. The output currents (ILU0, ILU1 and BIAS) may be switched on and off by using the ENA# pin. In applications that require very high speed operation, the VBURST pin may be used as a ballast load for the BIAS current. When ENA# is de-asserted, all current that was flowing through the BIAS output is diverted to the VBURST pin. For optimal performance, the load attached to VBURST should closely resemble the load of the laser in order to keep internal nodes biased at the correct levels. Additionally, the ENA# pin should be configured for "FAST MODE" by setting Config Reg 15, Bit 7 high. This setting increases the throughput of the enabling signal by eliminating noise filters on the input; this setting also eliminates the VHIGH/VLOW level shifter. Thus, when using the ENA# pin in FAST MODE, the input levels need to range between VDD and VSS, rather than VHIGH and VLOW. (Applicable only in dual voltage systems.)

E^2PROM

The SML2120 contains 6k bits of user-accessible E^2PROM memory. Each LUT is comprised of 2k bits arranged as 256 words by 8 bits. LUT0 occupies addresses 000h - 0FFh and LUT1 occupies addresses 100h - 1FFh, both using the I^2C slave address of 1011. A third 2k block of E^2PROM is available to the user as a general-purpose memory. This block is accessed via slave address 1010, memory addresses 000h - 0FFh.

Device configuration information is stored in 16 non-volatile registers located at addresses 100h - 10Fh, also under the slave address 1010. Note that the user may program the device to prevent any further writes to this configuration space.

Refer to the "Configuration Register Description" section below for details of the available configuration settings. Refer to "I^2C Interface" section for further details and examples of communicating with the SML2120 over the I^2C bus.

Status Register

The Status register is a volatile register that allows the user to control and receive feedback from the device, accessible using the 1001 slave address at memory address 00Fh. Table 2 describes the status byte:

Table 2. Status Register

Slave Address 1001, Word Address 00Fh		
Bit	**I/O**	**Description**
7	Output	Alert Channel
6	Output	Alert Limit (Hi/Low)
5:4	-	Unused
3	I/O	Alert
2	I/O	Auto-Monitor
1	I/O	Output Enable
0	I/O	Write Protect

Bits 7 and 6 are read-only bits that indicate the offending channel and limit, respectively, during an alert condition. Bits 3:0 are I/O's that indicate the status of the device when read out, and affect operation of the device when written to. Bit 3 represents the state of the ALERT# output; when this bit is high, the ALERT# output is asserted. Writing a zero to this bit will de-assert the ALERT# output. Bits 2 and 1 represent the state of the Auto-Monitor and Output Enable functions, respectively. On power-up, these functions are controlled by the appropriate pin, AM# or ENA#; however, the state of either pin may be overridden by writing to the selected bit of the status register. Bit 0 controls the write protect status of the device; no data may be changed until this bit is cleared.

Dual Voltage Operation

The SML2120 was designed to operate with a single-ended supply (i.e. 3.3V or 5V), or in a dual voltage environment of –5.2V, 0V, and +3.3V. It is common for many lasers to be driven off the –5.2V rail, while the interface runs on the positive supply. The SML2120 runs entirely between VDD and VSS, with the exception of the digital interface pins (pins 1-6) and three analog monitor pins (26-28), which are driven between VHI and VLOW. Table 3 details the different modes of operation. In all cases, current outputs are sourced from VDD and sink to VSS.

Table 3. Voltage Supply Modes

Pin	Single Supply	Single Supply	Dual Supply
VDD	3.0V to 3.6V	4.5V to 5.5V	0V
VSS	0V	0V	-5.5V to -4.9V
VHI	3.0V to 3.6V	4.5V to 5.5V	3.0V to 3.6V
VLOW	0V	0V	0V
Digital Interface	0V TO 3.6v	0V TO 5.5V	0V to 3.6V

Analog Monitor Outputs

There are three analog monitor outputs on the SML2120 that provide a continuous measure of the critical parameters in the system. The POWERMON output reflects the state of the APC loop, which is an indirect measure of the laser power output. The TEMPMON output has different characteristics depending on which input has been selected as the temperature pin. If the ADC input for either LUT0 or LUT1 is selected to be from the THERMISTOR pin, then the TEMPMON output is a level-shifted and amplified version of the THERMISTOR input. Otherwise, the TEMPMON output is generated based on the voltage on the EXT_TEMP pin. The BIASMON output indicates the instantaneous bias current. All three of these outputs are level-shifted up to the VHIGH/VLOW rail as described by the following equations:

$V_{POWERMON} - V_{LOW} = (V_{C1} - V_{SS})$

$V_{TEMPMON} - V_{LOW} = (V_{EXT\_TEMP} - V_{SS})$ or
$25 * ((V_{THERMISTOR} - V_{SS}) - 0.1)$

$V_{BIASMON} - V_{LOW} = 2 * I_{BIAS}/I_{BIASMAX}$

Serial Interface

The SML2120 uses the industry standard I^2C, 2-wire serial interface. This interface provides access to the status registers, ADC, general purpose E^2PROM, configuration registers and LUT tables according to Table 4. Associated with the interface are two address pins (A2 and A1), which allow up to four devices on the same bus.

Table 4. SML2120 Access Types

Slave Address	A0 (Address bit 8)	Access Type
1001	0	Read/Write Status registers
	1	Read A/D converter
1010	0	General Purpose E^2PROM
	1	Configuration registers
1011	0	Read/Write Lookup Table 0
	1	Read/Write Lookup Table 1

Device configuration and access is simplified using the SML2120 graphical user interface (GUI) software available from the Summit website (www.summitmicro.com). This software utilizes a programming dongle (SMX3200) connected to the parallel port of a PC to read and write the device.Compatible Laser Drivers

Compatible Laser Drivers

The SML2120 is compatible with a wide array of laser drivers from many different manufacturers. The SML2120 controls the power, biasing and modulation current independent of the data rate of the laser driver. Therefore, it can be applied with drivers that operate at sub-GHz, 2.5GHz, 10GHz and 40GHz rates. An example application for an electro-absorptive modulated laser is shown in Figure 8. The SML2120 interfaces to the laser module thermistor, monitor diode and laser diode to control bias and modulation levels over temperature.

Another application example is shown in Figure 9. Here, the SML2120 is shown controlling a laser diode and an external thermistor. The thermistor output is monitored and also buffered to drive the external temperature pin which is connected to one of the LUTs on the SML2120. Also shown are the optional connections for dual supply operation and connections to the SMX3200 programmer header.

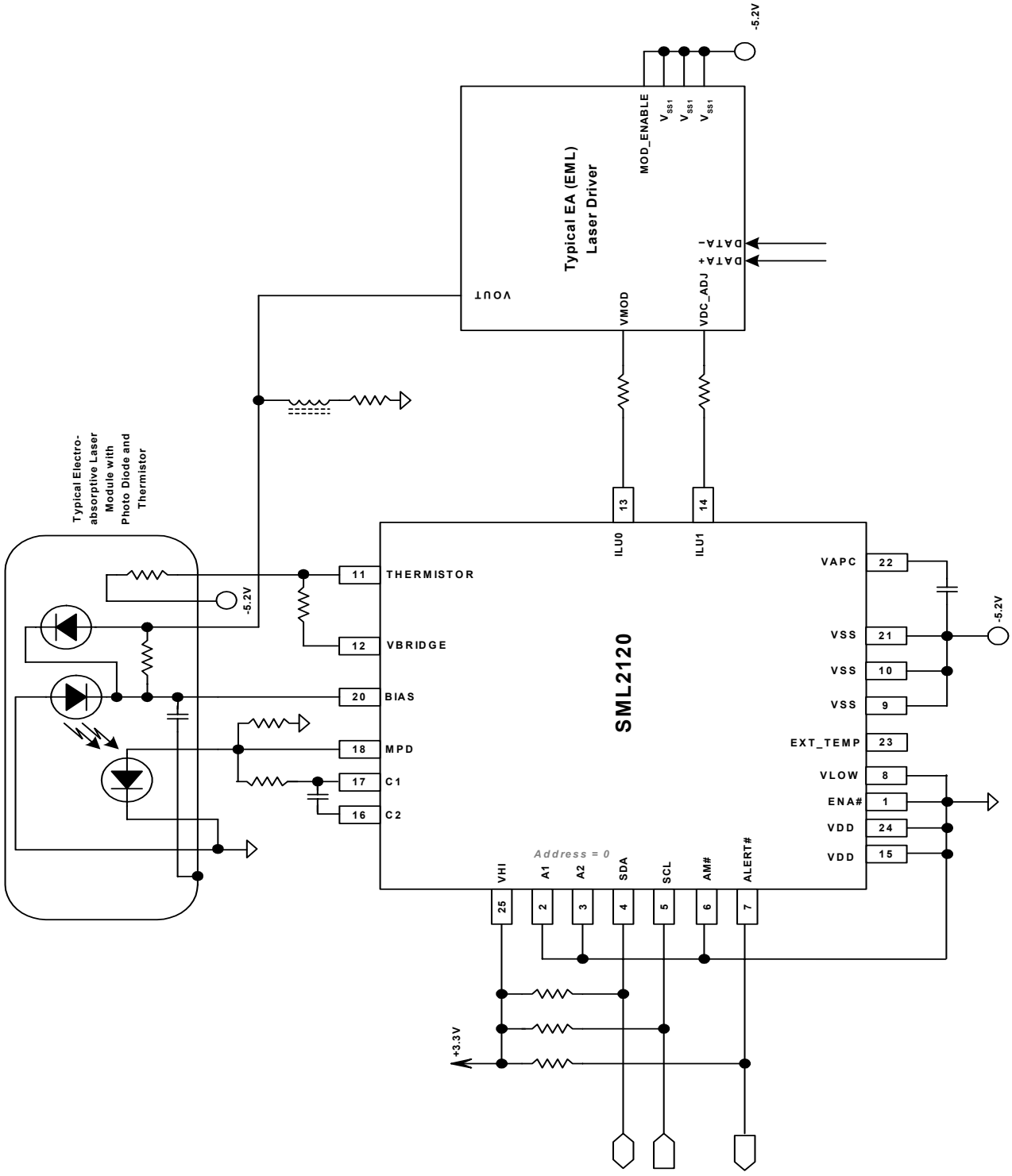


Figure 8. Typical Electro-Absorptive Modulated Laser Application (-5.2V Supply)

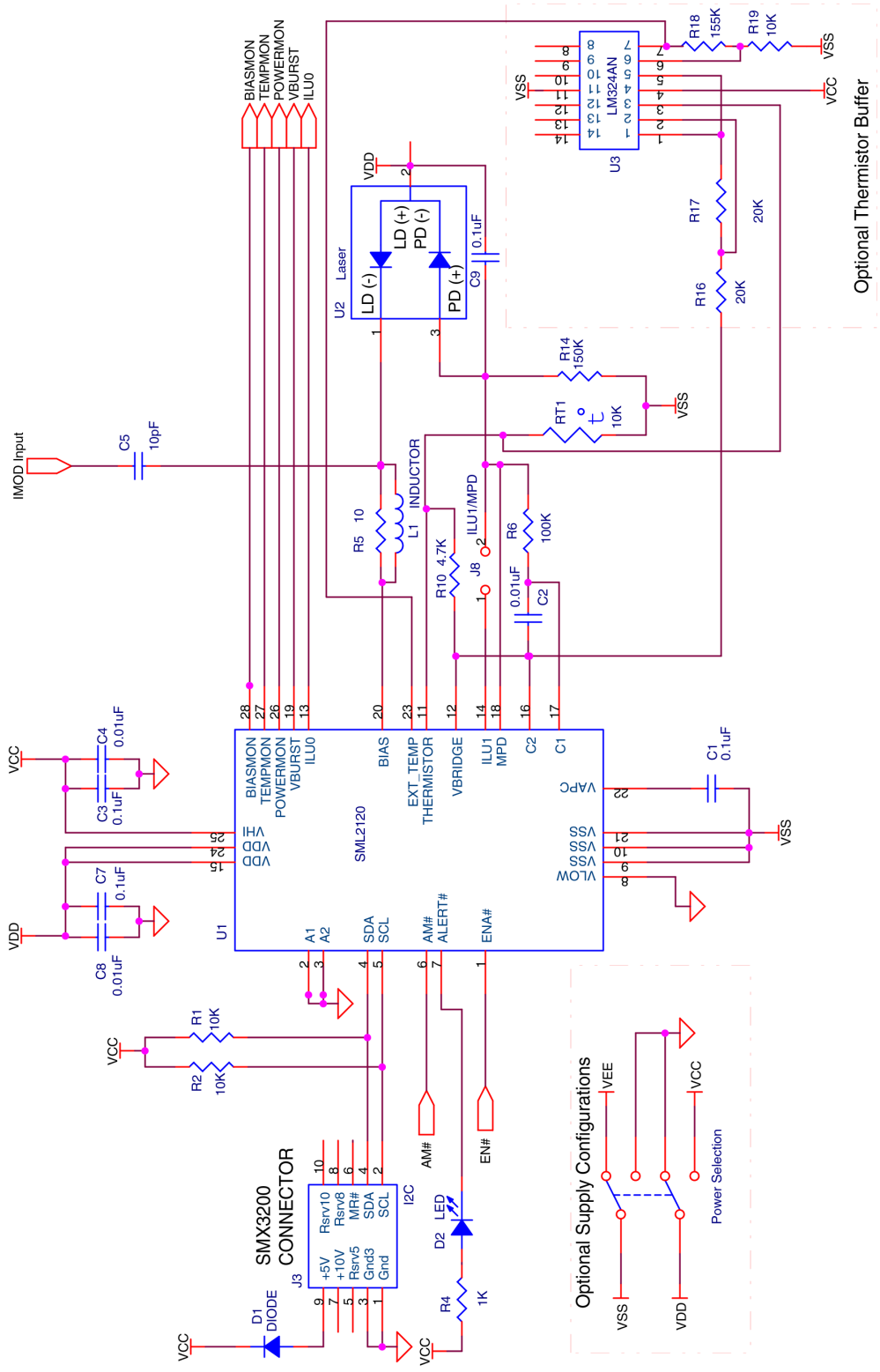


Figure 9. Typical laser applications schematic showing programming and dual supply connection options.

DEVELOPMENT HARDWARE & SUPPORT

The end user can obtain the Summit SMX3200 programming system for device prototype development. The SMX3200 system consists of a programming Dongle, cable and Windows GUI software. It can be ordered on the website or from a local representative. The latest revisions of all software and an application brief describing the SMX3200 is available from the website (www.summitmicro.com).

The SMX3200 programming Dongle/cable interfaces directly between a PC's parallel port and the target application. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus.

The Windows GUI software will generate the data and send it in I^2C serial bus format so that it can be directly downloaded to the SML2120 via the programming Dongle and cable. An example of the connection interface is shown in Figure 10.

When design prototyping is complete, the software can generate a HEX data file that should then be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

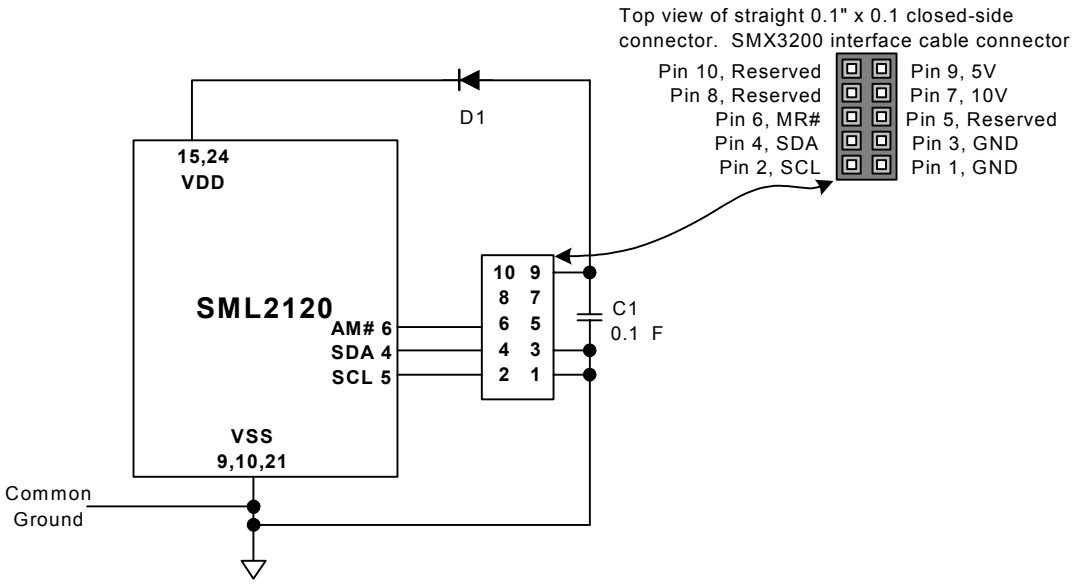


Figure 10. SMX3200 Programmer and I^2C serial bus connections to program the SML2120. For the SML2120, the AM# pin must be high in order to program the device. Normally, SDA and SCL signals require on board pull-up resistors, however, the SMX3200 has internal pull-up resistors. D1 is needed between the Dongle Supply and the VDD pin so that there will be no contention between the two supplies. C1 is for noise bypassing. Note, AM# must be high for programming, it can be pulled high externally or by the SMX3200 programmer. AM# must be low for auto-monitor mode operation.

I²C INTERFACE

The I2C bus is a standard two-wire serial communication interface used between different integrated circuits. The two lines are serial data (SDA), which is a bi-directional pin, and serial clock (SCL). The SML2120 supports a 100kHz and 400kHz clock rate.

The SDA line must be connected to a positive supply by a pull-up resistor located on the bus. The SML2120 contains a Schmitt input on both the SDA and SCL signals.

When the slave address is 1001 and address bit 8 is low, the Status register is accessed. When bit 8 is high, the A/D converter is read. The channel read from the ADC is determined by the word address (see Figure 18).

When the slave address is 1010 and address bit 8 is low, the General Purpose E^2PROM is accessed. When bit 8 is high, the Configuration registers are accessed.

When the slave address is 1011, address bit 8 determines whether Lookup Table 0 or 1 is accessed. If bit 8 is '0', Lookup Table 0 is accessed. A '1' accesses Lookup Table 1. See Figure 23 and 24.

Start and Stop Conditions

Both the SDA and SCL pins remain high when the bus is not busy. Data transfers between devices may be initiated with a Start condition only when SCL and SDA are high. A high-to-low transition of the SDA while the SCL pin is high is defined as a Start condition. A low-to-high transition SDA while SCL is high is defined as a Stop condition. Figure 11 shows a timing diagram of the start and stop conditions.

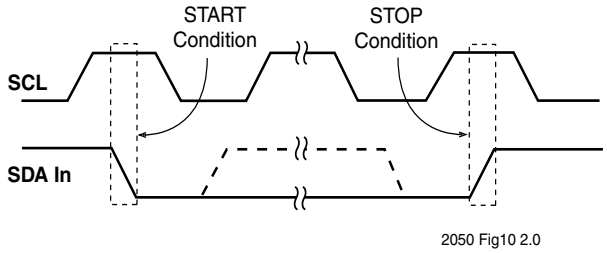


Figure 11. Start and Stop Conditions

Master/Slave Protocol

The master/slave protocol defines any device that sends data onto the bus as a transmitter, and any device that receives data as a receiver. The device controlling data transmission is called the Master, and the controlled device is called the Slave. In all cases the SML2120 is referred to as a Slave device since it never initiates any data transfers.

Acknowledge

Data is always transferred in bytes. Acknowledge (ACK) is used to indicate a successful data transfer. The transmitting device releases the bus after transmitting eight bits. During the ninth clock cycle the Receiver pulls the SDA line low to acknowledge that it received the eight bits of data. This is shown by the ACK callout in Figure 12.

When the last byte has been transferred to the Master during a read of the SML2120, the Master leaves SDA high for a Not Acknowledge (NACK) cycle. This causes the SML2120 part to stop sending data, and the Master issues a Stop on the clock pulse following the NACK.

Figure 12 shows the Acknowledge timing.

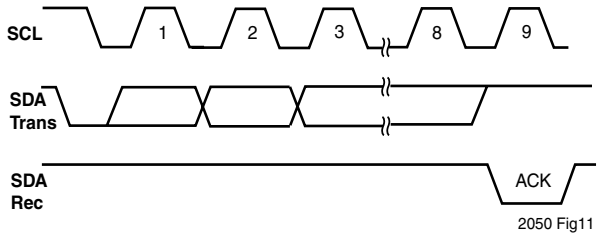


Figure 12. Acknowledge Timing

Read and Write

The first byte from a Master is always made up of a 7-bit Slave address and the Read/Write (R/W) bit. The R/W bit tells the Slave whether the Master is reading data from the bus or writing data to the bus (1 = Read, 0 = Write). The first four of the seven address bits are called the Device Type Identifier (DTI). The DTI for the SML2120 is 1010_{BIN}.

The next three bits are Address values for A2, A1, and A0 (if multiple devices are used). In the SML2120, A0 functions as address bit 8. Refer to Table 4 for more information on the state of address bit 8 and the access types supported.

The SML2120 issues an Acknowledge after recognizing a Start condition. Figure 13 shows an example of a typical master address byte transmission.

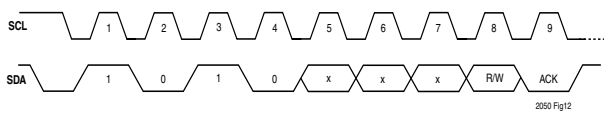


Figure 13. Typical Master Address Byte Transmission

During a read by the Master device, the SML2120 transmits eight bits of data, then releases the SDA line, and monitors the line for an Acknowledge signal. If an Acknowledge is detected, and no Stop condition is generated by the Master, the SML2120 continues to transmit data. If an Acknowledge is not detected (NACK), the SML2120 terminates any subsequent data transmission. The read transfer protocol on SDA is shown in Figure 14.

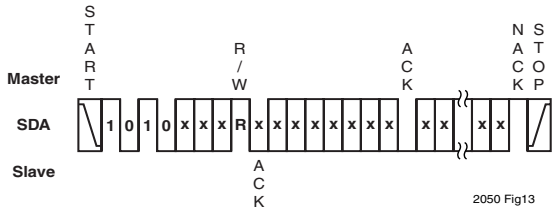


Figure 14. Read Protocol

During a Master write, the SML2120 receives eight bits of data, then generates an Acknowledge signal. It device continues to generate the ACK condition on SDA until a Stop condition is generated by the Master. The write transfer protocol on SDA is shown in Figure 15.

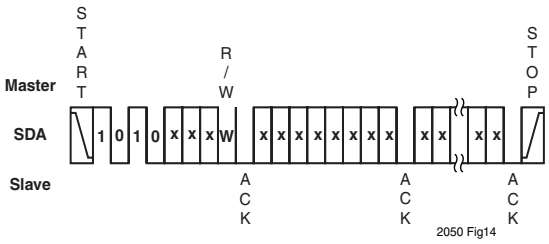


Figure 15. Write Protocol

Random Access Read

Random address read operations allow the Master to access any memory location in a random fashion. This operation involves a two-step process. First, the Master issues a Write command which includes the Start condition and the Slave address field (with the R/W bit set to Write) followed by the address of the word it is to read. This procedure sets the internal address counter of the SML2120 to the desired address.

After the word address Acknowledge is received by the Master, it immediately reissues a Start condition followed by another Slave address field with the R/W bit set to Read. The SML2120 responds with an Acknowledge and then transmits the 8 data bits stored at the addressed location. At this point, the Master sets the SDA line to NACK and generates a Stop condition. The SML2120 discontinues data transmission and reverts to its standby power mode.

Sequential Reads

Sequential reads can be initiated as either a current address read or a random access read. The first word is transmitted as with the other byte Read modes (current address byte Read or random address byte Read). However, the Master now responds with an Acknowledge, indicating that it requires additional data from the SML2120.

The SML2120 continues to output data for each Acknowledge received. The Master sets the SDA line to NACK and generates a Stop condition. During a sequential Read operation the internal address counter is automatically incremented with each Acknowledge signal.

For Read operations all address bits are incremented, allowing the entire array to be read using a single Read command. After a count of the last memory address the address counter rolls over and the memory continues to output data.

Transaction Types

The figures below show timing diagrams for the following transaction types.

- Status Register Read
- Status Register Write
- ADC Read
- Configuration E^2PROM Read
- Configuration E^2PROM Write
- General Purpose E^2PROM Read
- General Purpose E^2PROM Write
- Lookup Table Read
- Lookup Table Write

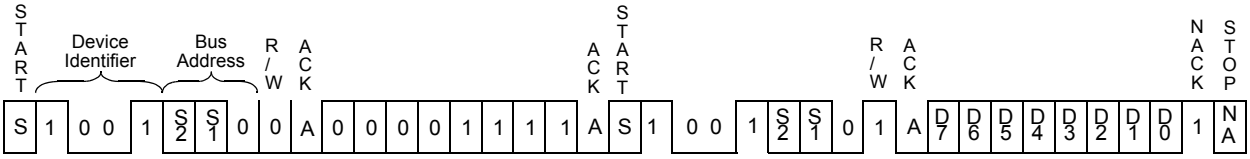


Figure 16. Status Register Read

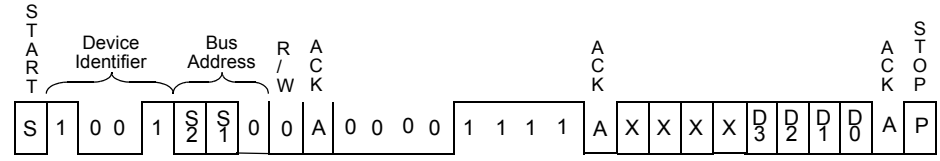


Figure 17. Status Register Write

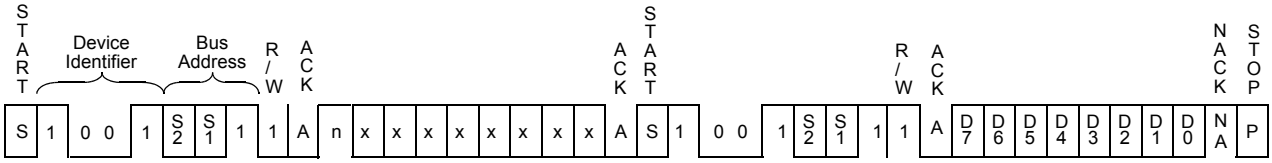


Figure 18. ADC Read

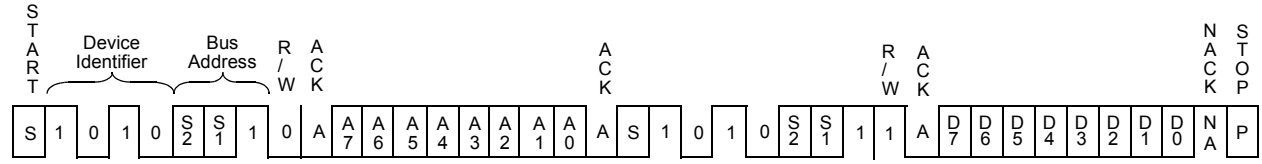


Figure 19. Configuration E^{2}PROM Read

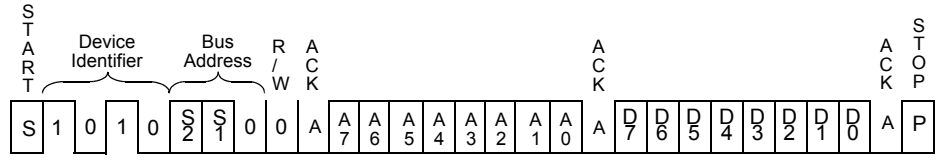
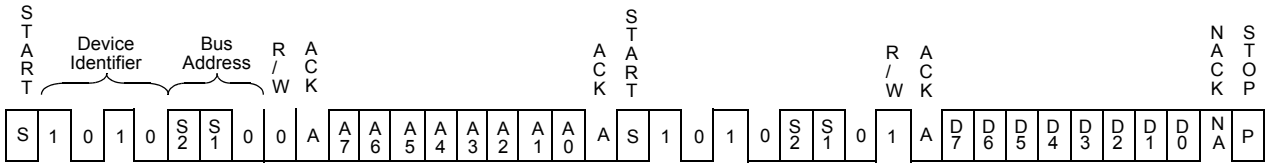
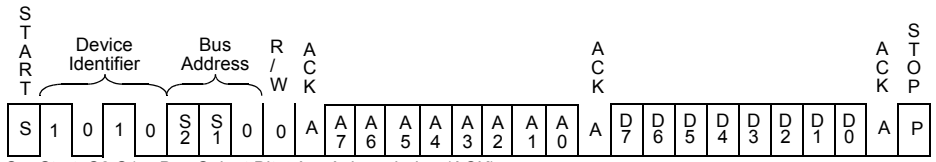


Figure 20. Configuration E^{2}PROM Write



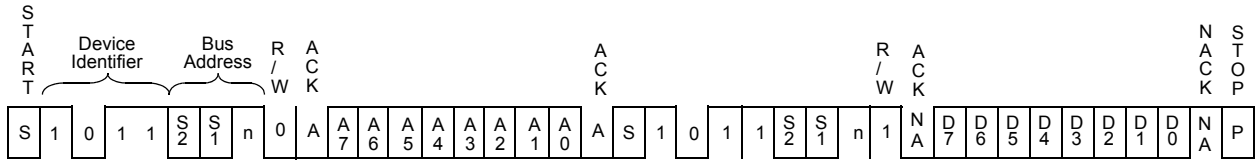
S = Start, S2:S1 = Bus Select Bits, A = Acknowledge (ACK)
NA = No Acknowledge (NACK), P = Stop, n = Lookup Table (LUT) 0 or 1

Figure 21. General Purpose E^{2}PROM Read



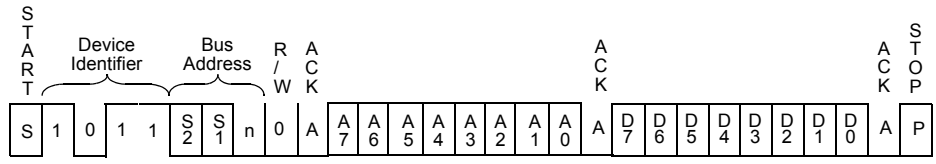
S = Start, S2:S1 = Bus Select Bits, A = Acknowledge (ACK)
NA = No Acknowledge (NACK), P = Stop, n = Lookup Table (LUT) 0 or 1

Figure 22. General Purpose E^{2}PROM Write



S = Start, S2:S1 = Bus Select Bits, A = Acknowledge (ACK)
NA = No Acknowledge (NACK), P = Stop, n = Lookup Table (LUT) 0 or 1

Figure 23. Lookup Table Read



S = Start, S2:S1 = Bus Select Bits, A = Acknowledge (ACK)
NA = No Acknowledge (NACK), P = Stop, n = Lookup Table (LUT) 0 or 1

Figure 24. Lookup Table Write

CONFIGURATION REGISTERS

The SML2120 has sixteen 8-bit user programmable, nonvolatile, configuration registers. Table 5 shows a listing of the configuration registers and the correspond decimal and hexadecimal addresses.

Table 5. Configuration Register Map

Decimal Address	Hexadecimal Address	Register Name	Contents	Default
256	0x100	Configuration Register 0	Low alarm value for Lookup Table 0.	00
257	0x101	Configuration Register 1	High alarm value for Lookup Table 0.	FF
258	0x102	Configuration Register 2	Low alarm value for Lookup Table 1.	00
259	0x103	Configuration Register 3	High alarm value for Lookup Table 1.	FF
260	0x104	Configuration Register 4	Minimum Update Delta, LU tables 0 and 1.	00
261	0x105	Configuration Register 5	Conversion Count, Alarm Count, AUTOMOM hold off timer.	00
262	0x106	Configuration Register 6	ADC input, scale, and offset for LU table 0.	60
263	0x107	Configuration Register 7	ADC input, scale, and offset for LU table 1.	00
264	0x108	Configuration Register 8	Power-up DAC settings for LU table 0.	00
265	0x109	Configuration Register 9	Power-up DAC settings for LU table 1.	00
266	0x10A	Configuration Register 10	Low DAC value, LU table 0.	00
267	0x10B	Configuration Register 11	High DAC value, LU table 0.	00
268	0x10C	Configuration Register 12	Low DAC value, LU table 1.	00
269	0x10D	Configuration Register 13	High DAC value, LU table 1.	00
270	0x10E	Configuration Register 14	Output polarity, Bias current, Quick Start	00
271	0x10F	Configuration Register 15	Fast Mode enable, alarm reset, configuration lockout, write protection.	03

Configuration Register 0 - Address 0x100

This register is used to set the low alarm value for Lookup Table 0. An ADC conversion on Lookup Table 0 that is less than the value programmed in this register causes the ALERT# pin to be asserted.

Bits								Default	Description
7	6	5	4	3	2	1	0		
Low Alarm								0x00	Low alarm value for Lookup Table 0. Values range from 0 to 255.

Table 6. Configuration Register 0 Bitmap

Configuration Register 1 - Address 0x101

This register is used to set the high alarm value for Lookup Table 0. An ADC conversion on Lookup Table 0 that is greater than the value programmed in this register causes the ALERT# pin to be asserted.

Bits								Default	Description
7	6	5	4	3	2	1	0		
High Alarm								0xFF	High alarm value for Lookup Table 0. Values range from 0 to 255.

Table 7. Configuration Register 1 Bitmap

Configuration Register 2 - Address 0x102

This register is used to set the low alarm value for Lookup Table 1. An ADC conversion on Lookup Table 1 that is less than the value programmed in this register causes the ALERT# pin to be asserted.

Bits								Default	Description
7	6	5	4	3	2	1	0		
Low Alarm								0x00	Low alarm value for Lookup Table 1. Values range from 0 to 255.

Table 8. Configuration Register 2 Bitmap

Configuration Register 3 - Address 0x103

This register is used to set the high alarm value for Lookup Table 1. An ADC conversion on Lookup Table 1 that is greater than the value programmed in this register causes the ALERT# pin to be asserted.

Bits								Default	Description
7	6	5	4	3	2	1	0		
High Alarm								0xFF	High alarm value for Lookup Table 1. Values range from 0 to 255.

Table 9. Configuration Register 3 Bitmap

Configuration Register 4 - Address 0x104

This register is used to set the minimum update delta for Lookup Tables 0 and 1. The contents of this register are used when the lookup table address translation by the ADC is compared against the previous value. The current value must differ from the previous stored value by the amount in this register in order for the translation to occur.

Bits								Default	Description
7	6	5	4	3	2	1	0		
Delta 1				x				0x0	Bits 7:4 determine the minimum update delta for Lookup Table 1. Valid values range from 0 to 15. 0000 = 0, 1111 = 15.
x				Delta 0				0x0	Bits 3:0 determine the minimum update delta for Lookup Table 0. Valid values range from 0 to 15. 0000 = 0, 1111 = 15.

Table 10. Configuration Register 4 Bitmap

Configuration Register 5 - Address 0x105

This register is used to set the consecutive count source for Lookup Table 0 and 1, the alarm count, the auto-monitor (AM#) lockout, and auto-monitor hold-off timer.

Bits								Default	Description
7	6	5	4	3	2	1	0		
COUNT 1								0b00	Indicates the minimum delta between addresses for Lookup table 1. 00 = 0, 11 = 3. Note that there must be at least COUNT1 consecutive conversions that differ from the previously stored conversion by at least DELTA 1 (bits 7:4 of Configuration register 4) in order for a new translation to occur.
		COUNT 0						0b00	Indicates the minimum delta between addresses for Lookup table 0. 0b00 = 0, 0b11 = 3. Note that there must be at least COUNT0 consecutive conversions that differ from the previously stored conversion by at least Delta 0 (bits 3:0 of Configuration register 4) in order for a new translation to occur.
				0				0b0	ALERT# pin assertion. When this bit is cleared, the ALERT# pin is asserted by the SML2120 on the first alert event.
				1					ALERT# pin assertion. When this bit is set, the ALERT# pin is asserted by the SML2120 on consecutive alert events.
					0			0b1	Assertion of the AM# pin by external logic does lock out interface.
					1				Assertion of the AM# pin by external logic does NOT lock out interface.
						0	0	0b0	0.4 ms delay for auto-monitor holdoff timer.
						0	1		3.2 ms delay for auto-monitor holdoff timer.
						1	0		12.8 ms delay for auto-monitor holdoff timer.
						1	1		51.2 ms delay for auto-monitor holdoff timer.

Table 11. Configuration Register 5 Bitmap

Configuration Register 6 - Address 0x106

This register contains the ADC input, scale, and offset fields for Lookup Table 0 (LUT0).

Bits								Default	Description
7	6	5	4	3	2	1	0		
0								0b0	Lookup Table 0 update disable. When this bit is cleared, updates to ILU0 are allowed.
1									Lookup Table 0 update disable. When this bit is set, updates to ILU0 are not allowed.
	0	0						0b11	ADC input source for LUT0. Indicates the THERMISTOR pin as the ADC input source for lookup table 0.
	0	1							ADC input source for LUT0. Indicates the EXT_TEMP pin (voltage) as the ADC input source for lookup table 0.
	1	0							ADC input source for LUT0. Indicates the EXT_TEMP pin (current) as the ADC input source for lookup table 0.
	1	1							ADC input source for LUT0. Indicates the BIAS current as the ADC input source for lookup table 0.
			0	0				0b00	ADC scale source 0. Indicates a scale factor of 1x.
			0	1					ADC scale source 0. Indicates a scale factor of 2x.
			1	0					ADC scale source 0. Indicates a scale factor of 4x.
			1	1					ADC scale source 0. Indicates a scale factor of 8x.
					0	0	0	0b000	ADC offset source 0. Indicates the ADC offset for Lookup Table 0. Offset = Full Scale * 0/8
					0	0	1		Offset = Full Scale * 7/8
					0	1	0		Offset = Full Scale * 6/8
					0	1	1		Offset = Full Scale * 5/8
					1	0	0		Offset = Full Scale * 4/8
					1	0	1		Offset = Full Scale * 3/8
					1	1	0		Offset = Full Scale * 2/8
					1	1	1		Offset = Full Scale * 1/8

Table 12. Configuration Register 6 Bitmap

Configuration Register 7 - Address 0x107

This register contains the ADC input, scale, and offset fields for Lookup Table 1 (LUT1).

Bits								Default	Description
7	6	5	4	3	2	1	0		
0								0b0	Lookup Table 1 update disable. When this bit is cleared, updates to ILU1 are allowed in auto-monitor mode.
1									Lookup Table 1 update disable. When this bit is set, updates to ILU1 are not allowed in auto-monitor mode.
	0	0						0b00	ADC input source for LUT1. Indicates the THERMISTOR pin as the ADC input source for lookup table 1.
	0	1							ADC input source for LUT1. Indicates the EXT_TEMP pin (voltage) as the ADC input source for lookup table 1.
	1	0							ADC input source for LUT1. Indicates the EXT_TEMP pin (current) as the ADC input source for lookup table 1.
	1	1							ADC input source for LUT1. Indicates the BIAS current as the ADC input source for lookup table 1.
			0	0				0b00	ADC scale source 1. Indicates a scale factor of 1x.
			0	1					ADC scale source 1. Indicates a scale factor of 2x.
			1	0					ADC scale source 1. Indicates a scale factor of 4x.
			1	1					ADC scale source 1. Indicates a scale factor of 8x.
					0	0	0	0b000	ADC offset source 1. Indicates the ADC offset for Lookup Table 1. Offset = Full Scale * 0/8
					0	0	1		Offset = Full Scale * 7/8
					0	1	0		Offset = Full Scale * 6/8
					0	1	1		Offset = Full Scale * 5/8
					1	0	0		Offset = Full Scale * 4/8
					1	0	1		Offset = Full Scale * 3/8
					1	1	0		Offset = Full Scale * 2/8
					1	1	1		Offset = Full Scale * 1/8

Table 13. Configuration Register 7 Bitmap

Configuration Register 8 - Address 0x108

This register contains the power-up DAC settings for Lookup Table 0.

Bits								Default	Description
7	6	5	4	3	2	1	0		
Power up DAC 0								0x00	Lookup current for DAC 0 ((High-Low) * n/256 + Low), where ‘High’ refers to High DAC 0, ‘Low’ refers to Low DAC 0, and ‘n’ equals the value programmed in this register.

Table 14. Configuration Register 8 Bitmap

Configuration Register 9 - Address 0x109

This register contains the power-up DAC settings for Lookup Table 0.

Bits								Default	Description
7	6	5	4	3	2	1	0		
Power up DAC 1								0x00	Lookup current for DAC 1 ((High-Low) * n/256 + Low), where ‘High’ refers to High DAC 1, ‘Low’ refers to Low DAC 1, and ‘n’ equals the value programmed in this register.

Table 15. Configuration Register 9 Bitmap

Configuration Register 10 - Address 0x10A

This register contains the low DAC settings for Lookup Table 0.

Bits								Default	Description
7	6	5	4	3	2	1	0		
Low DAC 0								0x00	Low DAC Lookup current for table 0 (2.5 mA * n/256), where ‘n’ equals the value programmed in this register.

Table 16. Configuration Register 10 Bitmap

Configuration Register 11 - Address 0x10B

This register contains the high DAC settings for Lookup Table 0.

Bits								Default	Description
7	6	5	4	3	2	1	0		
High DAC 0								0x00	High DAC Lookup current for table 0 (2.5 mA * (256 - n)/256), where ‘n’ equals the value programmed in this register.

Table 17. Configuration Register 11 Bitmap

Configuration Register 12 - Address 0x10C

This register contains the low DAC settings for Lookup Table 1.

Bits								Default	Description
7	6	5	4	3	2	1	0		
Low DAC 1								0x00	Low DAC Lookup current for table 1 (2.5 mA * n/256), where ‘n’ equals the value programmed in this register.

Table 18. Configuration Register 12 Bitmap

Configuration Register 13 - Address 0x10D

This register contains the high DAC settings for Lookup Table 1.

Bits								Default	Description
7	6	5	4	3	2	1	0		
High DAC 1								0x00	High DAC Lookup current for table 1 (2.5 mA * (256 - n)/256), where ‘n’ equals the value programmed in this register.

Table 19. Configuration Register 13 Bitmap

Configuration Register 14 - Address 0x10E

This register contains output polarity and bias current information.

Bits								Default	Description
7	6	5	4	3	2	1	0		
0								0b0	Output polarity for ILU1. 0 = sink current.
1									Output polarity for ILUI. 1 = source current.
	0							0b0	Output polarity for ILU0. 0 = sink current.
	1								Output polarity for ILU0. 1 = source current.
		0						0b0	Quick start enabled.
		1							Quick start disabled.
			0					0b0	Bias current controlled by APC loop, or conditions from bit 3, Note 1
			1						Bias current fixed by ILU1 only while AM# is not asserted.
				0				0b0	Bias current controlled by APC loop, or conditions from bit 4, Note 1
				1					Bias current fixed by ILU1 at all time.
					0	0	0	0b000	Maximum bias current setting. 100 mA * (n+1)/8, where ‘n’ equals the value programmed in this register.
					.	.	.		
					1	1	1		

Table 20. Configuration Register 14 Bitmap

Note 1 - If bit 3 is set to a '1', then the APC feedback loop is not used at all - the bias current is a fixed value based on ILU1. If bit 3 is '0' and bit 4 is '1', then the APC loop does determine the bias current as long as AM# is asserted. When AM# is not asserted, then the bias current is fixed based on ILU1. If both bits are 0, then the bias current is only determined by the APC loop.

Configuration Register 15 - Address 0x10F

This register contains fast mode enable, alarm control, configuration lockout, and write protect information.

Bits								Default	Description
7	6	5	4	3	2	1	0		
0								0b0	Fast Mode on ENA# is disabled
1									Fast Mode on ENA# is enabled.
	0							0b0	E^2PROM write protect. E^2PROM Write Protect is determined by the WP status bit
	1								E^2PROM write protect. E^2PROM is write protected when ENA# is asserted.
		0						0b0	Alarm reset. A write to the status register will reset Alarm.
		1							Alarm reset. When the AM# pin is de-asserted, the Alarm is reset.
			0					0b0	Alarm Forces Shutdown. When this bit is cleared, an alarm does not cause a shutdown.
			1						Alarm Forces Shutdown. When this bit is set, an alarm causes a shutdown.
				0				0b0	Configuration Lockout. When this bit is cleared, the configuration registers are not locked out and can be accessed.
				1					Configuration Lockout. When this bit is set, the configuration registers are locked out and cannot be accessed.
					0			0b0	Write-protect not set on power-up.
					1				Write-protect set on power-up.
						0	0	0b11	Sample interval is 0.4 ms.
						0	1		Sample interval is 3.2 ms.
						1	0		Sample interval is 51.2 ms.
						1	1		Sample interval is 409.6 ms.

Table 21. Configuration Register 15 Bitmap

PACKAGE DRAWING

Figure 25 shows the package dimensions for the 28-pin QFN package.

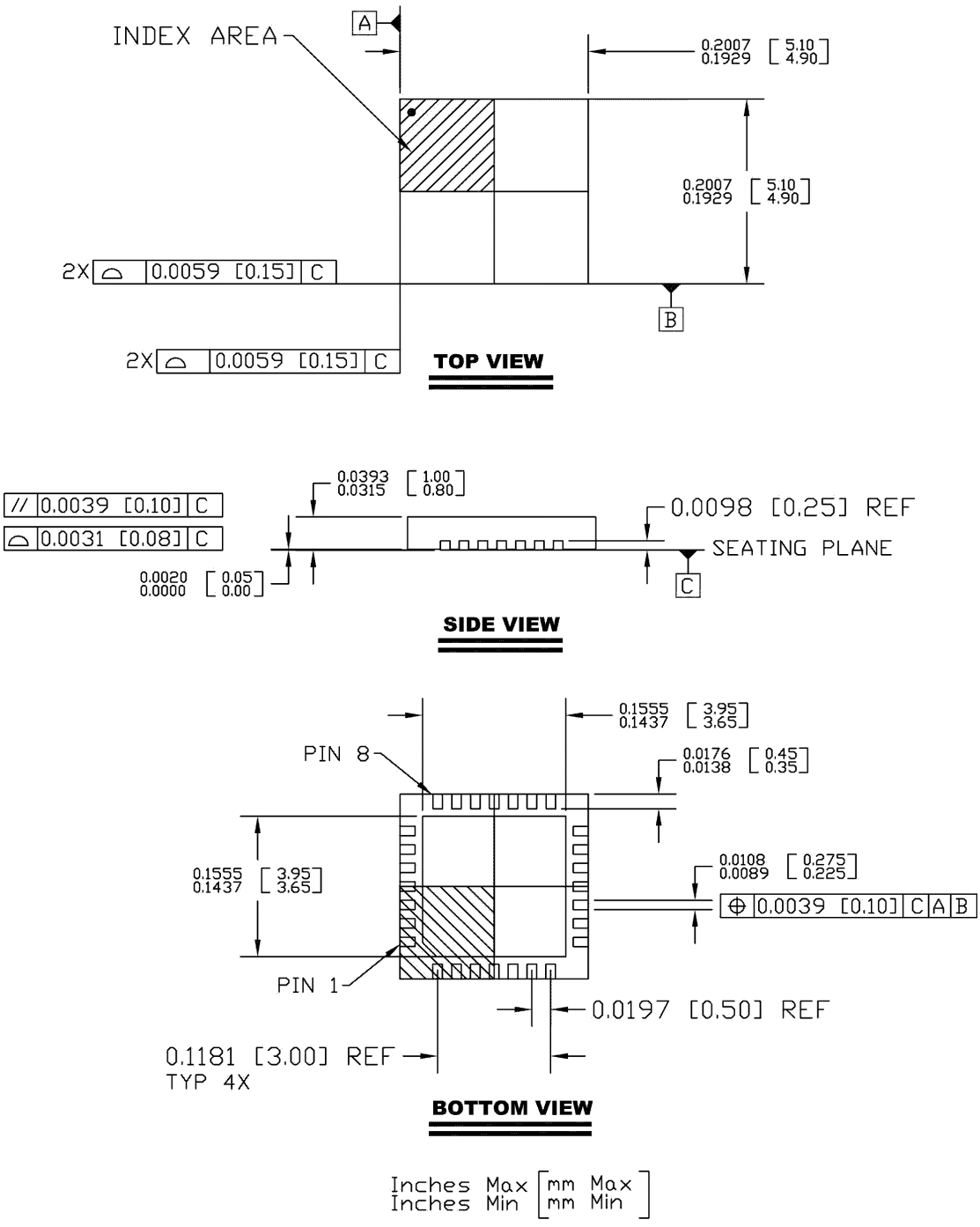
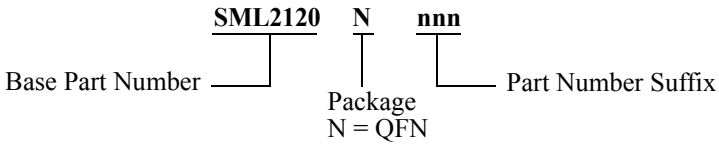
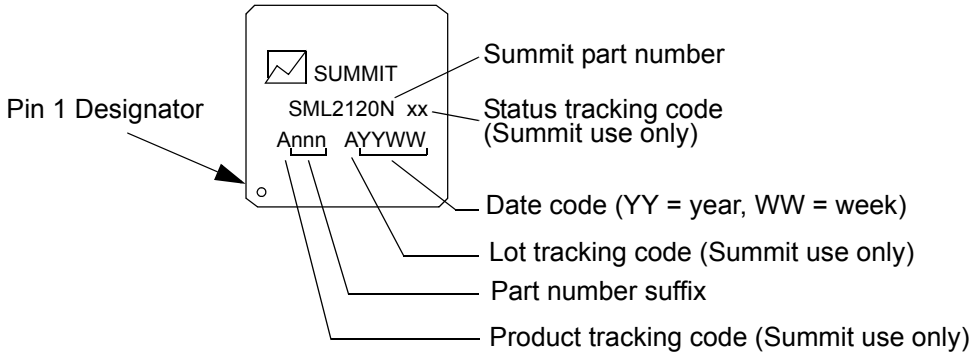


Figure 25. 28-Pin QFN Package Drawing

ORDERING INFORMATION



PART MARKING



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