

## Military 128K x 8 CMOS EPROM

### KEY FEATURES

- **High Performance CMOS**
  - 90 ns Access Time
- **Fast Programming**
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000 Volts
- **DESC SMD No. 5962-89614**
- **Compatible with JEDEC 27010 and 27C010 EPROMs**
- **JEDEC Standard Pin Configuration**
  - 32 Pin CERDIP Package
  - 32 Pin Leadless Chip Carrier (CLLCC)

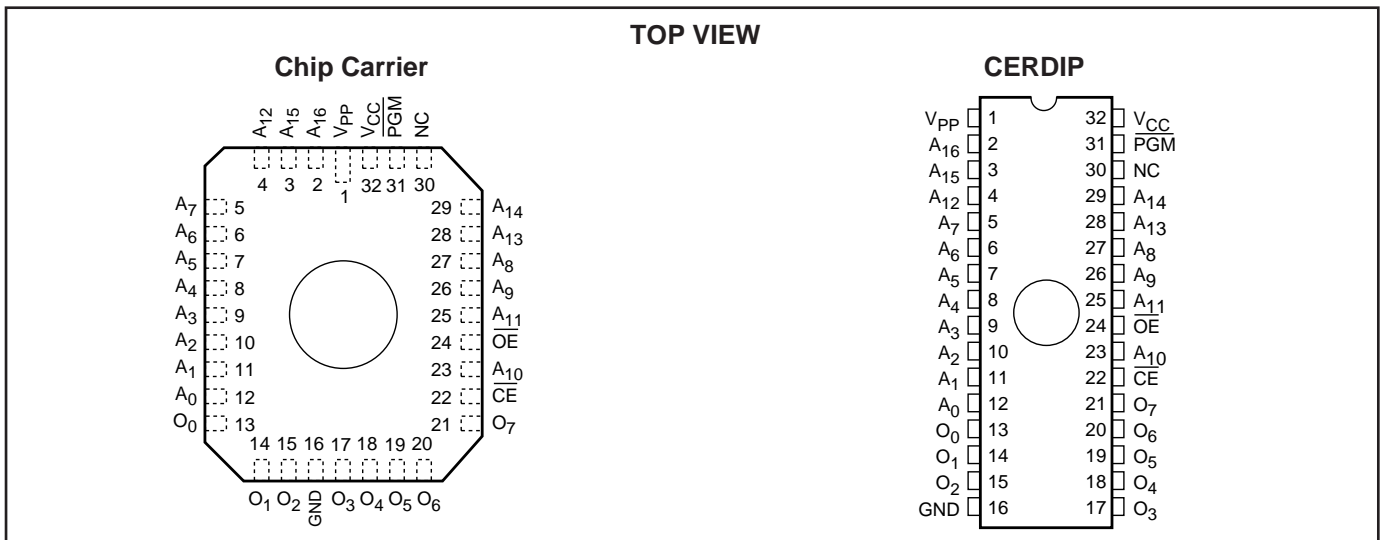
### GENERAL DESCRIPTION

The WS27C010L is a performance oriented 1 Meg UV Erasable Electrically Programmable Read Only Memory organized as 128K words x 8 bits/word. It is manufactured using an advanced CMOS technology which enables it to operate at data access times as fast as 120 nsecs. The memory was designed utilizing WSI's patented self-aligned split gate EPROM cell, resulting in a low power device with a very cost effective die size.

The WS27C010L 1 Meg EPROM provides extensive code store capacity for microprocessor, DSP, and microcontroller-based systems. Its 120 nsec access time over the full Military temperature range provides the potential of no-wait state operation. And where this parameter is important, the WS27C010L provides the user with a very fast 35 nsec  $T_{OE}$  output enable time.

The WS27C010L is offered in both a 32 pin 600 mil CERDIP, and a 32 pad Ceramic Leadless Chip Carrier (CLLCC) for surface mount applications. Its standard JEDEC EPROM pinouts provide for automatic upgrade density paths for existing 128K and 256K EPROM users.

### PIN CONFIGURATION



### PRODUCT SELECTION GUIDE

PARAMETER	27C010L-90	27C010L-12	27C010L-15	27C010L-17	27C010L-20
Address Access Time (Max)	90 ns	120 ns	150 ns	170 ns	200 ns
Chip Select Time (Max)	90 ns	120 ns	150 ns	170 ns	200 ns
Output Enable Time (Max)	35 ns	35 ns	40 ns	40 ns	40 ns

**ABSOLUTE MAXIMUM RATINGS\***

Storage Temperature.....-65° to + 150°C  
 Voltage on any Pin with Respect to Ground .....-0.6V to +7V  
 $V_{PP}$  with Respect to Ground.....-0.6V to + 14V  
 $V_{CC}$  Supply Voltage with Respect to Ground .....-0.6V to +7V  
 ESD Protection.....>2000V

**\*NOTICE:**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

**OPERATING RANGE**

RANGE	TEMPERATURE	$V_{CC}$
Military	-55°C to +125°C	+5V ± 10%

**DC READ CHARACTERISTICS** Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
$V_{IL}$	Input Low Voltage		-0.5	0.8	V
$V_{IH}$	Input High Voltage		2.0	$V_{CC} + 1$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1 \text{ mA}$		0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -400 \mu\text{A}$	3.5		V
$I_{SB1}$	$V_{CC}$ Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3 \text{ V}$ (Note 2)		100	$\mu\text{A}$
$I_{SB2}$	$V_{CC}$ Standby Current	$\overline{CE} = V_{IH}$		1	mA
$I_{CC}$	$V_{CC}$ Active Current (TTL)	$\overline{CE} = \overline{OE} = V_{IL}$ (Note 1)	F = 5 MHz	50	mA
			F = 8 MHz	60	mA
$I_{PP}$	$V_{PP}$ Supply Current	$V_{PP} = V_{CC}$		100	$\mu\text{A}$
$V_{PP}$	$V_{PP}$ Read Voltage		$V_{CC} - 0.4$	$V_{CC}$	V
$I_{LI}$	Input Leakage Current	$V_{IN} = 5.5 \text{ V}$ or Gnd	-10	10	$\mu\text{A}$
$I_{LO}$	Output Leakage Current	$V_{OUT} = 5.5 \text{ V}$ or Gnd	-10	10	$\mu\text{A}$

NOTES: 1. The supply current is the sum of  $I_{CC}$  and  $I_{PP}$ . The maximum current value is with Outputs  $O_0$  to  $O_7$  unloaded.  
 2. CMOS inputs:  $V_{IL} = \text{GND} \pm 0.3\text{V}$ ,  $V_{IH} = V_{CC} \pm 0.3 \text{ V}$ .

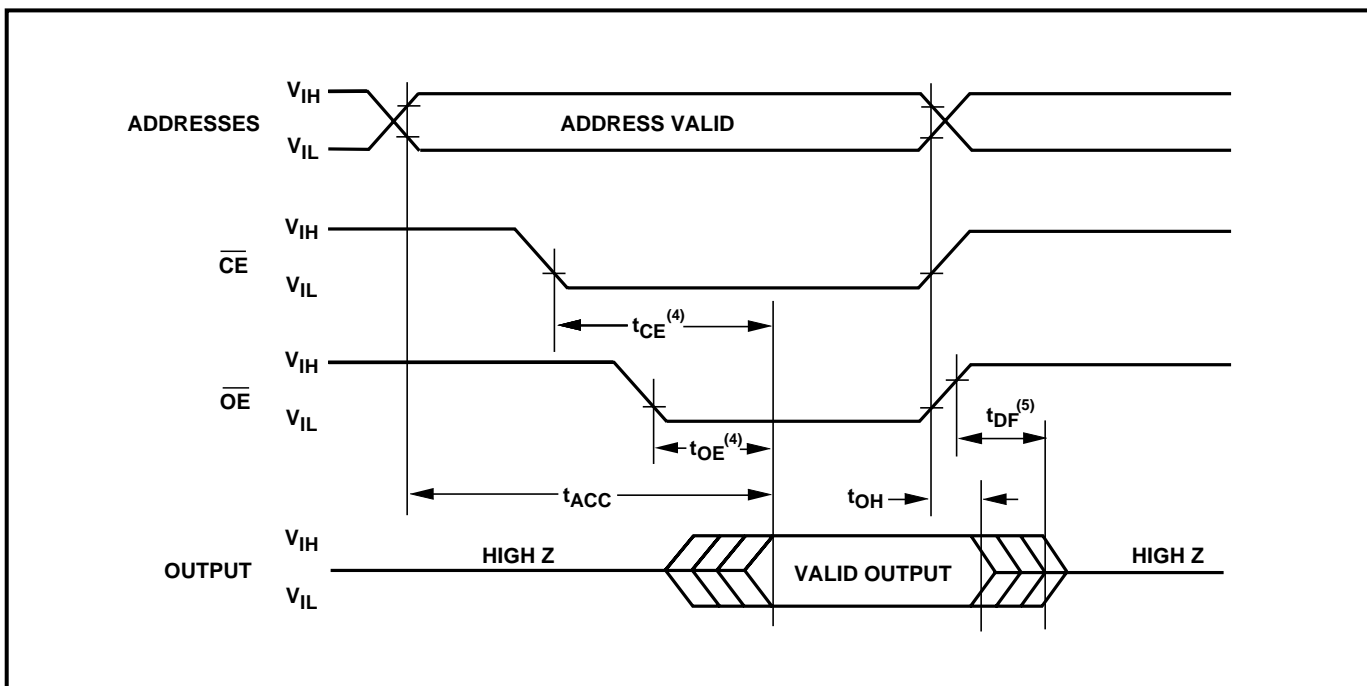
**AC READ CHARACTERISTICS** Over Operating Range with  $V_{PP} = V_{CC}$ .

SYMBOL	PARAMETER	-90		-12		-15		-17		-20		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{ACC}$	Address to Output Delay		90		120		150		170		200	ns
$t_{CE}$	$\overline{CE}$ to Output Delay		90		120		150		170		200	
$t_{OE}$	$\overline{OE}$ to Output Delay		35		35		40		40		40	
$t_{DF}$	Output Disable to Output Float (Note 3)		35		35		40		40		40	
$t_{OH}$	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ , Whichever Occurred First (Note 3)	0		0		0		0		0		

NOTE: 3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.



**AC READ TIMING DIAGRAM**



NOTE: 4.  $\overline{OE}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$ .

**CAPACITANCE<sup>(5)</sup>**  $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$

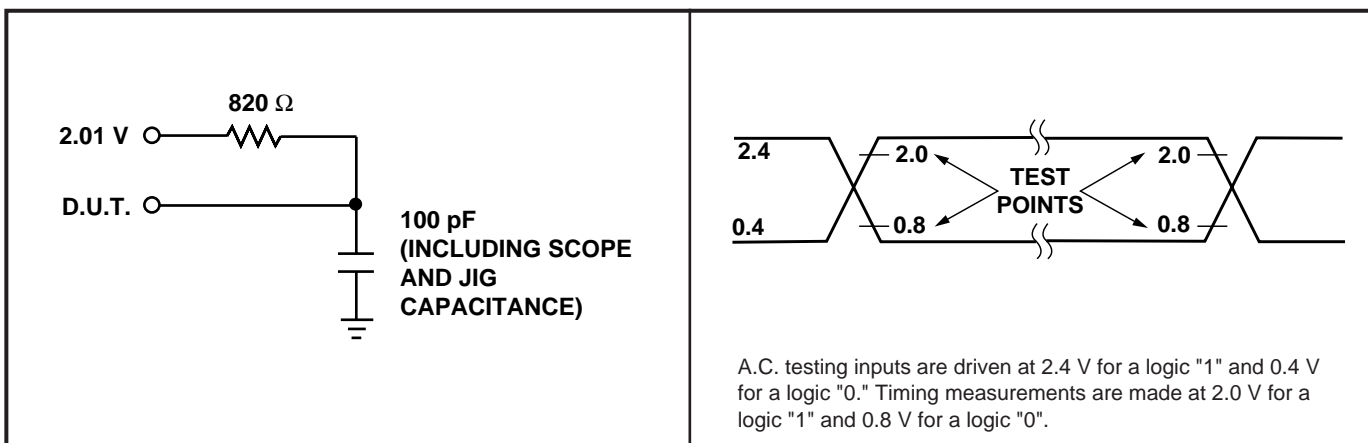
SYMBOL	PARAMETER	CONDITIONS	TYP <sup>(6)</sup>	MAX	UNITS
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	4	6	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	8	12	pF
$C_{VPP}$	$V_{PP}$ Capacitance	$V_{PP} = 0V$	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.

6. Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltages.

**TEST LOAD** (High Impedance Test Systems)

**A.C. TESTING INPUT/OUTPUT WAVEFORM**



A.C. testing inputs are driven at 2.4 V for a logic "1" and 0.4 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 0.1 microfarad capacitor in parallel with a 0.01 microfarad capacitor connected between  $V_{CC}$  and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.



**PROGRAMMING INFORMATION**

**DC CHARACTERISTICS** ( $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.25 \pm 0.25\text{ V}$ ,  $V_{PP} = 12.75 \pm 0.25\text{ V}$ . See Notes 8, 9 and 10)

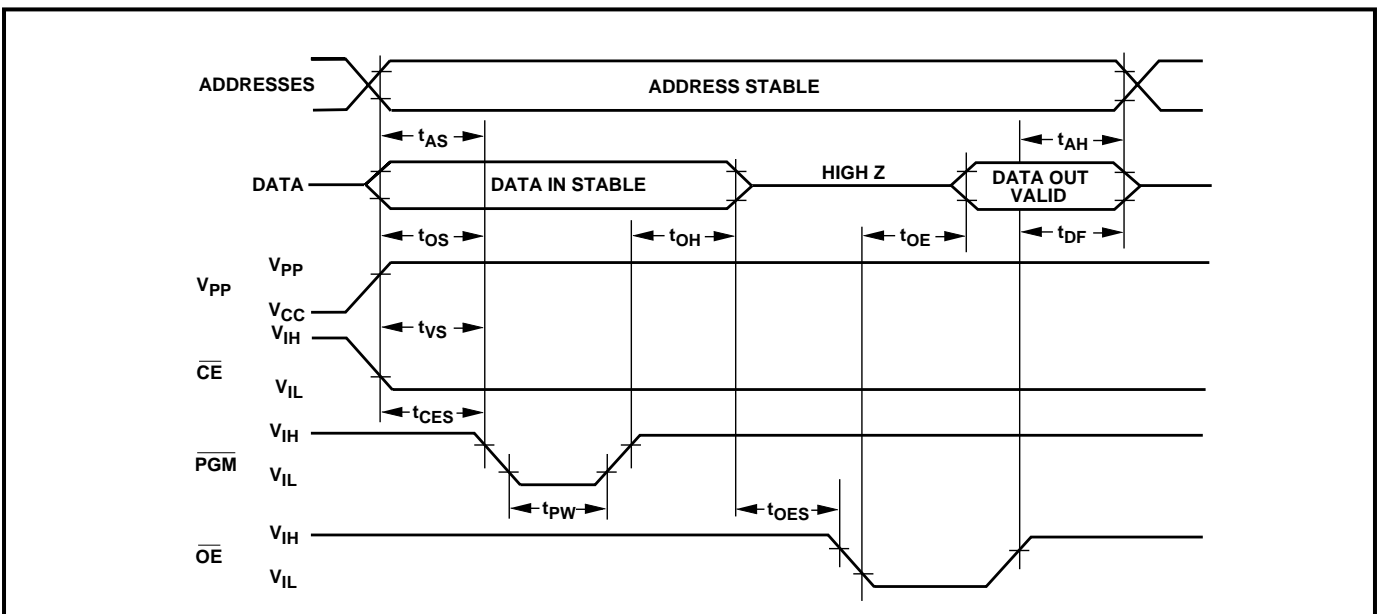
SYMBOLS	PARAMETER	MIN	MAX	UNITS
$I_{LI}$	Input Leakage Current ( $V_{IN} = V_{CC}$ or Gnd)	-10	10	$\mu\text{A}$
$I_{PP}$	$V_{PP}$ Supply Current During Programming Pulse ( $\overline{CE} = \overline{PGM} = V_{IL}$ )		60	mA
$I_{CC}$	$V_{CC}$ Supply Current		50	mA
$V_{IL}$	Input Low Voltage	-0.1	0.8	V
$V_{IH}$	Input High Voltage	2.0	$V_{CC} + 0.3$	V
$V_{OL}$	Output Low Voltage During Verify ( $I_{OL} = 2.1\text{ mA}$ )		0.4	V
$V_{OH}$	Output High Voltage During Verify ( $I_{OH} = -400\ \mu\text{A}$ )	3.5		V

- NOTES:** 8.  $V_{CC}$  must be applied either coincidentally or before  $V_{PP}$  and removed either coincidentally or after  $V_{PP}$ .  
 9.  $V_{PP}$  must not be greater than 14 volts including overshoot. During  $\overline{CE} = \overline{PGM} = V_{IL}$ ,  $V_{PP}$  must not be switched from 5 volts to 12.75 volts or vice-versa.  
 10. During power up the  $\overline{PGM}$  pin must be brought high ( $\geq V_{IH}$ ) either coincident with or before power is applied to  $V_{PP}$ .

**AC CHARACTERISTICS** ( $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.25 \pm 0.25\text{ V}$ ,  $V_{PP} = 12.75 \pm 0.25\text{ V}$ )

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
$t_{AS}$	Address Setup Time	2			$\mu\text{s}$
$t_{OES}$	Output Enable Setup Time	2			$\mu\text{s}$
$t_{OS}$	Data Setup Time	2			$\mu\text{s}$
$t_{AH}$	Address Hold Time	0			$\mu\text{s}$
$t_{OH}$	Data Hold Time	2			$\mu\text{s}$
$t_{DF}$	Chip Disable to Output Float Delay	0		55	ns
$t_{OE}$	Data Valid From Output Enable			55	ns
$t_{VS}/t_{CES}$	$V_{PP}$ Setup Time/ $\overline{CE}$ Setup Time	2			$\mu\text{s}$
$t_{PW}$	$\overline{PGM}$ Pulse Width	0.1	3	4	ms

**PROGRAMMING WAVEFORM**



**MODE SELECTION**

The modes of operation of the WS27C010L are listed below. A single 5 V power supply is required in the read mode. All inputs are TTL levels except for  $V_{PP}$  and  $A_9$  for device signature.

MODE	PINS	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	$A_9$	$A_0$	$V_{PP}$	$V_{CC}$	OUTPUTS
Read		$V_{IL}$	$V_{IL}$	X <sup>(11)</sup>	X	X	X	5.0 V	$D_{OUT}$
Output Disable		X	$V_{IH}$	X	X	X	X	5.0 V	High Z
Standby		$V_{IH}$	X	X	X	X	X	5.0 V	High Z
Programming		$V_{IL}$	$V_{IH}$	$V_{IL}$	X	X	$V_{PP}$ <sup>(12)</sup>	6.0 V	$D_{IN}$
Program Verify		$V_{IL}$	$V_{IL}$	$V_{IH}$	X	X	$V_{PP}$ <sup>(12)</sup>	6.0 V	$D_{OUT}$
Program Inhibit		$V_{IH}$	X	X	X	X	$V_{PP}$ <sup>(12)</sup>	5.0 V	High Z
Signature	Manufacturer <sup>(13)</sup>	$V_{IL}$	$V_{IL}$	X	$V_H$ <sup>(12)</sup>	$V_{IL}$	X	5.0 V	23 H
	Device <sup>(13)</sup>	$V_{IL}$	$V_{IL}$	X	$V_H$ <sup>(12)</sup>	$V_{IH}$	X	5.0 V	C1 H

NOTES: 11. X can be  $V_{IL}$  or  $V_{IH}$ .

12.  $V_H = V_{PP} = 12.75 \pm 0.25$  V.

13.  $A_1 - A_8, A_{10} - A_{16} = V_{IL}$ .

**ORDERING INFORMATION**

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C010L-12CMB*	120	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C010L-12DMB*	120	32 Pin CERDIP, 0.6"	D4	Military	MIL-STD-883C
WS27C010L-15CMB	150	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C010L-15DMB	150	32 Pin CERDIP, 0.6"	D4	Military	MIL-STD-883C
WS27C010L-17CMB*	170	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C010L-17DMB*	170	32 Pin CERDIP, 0.6"	D4	Military	MIL-STD-883C
WS27C010L-20CMB*	200	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C010L-20DMB*	200	32 Pin CERDIP, 0.6"	D4	Military	MIL-STD-883C

NOTE: 14. The actual part marking will not include the initials "WS."

\*SMD product. See page 4-2 for SMD number.

**PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS**

**REFER TO  
PAGE 5-1**

The WS27C010L is programmed using Algorithm E shown on page 5-11.

(This product can also be programmed by using National Semiconductor's 27C010 Programming Algorithm.)

