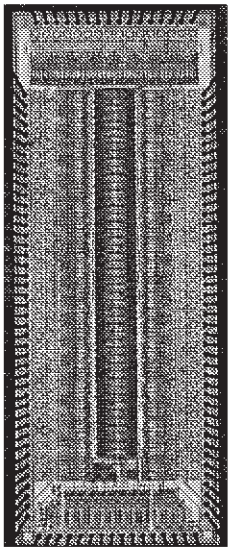
STV7620

PLASMA DISPLAY PANEL DATA DRIVER

PRELIMINARY DATA

FEATURES

- 96 Outputs Plasma Display Driver
- 90V Absolute Maximum Rating
- Reduced EMI (Electro Magnetic Interference)
- 3.3V / 5V Compatible Logic
- -40 / 30 mA Source / Sink Output Mos
- 6 Bit Data Bus (40 MHz)
- BCD Process
- Packaging Adapted to Customer Request (DICE, COB, COF, TAB).



Order code (1)	**Version**
STV7620S	slow speed
STV7620M	medium speed
STV7620F	fast speed

(1) refer to timing characteristics (Section 10)

Please contact STMicroelectronics for ordering information concerning samples or bump version

DESCRIPTION

STV7620S/M/F is a data driver for Plasma Display Panel (PDP) designed in the ST proprietary BCD high voltage technology. A new shape of the output pulse generated by the STV7620S/M/F ensures a noticeable EMI reduction. Three different versions are available with various falling edge shapes. Using a 6 bit wide data bus, they can control 96 high current & high voltage outputs. The STV7620S/M/F is supplied with a separated 70V power output supply and a 5V logic supply. All command inputs are CMOS and 3.3V logic levels compatible.

Version 3.1

Revision follow-up

Target specification

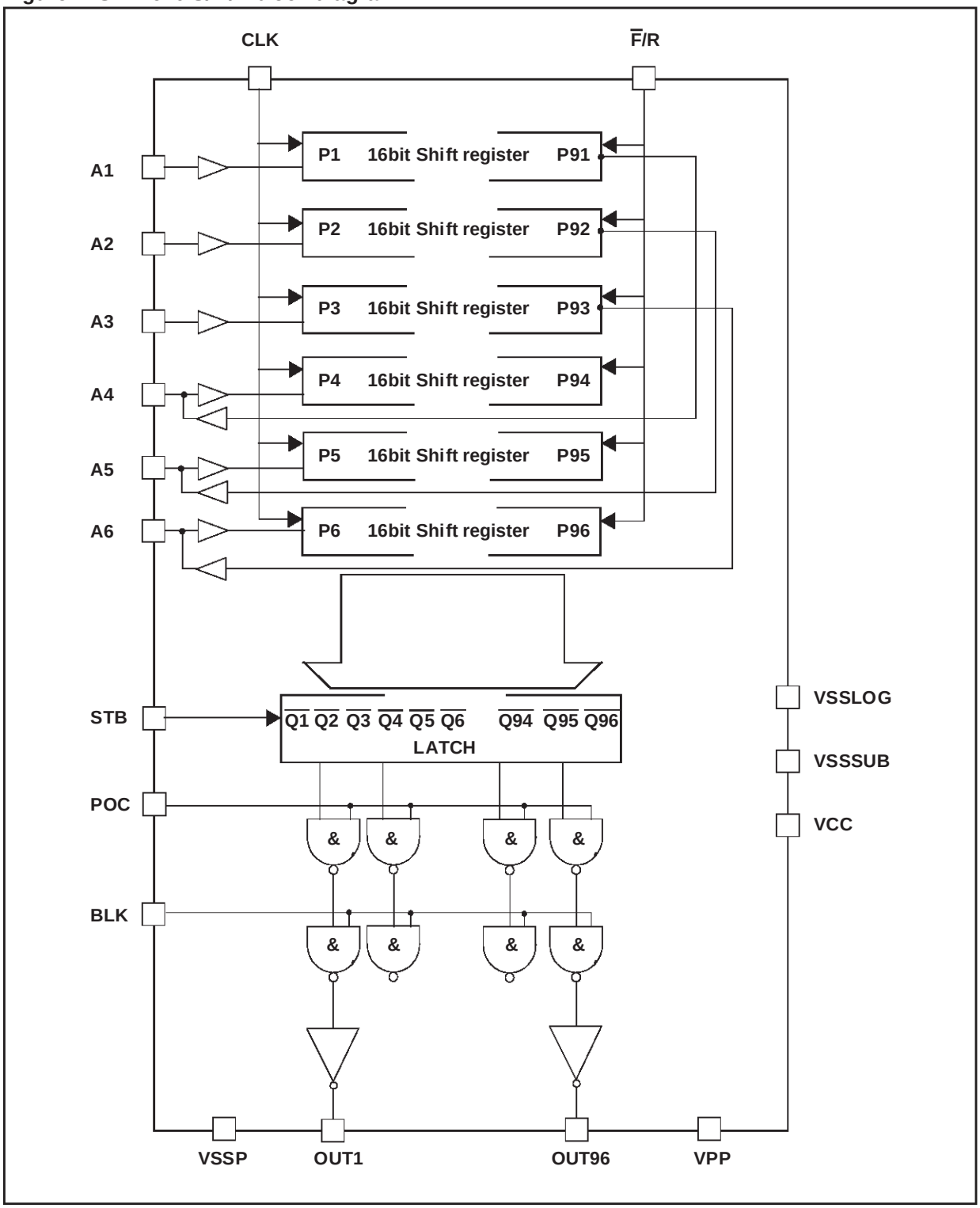
02/2001	version 1.0
	document creation
03/2001	version 1.1
	general update, addition of EMI and figure 1
04/2001	version 1.2
	general update, new pads dimensions
10/2001	version 1.3
	addition of die photo in cover page, new pads dimensions
	Electrical characteristics: replaced a few TBD mentions with values
	AC timing characteristics: some TBD replaced with values
	F/$\overline{R}$ replaced with $\overline{F}$/R
	Electrical characteristics: Idoutl/h value replaced with ±30mA

Preliminary data

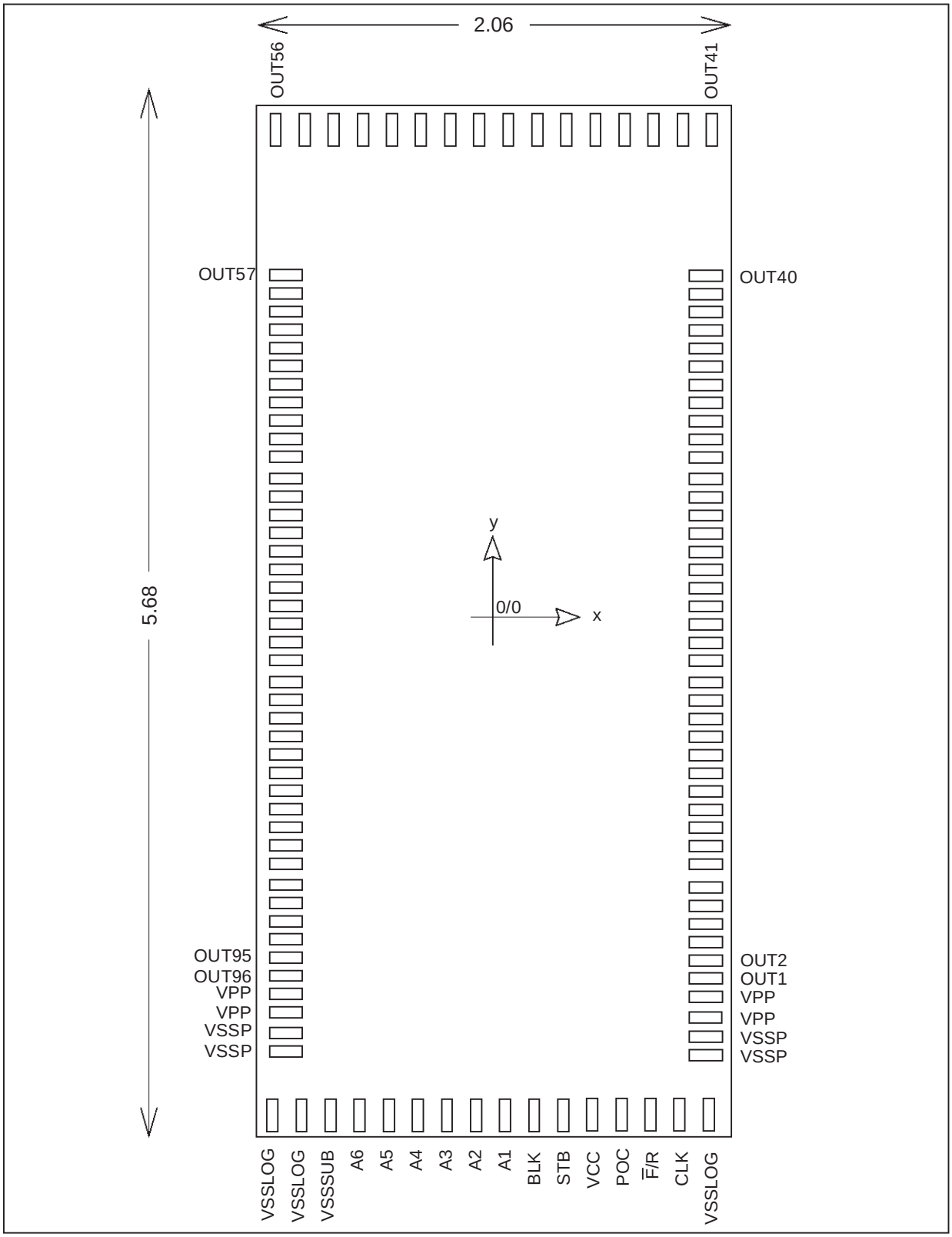
02/2002	version 3.0
	whole document: sales type becomes STV7620S/M/F for slow, medium, fast general update
04/02/2002	Version 3.1
	general update

1 BLOCK DIAGRAM

Figure 1. STV7620 S/M/F block diagram



2 DIE PIN OUT / DIE DESCRIPTION



3 PADS DIMENSIONS (in μm)/ PADS POSITIONS

The reference is the centre of the die (x=0, y=0)
Pad size is specified for wire-bonding options

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TOP SIDE from left to right

Name	Centre:X	Centre:Y	Size:x	SIze: y
OUT56	-774.478	2696.03	76	92
OUT55	-671.288	2696.03	76	92
OUT54	-568.098	2696.03	76	92
OUT53	-464.907	2696.03	76	92
OUT52	-361.718	2696.03	76	92
OUT51	-258.528	2696.03	76	92
OUT50	-155.338	2696.03	76	92
OUT49	-52.148	2696.03	76	92
OUT48	51.042	2696.03	76	92
OUT47	154.232	2696.03	76	92
OUT46	257.422	2696.03	76	92
OUT45	360.612	2696.03	76	92
OUT44	463.802	2696.03	76	92
OUT43	566.992	2696.03	76	92
OUT42	670.267	2696.03	76	92
OUT41	773.457	2696.03	76	92

BOTTOM SIDE from right to left

Name	Centre:X	Centre:Y	Size:x	SIze: y
VSSLOG	770.822	-2696.03	76	92
CLK	670.352	-2696.03	76	92
$\overline{F}$/R	567.162	-2696.03	76	92
POC	463.972	-2696.03	76	92
VCC	360.782	-2696.03	76	92
STB	258.442	-2696.03	76	92
BLK	155.252	-2696.03	76	92
A1	52.062	-2696.03	76	92
A2	-51.128	-2696.03	76	92
A3	-154.318	-2696.03	76	92
A4	-257.508	-2696.03	76	92
A5	-360.698	-2696.03	76	92
A6	-463.888	-2696.03	76	92

BOTTOM SIDE from right to left

Name	Centre:X	Centre:Y	Size:x	SIze: y
VSSSUB	-567.078	-2696.03	76	92
VSSLOG	-670.352	-2696.03	76	92
VSSLOG	-770.822	-2696.03	76	92

RIGHT SIDE from top to bottom

Name	Centre:X	Centre:Y	Size:x	SIze: y
OUT40	887.655	1950.792	92	76
OUT39	887.655	1847.602	92	76
OUT38	887.655	1744.327	92	76
OUT37	887.655	1641.138	92	76
OUT36	887.655	1537.947	92	76
OUT35	887.655	1434.757	92	76
OUT34	887.655	1331.568	92	76
OUT33	887.655	1228.378	92	76
OUT32	887.655	1125.188	92	76
OUT31	887.655	1021.998	92	76
OUT30	887.655	918.807	92	76
OUT29	887.655	815.618	92	76
OUT28	887.655	712.428	92	76
OUT27	887.655	609.238	92	76
OUT26	887.655	506.048	92	76
OUT25	887.655	402.857	92	76
OUT24	887.655	299.668	92	76
OUT23	887.655	196.478	92	76
OUT22	887.655	93.288	92	76
OUT21	887.655	-9.902	92	76
OUT20	887.655	-113.092	92	76
OUT19	887.655	-216.282	92	76
OUT18	887.655	-319.472	92	76
OUT17	887.655	-422.662	92	76
OUT16	887.655	-525.852	92	76
OUT15	887.655	-629.042	92	76
OUT14	887.655	-732.232	92	76

RIGHT SIDE from top to bottom

Name	Centre:X	Centre:Y	Size:x	SIze: y
OUT13	887.655	-835.422	92	76
OUT12	887.655	-938.612	92	76
OUT11	887.655	-1041.802	92	76
OUT10	887.655	-1144.992	92	76
OUT9	887.655	-1248.182	92	76
OUT8	887.655	-1351.372	92	76
OUT7	887.655	-1454.562	92	76
OUT6	887.655	-1557.752	92	76
OUT5	887.655	-1660.942	92	76
OUT4	887.655	-1764.132	92	76
OUT3	887.655	-1867.322	92	76
OUT2	887.655	-1970.512	92	76
OUT1	887.655	-2073.702	92	76
VPP	887.655	-2176.722	92	76
VPP	887.655	-2279.912	92	76
VSSP	887.655	-2383.018	92	76
VSSP	887.655	-2486.208	92	76

LEFT SIDE from bottom to top

Name	Centre:X	Centre:Y	Size:x	SIze: y
VSSP	-887.655	-2486.208	92	76
VSSP	-887.655	-2383.018	92	76
VPP	-887.655	-2279.912	92	76
VPP	-887.655	-2176.722	92	76
OUT96	-887.655	-2073.702	92	76
OUT95	-887.655	-1970.512	92	76
OUT94	-887.655	-1867.322	92	76
OUT93	-887.655	-1764.132	92	76
OUT92	-887.655	-1660.942	92	76
OUT91	-887.655	-1557.752	92	76
OUT90	-887.655	-1454.562	92	76
OUT89	-887.655	-1351.372	92	76
OUT88	-887.655	-1248.182	92	76
OUT87	-887.655	-1144.992	92	76
OUT86	-887.655	-1041.802	92	76
OUT85	-887.655	-938.612	92	76

LEFT SIDE from bottom to top

Name	Centre:X	Centre:Y	Size:x	SIze: y
OUT84	-887.655	-835.422	92	76
OUT83	-887.655	-732.232	92	76
OUT82	-887.655	-629.042	92	76
OUT81	-887.655	-525.852	92	76
OUT80	-887.655	-422.662	92	76
OUT79	-887.655	-319.472	92	76
OUT78	-887.655	-216.282	92	76
OUT77	-887.655	-113.092	92	76
OUT76	-887.655	-9.902	92	76
OUT75	-887.655	93.287	92	76
OUT74	-887.655	196.477	92	76
OUT73	-887.655	299.667	92	76
OUT72	-887.655	402.857	92	76
OUT71	-887.655	506.047	92	76
OUT70	-887.655	609.238	92	76
OUT69	-887.655	712.428	92	76
OUT68	-887.655	815.618	92	76
OUT67	-887.655	918.808	92	76
OUT66	-887.655	1021.998	92	76
OUT65	-887.655	1125.188	92	76
OUT64	-887.655	1228.378	92	76
OUT63	-887.655	1331.568	92	76
OUT62	-887.655	1434.758	92	76
OUT61	-887.655	1537.948	92	76
OUT60	-887.655	1641.137	92	76
OUT59	-887.655	1744.328	92	76
OUT58	-887.655	1847.602	92	76
OUT57	-887.655	1950.792	92	76

4 DATA BUS CONFIGURATION

$\overline{F}$/R	Input	Data Shift														
		CLK	**01**	**02**	**03**	**04**	**05**	**06**	**...**	**11**	**12**	**13**	**14**	**15**	**16**	
L	A1	Out	01	07	13	19	25	31		61	67	73	79	85	91	Forward Shift
	A2	Out	02	08	14	20	26	32		62	68	74	80	86	92	
	A3	Out	03	09	15	21	27	33		63	69	75	81	87	93	
	A4	Out	04	10	16	22	28	34		64	70	76	82	88	94	
	A5	Out	05	11	17	23	29	35		65	71	77	83	89	95	
	A6	Out	06	12	18	24	30	36		66	72	78	84	90	96	
H	A1	Out	91	85	79	73	67	61		31	25	19	13	07	01	Reverse Shift
	A2	Out	92	86	80	74	68	62		32	26	20	14	08	02	
	A3	Out	93	87	81	75	69	63		33	27	21	15	09	03	
	A4	Out	94	88	82	76	70	64		34	28	22	16	10	04	
	A5	Out	95	89	83	77	71	65		35	29	23	17	11	05	
	A6	Out	96	90	84	78	72	66		36	30	24	18	12	06	

This table describes the position of the first data sampled by the first rising edge of the CLK signal. After 16 clock pulses this data will be shifted to Output 91.

5 PIN DESCRIPTION

Symbol	Function	Description
OUT(01-96)	Output	Power output
VSSP	Ground	Ground of power outputs
VPP	Supply	High voltage supply of power outputs
BLK	Input	Blanking input
POC	Input	Power output control input
$\overline{F}$/R	Input	Selection of shift direction
VCC	Supply	5V logic supply
VSSLOG	Ground	Logic ground
VSSSUB	Ground	Substrate ground
CLK	Input	Clock of data shift register
STB	Input	Latch of data to outputs
IN (A1-A6)	Input	Shift register input
OUT(A4-A6)	output	A1, A2, A3 shift register output

6 CIRCUIT DESCRIPTION

STV7620S/M/F includes all the logic and power circuits necessary to drive the Plasma Display Panel (PDP) column of electrodes. Binary values of each pixel of the displayed line are loaded into the shift register by a 6 bit wide (A1 - A6) data bus. Data is shifted at each low to high transition of the CLK clock.

The forward /reverse ($\overline{F}$/R) input is used to select the direction of the shift register.

The maximum frequency of the shift clock is 40MHz. This leads to an equivalent 240 MHz serial shift register for a 6 x 16 bits arrangement.

When the STB signal is Low, data are transferred from the shift register to the latch and the power output stages.

All the output data are kept memorised and held in the latch stage when the latch input STB is pulled high.

Vsssub and Vsslog must be connected as close as possible to the logical reference ground of the application.

STV7620S/M/F is supplied with a 5 V power supply. All the logic inputs can be driven either by 5V CMOS logic or by 3.3V CMOS logic.

A low EMI function has been implemented: the falling edge of the outputs has 2 slopes, a smooth one followed by a steeper one.

The smooth slopes width increases from 20ns for the fast version to 55ns for the slow version whatever the external load.

Table 1: Shift register truth table

Input		Shift register function
$\overline{F}$/R	CLK	Output Q
L	rise	Forward shift
L	H or L	Steady
H	rise	Reverse shift
H	H or L	Steady
X	X	6 bits shift register

Table 2: Power output truth table

Qn	STB	BLK	POC	Driver Output	Comments
X	X	L	X	all L	Output at low level
X	X	H	L	all H	Output at high level
X	H	H	H	Qn	Data latched
L	L	H	H	L	Data copied
H	L	H	H	H	Data copied

Qn+1 = A1, Qn+2 = A2, Qn+3 = A3, Qn+4 = A4, Qn+5 = A5, Qn+6 = A6, n = [0,6,12,18,...,90]

7 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vcc	Logic supply range	-0.3, +7	V
Vpp	Driver supply range	-0.3, +90	V
Vin	Logic input voltage range	-0.3, Vcc+0.3	V
Ipout	Driver output current (Note 1)(Note 3) (Note 4:)	- 150 / + 150	mA
I_{dout}	Diode Output Current (Note 2:) (Note 3:) (Note 4:)	-200 / +300	mA
Tjmax	Maximum junction temperature	125	°C
Tstg	Storage temperature range	-50, +150	°C
Vout	Output power voltage range	-0.3, +90	V

Note 1: Through one power output.

Note 2: Through one power output for all power outputs (see Figure 4) with Junction temperature lower than or equal to Tjmax

Note 3: These parameters are measured during ST's internal qualification which includes temperature characterisation on standard batches and on corners batches of the process. These parameters are not tested on the parts.

Note 4: Transient current. Spike current duration inferior to 300ns.

Remark: ESD susceptibility
Human body model: 100pF, 1.5kΩ
A5, A6 pins - V_{ESD} = +800 V

8 ELECTRICAL CHARACTERISTICS

(Vcc = 5V, Vpp = 70V, Vssp = 0V, Vss = 0V, Tamb = 25°C, FCLK = 40 MHz, unless otherwise specified)

Symbol	Parameter	Min.	Typ	Max	Unit
SUPPLY					
Vcc	Logic supply voltage	4.50	5	5.5	V
Icc	Logic supply current (Note 5)	-		100	µA
Iccl	Logic Dynamic Supply Current (FCLK=20Mhz) (Note 6)	-	20	-	mA
Icc	Logic Supply Current (Vih=2.0V)		500	750	µA
Vpp	Power output supply voltage - DC mode	15		70	V
Vpp	Power output supply voltage - AC mode	15		75	V
Ipph	Power output supply current (steady outputs)	-	-	100	µA
OUTPUT					
OUT1-OUT96					
Vpouth	Power output high level (voltage drop versus Vpp) @Ipouth = - 25mA and Vpp = 70V	-	11	16	V
Vpoutl	Power output low level @ Ipoutl = + 25mA	-	8	13	V
Vdouth	Output diode voltage drop @ Idouth = + 30mA (Note 7)	-	1	2	V
Vdoutl	Output diode voltage drop @ Idoutl = - 30mA (Note 7)	-2	-1	-	V
INPUT					
CLK, $\overline{F}$/R, STB, POC, BLK, A1-A6					
Vih	Input high level	2.0	-	-	V
Vil	Input low level	-	-	0.9	V
Iih	High level input current (Vih >=2.0V)	-	-	5	µA
Iil	Low level input current (Vil = 0v)	-	-	5	µA
Cin	Input capacitance (Note 8)			15	pF
A4-A6					
Voh	Logic output high level (Ioh = -1mA)		4.85		V
Vol	Logic output low level (Iol = 1mA)		0.1		V

Note 5: Logic input levels compatible with 5V CMOS logic

Note 6: All data inputs are commuted at 10MHz

Note 7: see Figure 4.Test configuration page15

Note 8: This parameter is measured during ST's internal qualification which includes temperature characterization on standard and corner batches of the process. This parameter is not tested on the part.

9 AC TIMING REQUIREMENTS

(Vcc = 4.5v to 5.5v, T amb = -20 to +85°C, input signals max leading edge & trailing edge (tr,tf) = 5ns)

Symbol	Parameter	Min.	Typ	Max	Unit
t_{CLK}	Data clock period	25	-	-	ns
t_{WHCLK}	Duration of CLK pulse at high level	10	-	-	ns
t_{WLCLK}	Duration of CLK pulse at low level	10	-	-	ns
t_{SDAT}	Set-up time of data input before low to high clock transition	5	-	-	ns
t_{HDAT}	Hold-time of data input after low to high clock transition	5	-	-	ns
t_{HSTB}	Hold-time of STB after low to high clock transition	5	-	-	ns
t_{STB}	STB low level pulse duration	10	-	-	ns
t_{SSTB}	STB set-up time before CLK rise	5			ns

10 AC TIMING CHARACTERISTICS

(Vcc = 5V, Vpp = 70V, Vssp = 0V, Vsssub = 0V, Vsslog = 0V, Tamb = 25°C, FCLK = 40MHz,)
(Vilmax = 0.2Vcc, Vihmin = 0.8Vcc)

Symbol	Parameter	Min.	Typ	Max	Unit
t_{PHL1} t_{PLH1}	Delay of power output change after CLK transition - high to low - low to high	 - -	 35 30	 100 100	 ns ns
t_{PHL2} t_{PLH2}	Delay of power output change after STB transition - high to low - low to high	 -	 - -	 95 95	 ns ns
t_{PHL3} t_{PLH3}	Delay of power output change after BLK, POC transition - high to low - low to high	 -	 25 20	 90 90	 ns ns
$t_{R\ OUT}$	Power output rise time (Note 9)	50	-	200	ns
$t_{F\ OUT}$	Power output fall time (Note 9)	50	-	200	ns
t_S	Width of the falling edge smooth shape STV7620F: Fast STV7620M: Medium STV7620S: Slow	 - - -	 25 30 55	 - - -	 ns ns ns
$t_{R\ DAT}$	Logic data output rise time (CL = 10pF)	-	9	TBD	ns
$t_{F\ DAT}$	Logic data output fall time (CL = 10pF)	-	5	TBD	ns
t_{PHL4} t_{PLH4}	Delay of logic data output change after CLK transition - high to low - low to high	 - -	 12 13	 TBD TBD	 ns ns

Note 9: one output among 96, loading capacitor CL = 50pF, other outputs at low level

Figure 2. AC Characteristics Waveform

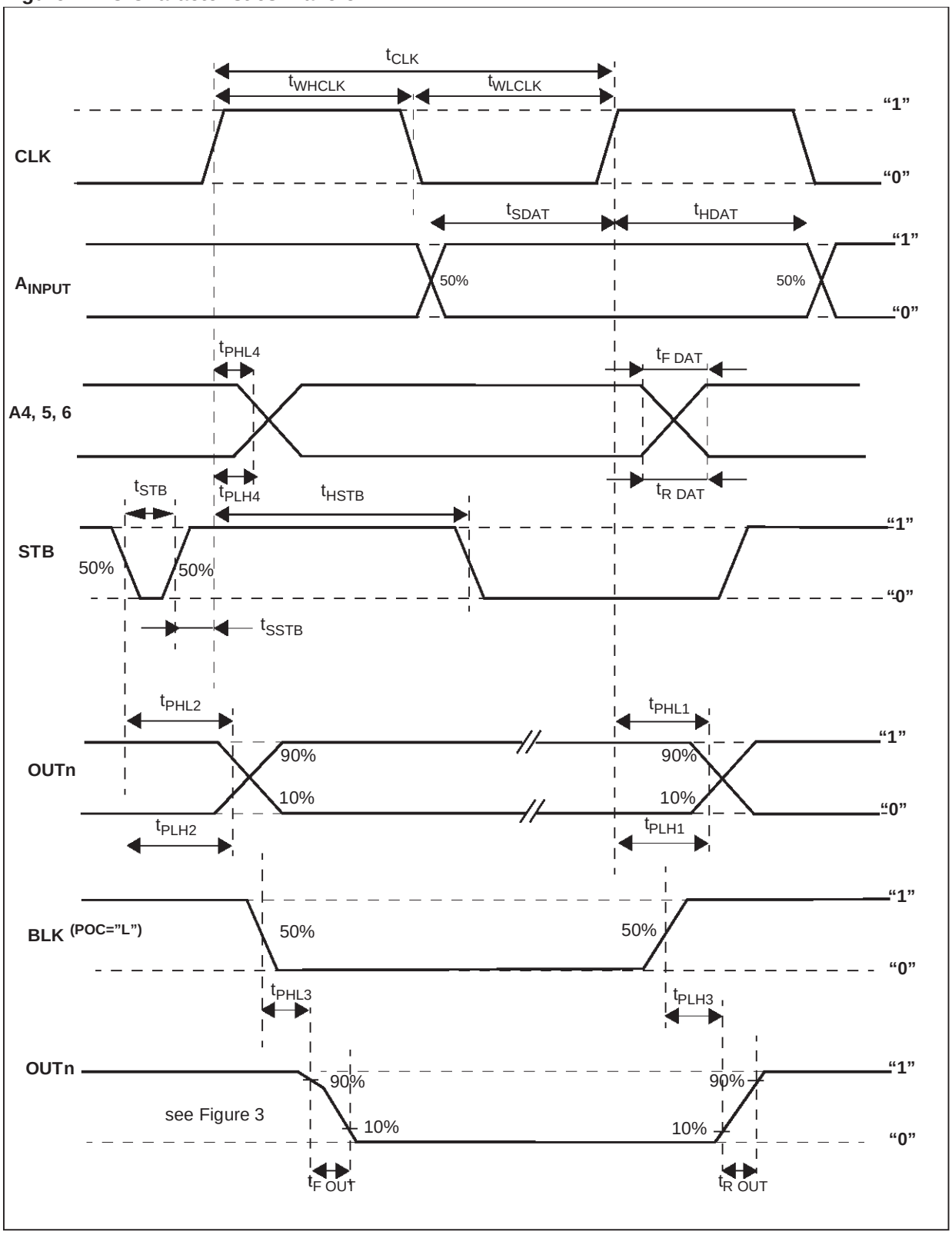


Figure 3. Zoom for OUTn showing t_S and $t_{F\ OUT}$

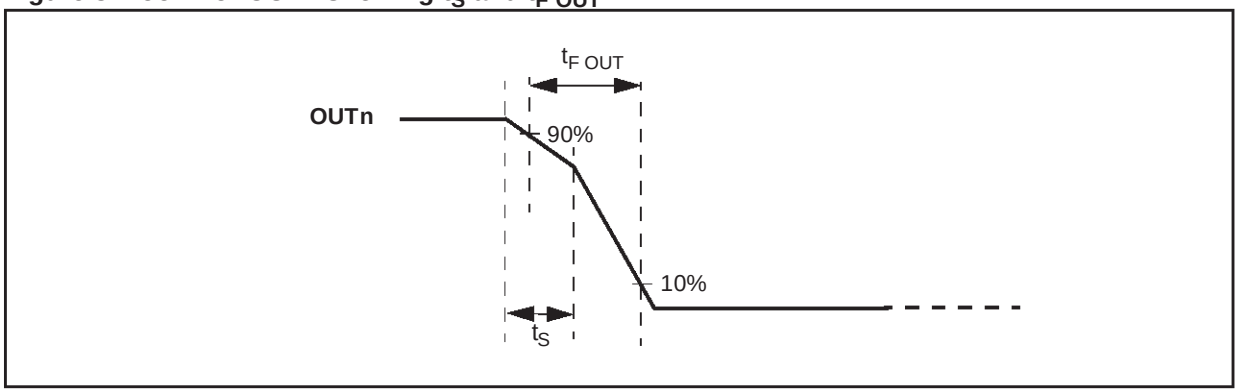
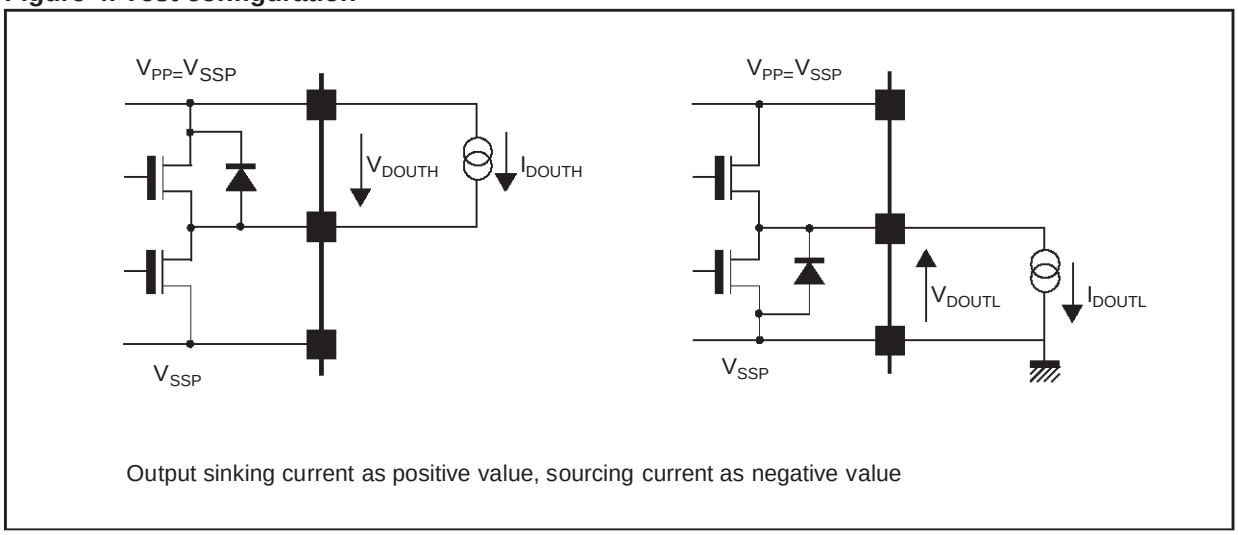


Figure 4. Test configuration



Output sinking current as positive value, sourcing current as negative value

11 TESTED WAFER DISCLAIMER

All wafers are tested and guaranteed to comply with all datasheet limits up to the point of wafer sawing for a period of ninety (90) days from the delivery date.

We remind you that it is the customer's responsibility to test and qualify their application in which the die is used. ST Microelectronics is ready to support the customer when qualifying the product.