

STP36NE06 STP36NE06FP

N - CHANNEL 60V - 0.032Ω - 36A - TO-220/TO-220FP STripFETTM POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	ID
STP36NE06	60 V	< 0.040 Ω	36 A
STP36NE06FP	60 V	< 0.040 Ω	20 A

- TYPICAL $R_{DS(on)} = 0.032 \Omega$
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- LOW GATE CHARGE 100 °C
- APPLICATION ORIENTED CHARACTERIZATION

DESCRIPTION

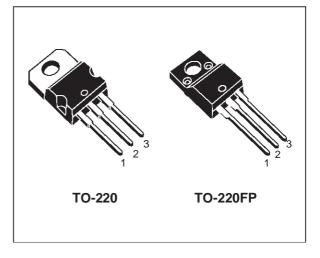
This Power Mosfet is the latest development of SGS-THOMSON unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalance characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

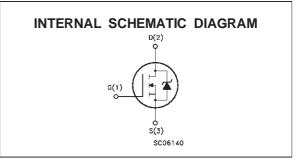
APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS

Symbol	Parameter		Va	lue	Unit
			STP36NE06	STP36NE06FP	
V _{DS}	Drain-source Voltage ($V_{GS} = 0$)		6	0	V
V _{DGR}	Drain- gate Voltage (R_{GS} = 20 k Ω)		6	0	V
V _{GS}	Gate-source Voltage		±	20	V
Ι _D	Drain Current (continuous) at T _c = 25 °C		36	20	А
Ι _D	Drain Current (continuous) at T _c = 100 °C		24	14	А
I _{DM} (●)	Drain Current (pulsed)		144	144	А
Ptot	Total Dissipation at $T_c = 25$ °C		100	35	W
	Derating Factor		0.66	0.27	W/°C
V _{ISO}	Insulation Withstand Voltage (DC)			2000	V
dv/dt	Peak Diode Recovery voltage slope			7	V/ns
T _{stg}	Storage Temperature		-65 t	o 175	°C
Tj	Max. Operating Junction Temperature		1	75	°C
(●) Pulse widt July 1998	th limited by safe operating area	(1) $I_{SD} \le 36$ /	A, di/dt ≤ 300 A/μs, V _Γ	$DD \leq V_{(BR)DSS}, T_j \leq T_{JMAX}$	1/9

ABSOLUTE MAXIMUM RATINGS





THERMAL DATA

			TO-220	TO-220FP	
R _{thj-case}	Thermal Resistance Junction-case	Max	1.51	4.28	°C/W
	Thermal Resistance Junction-ambient Thermal Resistance Case-sink Maximum Lead Temperature For Soldering Pr	Max Typ urpose	62. 0.5 30	5	°C/W °C/W °C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	36	A
E _{AS}	Single Pulse Avalanche Energy (starting $T_j = 25 \ ^{\circ}C$, $I_D = I_{AR}$, $V_{DD} = 25V$)	180	mJ

ELECTRICAL CHARACTERISTICS ($T_{case} = 25 \ ^{\circ}C$ unless otherwise specified) OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \ \mu A$ $V_{GS} = 0$	60			V
I _{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = Max Rating$ $V_{DS} = Max Rating$ $T_c = 125$ °C			1 10	μΑ μΑ
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	$V_{GS} = \pm 20 V$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250 \ \mu A$	2	3	4	V
RDS(on)	Static Drain-source On Resistance	Vgs = 10V Id = 18 A		0.032	0.04	Ω
I _{D(on)}	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10 V$	36			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g _{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_{D} = 18 \text{ A}$	7	15		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 V$ f = 1 MHz $V_{GS} = 0$		2115 260 65	2800 350 90	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r	Turn-on Time Rise Time			28 85	40 115	ns ns
(di/dt) _{on}	Turn-on Current Slope			250		A/μs
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 48 \text{ V}$ $I_{D} = 36 \text{ A}$ $V_{GS} = 10 \text{ V}$		50 13 18	70	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{r(Voff)} t _f t _c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 48 \text{ V}$ ID = 36 A R _G = 4.7 Ω V _{GS} = 10 V		12 25 40	16 35 55	ns ns ns

SOURCE DRAIN DIODE

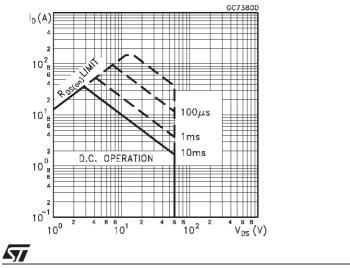
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} (●)	Source-drain Current Source-drain Current (pulsed)				36 144	A A
V _{SD} (*)	Forward On Voltage	$I_{SD} = 36 \text{ A} V_{GS} = 0$			1.5	V
t _{rr}	Reverse Recovery Time	$I_{SD} = 36 A$ di/dt = 100 A/µs V_{DD} = 30 V $T_i = 150 \ ^{\circ}C$		75		ns
Qrr	Reverse Recovery Charge			245		μC
I _{RRM}	Reverse Recovery Current			6.5		A

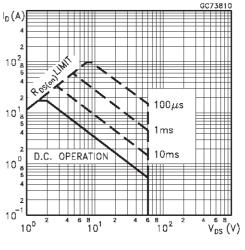
(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

(•) Pulse width limited by safe operating area

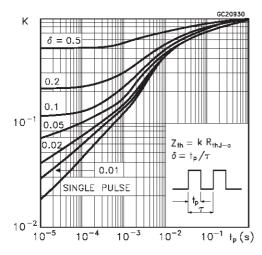
Safe Operating Area for TO-220

Safe Operating Area for TO-220FP

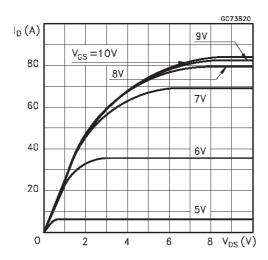




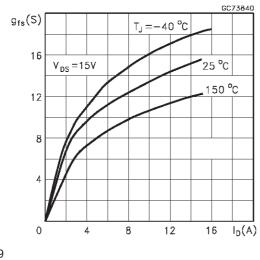
Thermal Impedance for TO-220



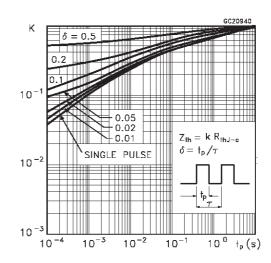
Output Characteristics



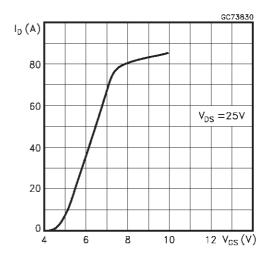
Transconductance



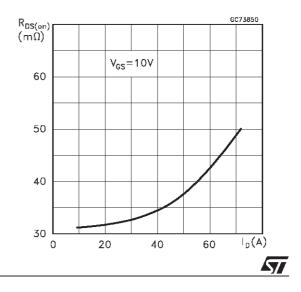
Thermal Impedance for TO-220FP

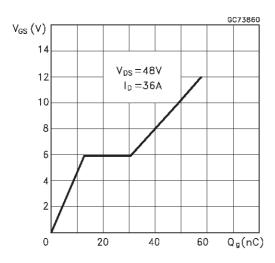


Transfer Characteristics



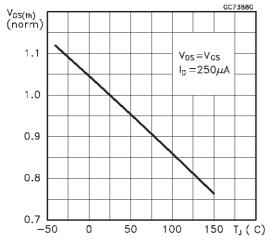
Static Drain-source On Resistance



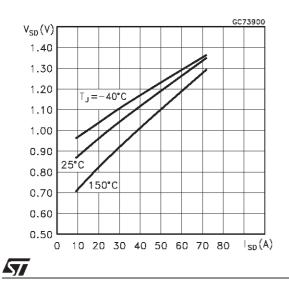


Gate Charge vs Gate-source Voltage

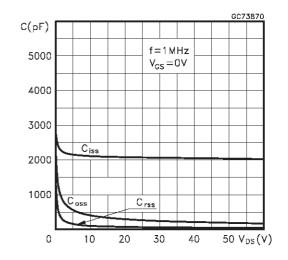
Normalized Gate Threshold Voltage vs Temperature



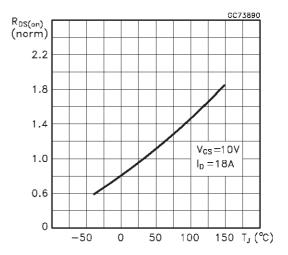
Source-drain Diode Forward Characteristics



Capacitance Variations



Normalized On Resistance vs Temperature



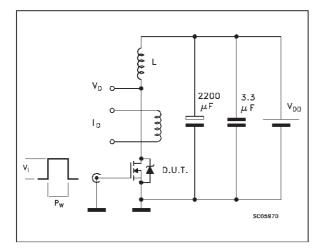


Fig. 1: Unclamped Inductive Load Test Circuit

Fig. 3: Switching Times Test Circuits For Resistive Load

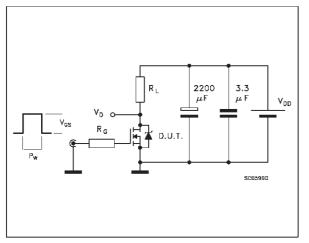


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

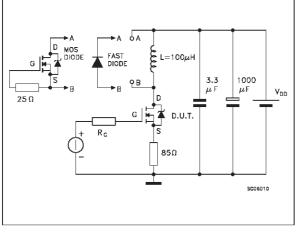


Fig. 2: Unclamped Inductive Waveform

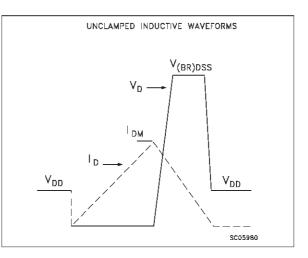
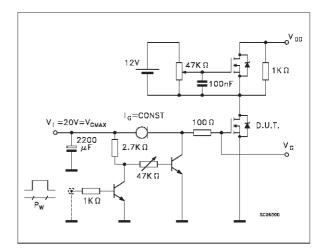
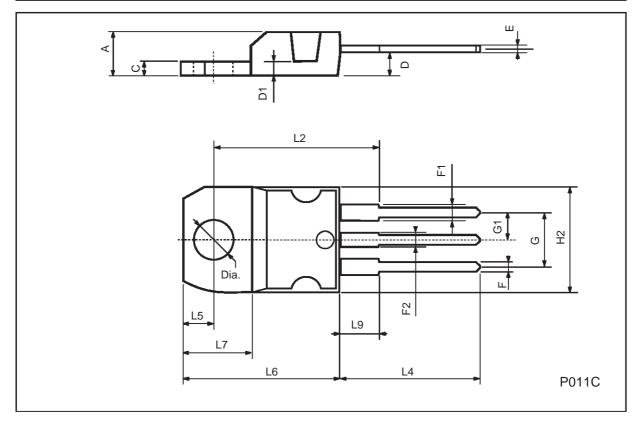


Fig. 4: Gate Charge test Circuit



DIM.		mm			inch	
DINI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А	4.40		4.60	0.173		0.181
С	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151

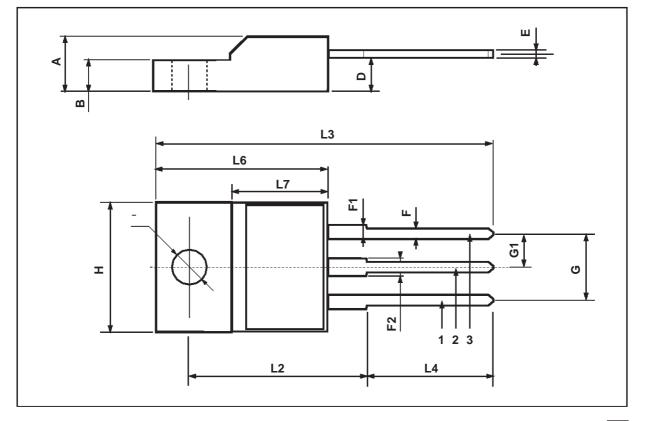




STP36NE06FP

MIN. TYP. MAX. MIN. TYP. A 4.4 4.6 0.173 B 2.5 2.7 0.098 D 2.5 2.75 0.098 E 0.45 2.75 0.098 F 0.75 0.017 0.017 F1 1.15 1.7 0.017 F2 1.15 1.7 0.045 G1 2.4 2.7 0.094 G1 2.4 2.7 0.094 G1 2.4 2.7 0.094 H 10 10.4 0.393 L2 16 30.6 1.126 L3 28.6 30.6 1.126 L4 9.8	DIM.		mm			inch	
B 2.5 2.7 0.098 D 2.5 2.75 0.098 E 0.45 0.7 0.017 F 0.75 1 0.030 F1 1.15 1.7 0.045 F2 1.15 1.7 0.045 G1 2.4 2.7 0.094 H 10 10.4 0.393 L2 16 30.6 1.126 L4 9.8 10.6 0.385		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
D 2.5 2.75 0.098 E 0.45 0.7 0.017 F 0.75 1 0.030 F1 1.15 1.7 0.045 F2 1.15 1.7 0.045 G 4.95 5.2 0.195 G1 2.4 2.7 0.094 H 10 10.4 0.393 L2 16 30.6 1.126 L3 28.6 30.6 1.126	А	4.4		4.6	0.173		0.181
E 0.45 0.7 0.017 F 0.75 1 0.030 F1 1.15 1.7 0.045 F2 1.15 1.7 0.045 G 4.95 5.2 0.195 G1 2.4 2.7 0.094 H 10 10.4 0.393 L2 16 30.6 1.126 L4 9.8 10.6 0.385	В	2.5		2.7	0.098		0.106
F 0.75 1 0.030 F1 1.15 1.7 0.045 F2 1.15 1.7 0.045 G 4.95 5.2 0.195 G1 2.4 2.7 0.094 H 10 10.4 0.393 L2 16 0.630 L3 28.6 30.6 1.126 L4 9.8 10.6 0.385	D	2.5		2.75	0.098		0.108
F1 1.15 1.7 0.045 F2 1.15 1.7 0.045 G 4.95 5.2 0.195 G1 2.4 2.7 0.094 H 10 10.4 0.393 L2 16 0.630 L4 9.8 10.6 0.385	E	0.45		0.7	0.017		0.027
F2 1.15 1.7 0.045 G 4.95 5.2 0.195 G1 2.4 2.7 0.094 H 10 10.4 0.393 L2 16 0.630 L3 28.6 30.6 1.126 L4 9.8 10.6 0.385	F	0.75		1	0.030		0.039
G 4.95 5.2 0.195 G1 2.4 2.7 0.094 H 10 10.4 0.393 L2 16 0.630 L3 28.6 30.6 1.126 L4 9.8 10.6 0.385	F1	1.15		1.7	0.045		0.067
G1 2.4 2.7 0.094 H 10 10.4 0.393 L2 16 0.630 L3 28.6 30.6 1.126 L4 9.8 10.6 0.385	F2	1.15		1.7	0.045		0.067
H 10 10.4 0.393 Image: Constraint of the state of the sta	G	4.95		5.2	0.195		0.204
L2 16 0.630 L3 28.6 30.6 1.126 L4 9.8 10.6 0.385	G1	2.4		2.7	0.094		0.106
L3 28.6 30.6 1.126 L4 9.8 10.6 0.385	Н	10		10.4	0.393		0.409
L4 9.8 10.6 0.385	L2		16			0.630	
	L3	28.6		30.6	1.126		1.204
	L4	9.8		10.6	0.385		0.417
Lo 15.9 16.4 0.626	L6	15.9		16.4	0.626		0.645
L7 9 9.3 0.354	L7	9		9.3	0.354		0.366
Ø 3 3.2 0.118		ł					0.12





8/9

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