STLC5412

2B1Q U INTERFACE DEVICE ENHANCED WITH DECT MODE

PRELIMINARY DATA

GENERAL FEATURES

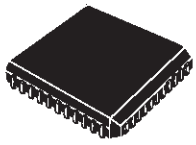
- SINGLE CHIP 2B1Q LINE CODE TRANSCEIVER
- SUITABLE FOR ISDN, PAIR GAIN AND DECT APPLICATIONS
- MEETS OR EXCEEDS ETSI EUROPEAN STANDARD
- SINGLE 5V SUPPLY
- DIP28 AND PLCC44 PACKAGE
- HCMOS3A SGS-THOMSON ADVANCED 1.2µm DOUBLE-METAL CMOS PROCESS
- ROUND TRIP DELAY MEASUREMENT
- EXTENDED TEMPERATURE RANGE (-40°C TO +70°C)

TRANSMISSION FEATURES

- 160 KBIT/S FULL DUPLEX TRANSCEIVER
- 2B1Q LINE CODING WITH SCRAMBLER/DE-SCRAMBLER
- SUPPORTS BRIDGE TAPS, SPLICES AND MIXED GAUGES
- >70DB ADAPTIVE ECHO-CANCELLATION
- ON CHIP HYBRID CIRCUIT
- DECISION FEEDBACK EQUALIZATION
- ON CHIP ANALOG VCO SYSTEM
- DIRECT CONNECTION TO SMALL LINE TRANSFORMER

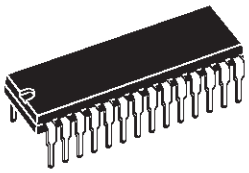
SYSTEM FEATURES

- ACTIVATION/DEACTIVATION CONTROLLER
- ON CHIP CRC CALCULATION AND VERIFICATION INCLUDING TWO PROGRAMMABLE BLOCK ERROR COUNTERS
- EOC CHANNEL AND OVERHEAD-BITS TRANSMISSION WITH AUTOMATIC MESSAGE CHECKING
- GCI AND µW/DSI MODULE INTERFACES COMPATIBLE
- DIGITAL LOOPBACKS
- COMPLETE (2B+D) ANALOG LOOPBACK IN LT
- ELASTIC DATA BUFFERS AND BACKPLANE CLOCK DE-JITTERIZER
- AUTOMODE NT1 AND REPEATER
- "U ACTIVATION ONLY" IN NT1



PLCC44

ORDERING NUMBER: STLC5412FN



Plastic DIP28

ORDERING NUMBER: STLC5412P

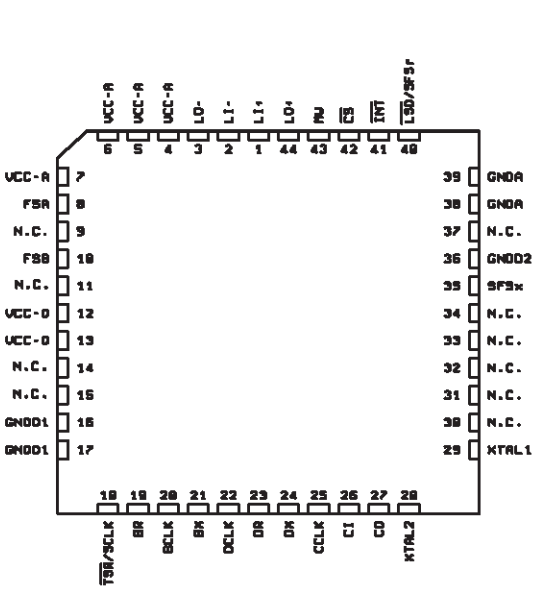
- IDENTIFICATION CODE AS PER GCI STANDARD
- DECT FRAME SYNCHRONIZATION
- EASILY INTERFACEABLE WITH ST5451 (HDLC & GCI CONTROLLER), STLC5464 / STLC5465 AND ANY OTHER GCI, IDL or TDM COMPATIBLE DEVICES

INDEX

PIN CONNECTIONS (Top view)

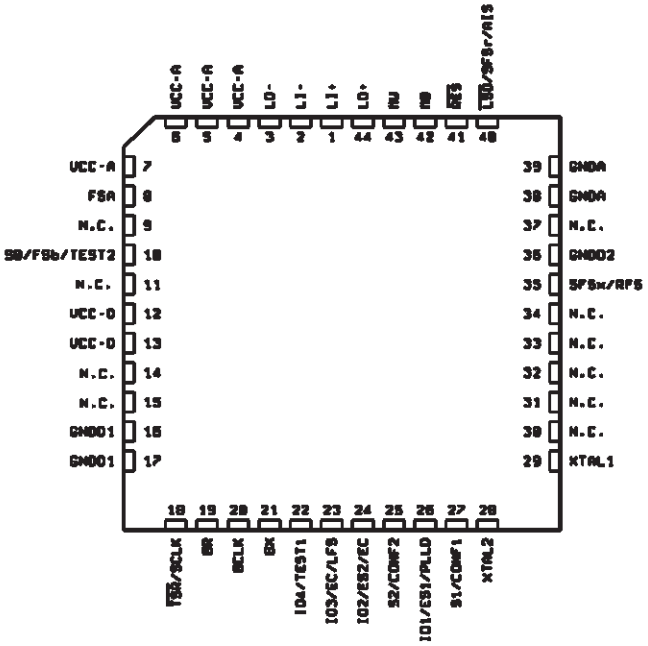
PLCC44

MICROWIRE MODE



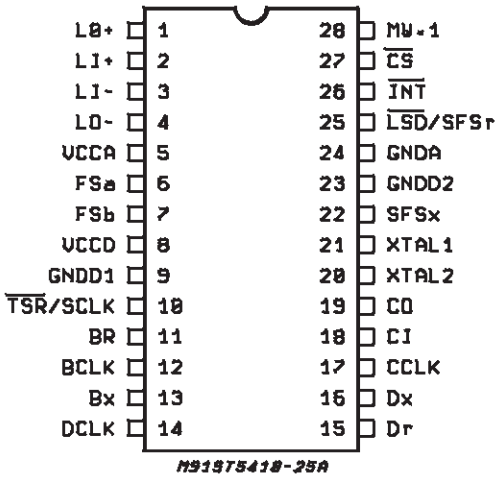
PLCC44

GCI MODE



DIP28

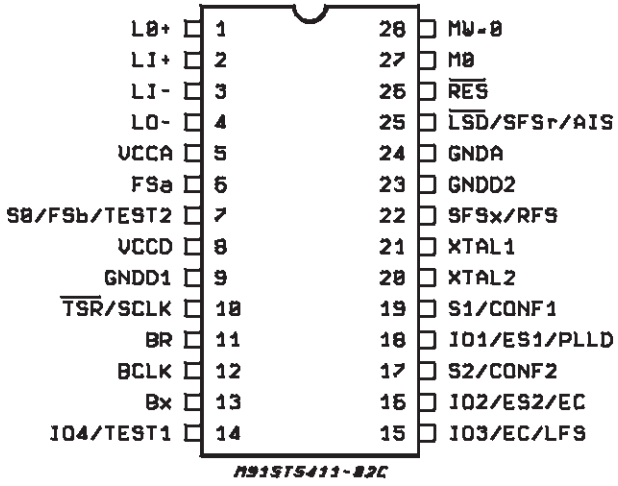
MICROWIRE MODE



M91ST5410-25A

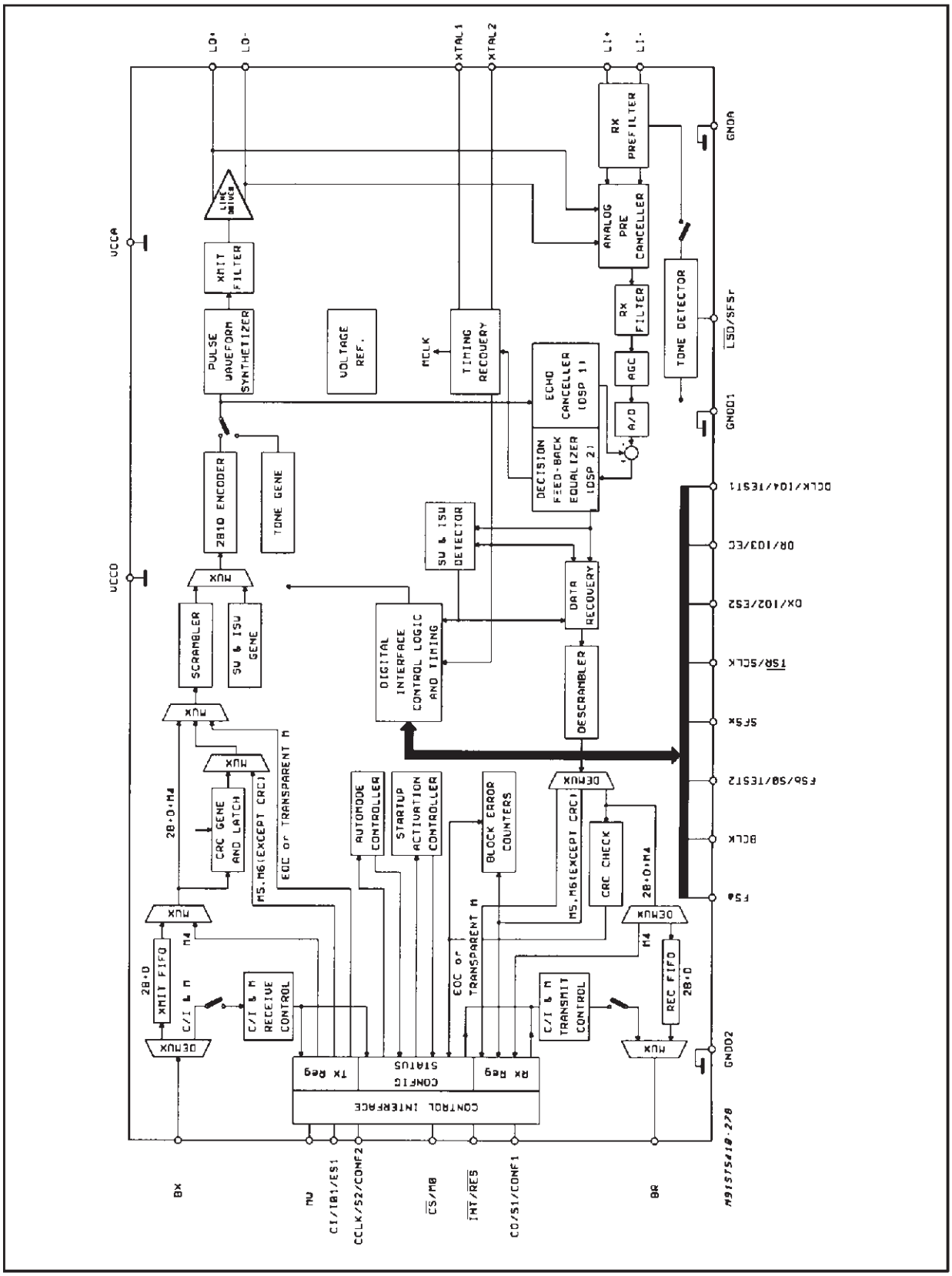
DIP28

GCI MODE



M91ST5411-B2C

Figure 1: Block Diagram.



GENERAL DESCRIPTION

STLC5412 is a complete monolithic transceiver for ISDN Basic access data transmission on twisted pair subscriber loops typical of public switched telephone networks. The device is fully compatible with ETSI ETRO80 and CSE (C32-11) French specifications.

The equivalent of 160 kbit/s full-duplex transmission on a single twisted pair is provided, according to the formats defined in the a.m. spec. Frames include two B channels, each of 64 kbit/s, one D channel of 16 kbit/s plus an additional 4 kbit/s M channel for loop maintenance and other user functions. 12 kbit/s bandwidth is reserved for framing. 2B1Q Line coding is used, where pairs of bits are coded into one of 4 quantum levels. This technique results in a low frequency spectrum (160 kbit/s turn into 80 kbaud), thereby reducing both line attenuation and crosstalk and achieving long range with low Bit Error Rates.

STLC5412 is designed to operate with Bit Error Rate near-end Crosstalk (NEXT) as specified in european ETSI recommendation.
To meet these very demanding specifications, the device includes two Digital Signal Processors, one configured as an adaptive Echo-Canceller to cancel the near end echoes resulting from the transmit/receive hybrid interface, the other as an adaptive line equalizer. A Digital Phase-Locked Loop (DPLL) timing recovery circuit is also included that provides in NT modes a 15.36 MHz synchronized clock to the system. Scrambling and descrambling are performed as specified in the specifications.

On the system side, STLC5412 can be linked to two bus configuration simply by pin MW bias.

MICROWIRE(μW/DSI) mode (MWpin = 5V): 144 kbit/s 2B+D basic access data is transferred on a multiplex Digital System Interface with 4 different interface formats (see fig. 2 and 3) providing maximum flexibility with a limited pin count (BCLK, Bx, Br, FSa, FSb). Three pre-defined 2B+D formats plus an internal time slot assigner allows direct connection of the UID to the most common multiplexed digital interfaces (TDM/IDL). Bit and Frame Synchronisation signals are inputs or outputs depending on the configuration selected. Data buffers allow any phase between the line and the digital interface. That permits building of slave-slave configurations e.g. in NT12 trunk-cards.

It is possible to separate the D from the B channels and to transfer it on a separate digital interface (Dx, Dr) using the same bit and frame clocks as for the B channels or in a continuous mode using an internally generated 16 kHz bit clock output (DCLK).

All the Control, Status and Interrupt registers are handled via a control channel on a separate serial interface MICROWIRE compatible (CI, CO, $\overline{CS}$, CCLK, $\overline{INT}$) supported by a number of microcontroller including the MCU families from SGS-THOMSON

GCI mode (MWpin = 0V). Control/maintenance channels are multiplexed with 2B+D basic access data in a GCI compatible interface format (see fig. 4a) requiring only 4 pins (BCLK, Bx, Br, FSa). On chip GCI channel assignement allows to multiplex on the same bus up to 8 GCI channels, each supporting data and controls of one device. Bit and Frame Synchronisation signals can be inputs or ouputs depending on the configuration selected. Data buffers, again, allow to have any phase between the line interface and the digital interface.

Through the M channel and its protocol allowing to check both direction exchanges, internal registers can be configured, the EOC channel and the Overhead-bits can be monitored. Associated to the M channel, there are A and E channels for enabling the exchanged messages and to check the flow control. The C/I channel allows the primitive exchanges following the standard protocol.

In both mode (μW and GCI) CRC is calculated and checked in both directions internally.
In LT mode, the transmit superframe can be synchronized by an external signal (SFSx) or be self running. In NT mode, the SFSx is always output synchronized by the transmit superframe.

Line side or Digital Interface side loopbacks can be selected for each B1, B2 or D channel independently without restriction in transparent or in non-transparent mode. A transparent complete analog loopback allowing the test of the transmission path is also selectable.

Activation and deactivation procedures, which are automatically processed by UID, require only the exchange of simple commands as Activation Request, Deactivation Request, Activation Indication. Cold and Warm start up procedures are operated automatically without any special instruction.

Four programmable I/Os are provided in GCI for external device control.

PIN FUNCTIONS (no Specific Microwire / GCI Mode)
Note: all pin number are referred to Plastic DIP28 package.

Pin	Name	In/Out	Description
1, 4	LO+, LO-	Out, Out	Transmit 2B1Q signal differential outputs to the line transformer. When used with an appropriate 1:1.5 step-up transformer and the proper line interface circuit the line signal conforms to the output specifications in ANSI standard with a nominal pulse amplitude of 2.5 Volts.
2, 3	LI+, LI-	In, In	Receive 2B1Q signal differential inputs from the line transformer.
5, 8	VCCA, VCCD	In, In	Positive power supply input for the analog and digital sections, which must be +5 Volts +/-5% and must be directly connected together.
24, 9 23	GNDA,GNDD1 GNDD2	In, In In	Negative power supply pins, which must be connected together close to the device. All digital and analog signals are referred to these pins, which are normally at the system Ground.
10	$\overline{TSR}$	Out	(LT configuration only) This pin is an open drain output normally in the high impedance state which pulls low when B1 and B2 time-slots are active. It can be used to enable the Tristate control of a backplane line-driver.
	SCLK	Out	(NT configuration only) 15.36 MHz clock output which is frequency locked to the received line signal active as soon as UID is powered up except in NT1 Auto configuration (active only if S line activation is requested)
20	XTAL2	Out	The output of the crystal oscillator, which should be connected to one end of the crystal, if used. Otherwise, this pin must be left not connected.
21	XTAL1	In	The master clock input, which requires either a parallel resonance crystal to be tied between this pin and XTAL2, or a logic level clock input from a stable source. This clock does not need to be synchronized to the digital interface clocks (FSa, BCLK).Crystal specifications: 15.36 MHz +/-50ppm parallel resonant; Rs $\leq$ 20 ohms; load with 33pF to GND each side.
28	MW	In	MICROWIRE selection: When set high, MICROWIRE control interface is selected. When set low, GCI interface is selected.

PIN FUNCTIONS (specific Micro Wire mode)

Pin	Name	In/Out	Description
6	FSa	In Out	Input or Output depending of the CMS bit in CR1 register, FSa is a 8 KHz clock which indicates the start of the frame on Bx when FSa is input, or Bx and Br when FSa is output. Input or Output, the location of FSa relative to the frame on Bx or Bx and Br depends of DDM bit in CR1 register, also the selected format.
7	FSb	In Out	Input or Output depending of the CMS bit in CR1 register, FSb is a 8 KHz clock which indicates the start of the frame on Br when it is an input. When it is an output, FSb is a 8 KHz pulse conforming with the selected format and always indicating the second 64Kbit/sec channel of the frame on Br. Input or Output, the location of FSb relative to the frame on Br depends of DDM bit in CR1 register, also the selected format.
11	Br	Out	2B+D datas tristate output. Datas received from the line are shifted out on the rising edge (at the BCLK frequency or the half BCLK frequency if format 4 is selected) during the assigned time slot. Br is in high impedance state outside the assigned time slot and during the assigned time slot of the channel if it is disabled. When D channel port is enabled, only B1 B2 are on Br.

PIN FUNCTIONS (specific Micro Wire mode)

Pin	Name	In/Out	Description
12	BCLK	In Out	Bit clock input or output depending of the CMS bit in CMR register. When BCLK is an input, its frequency may be any multiple of 8 KHz from 256 KHz to 4096 KHz in formats 1, 2, 3; 512 KHz to 6176 KHz in format 4. When BCLK is an output, its frequency is 256 KHz, 512 KHz, 1536 KHz, 2048 KHz or 2560 KHz depending of the selection in CR1 register. In this case, BCLK is locked to the recovered clock received from the line. Input or Output BCLK is synchronous with FSa/FSb. Datas are shifted in and out (on Bx and Br) at the BCLK frequency in formats 1, 2, 3. In format 4 datas are shifted out at half the BCLK frequency.
13	Bx	In	2B+D input. Basic access data to transmit to the line is shifted in on the falling edges (at the BCLK frequency or the half BCLK frequency if format 4 is selected) during the assigned time-slots. When D channel port is enabled, only B1 & B2 sampled on Bx.
14	DCLK	Out	D channel clock output when the D channel port is enabled in continuous mode. Datas are shifted in and out (on Dx and Dr) at 16 KHz on the falling and rising edges of DCLK respectively. In master mode, DCLK is synchronous with BCLK.
15	Dr	Out	D channel data output when the D channel port is enabled. D channel data is shifted out from the UID on this pin in 2 selectable modes: in TDM mode data is shifted out at the BCLK frequency (or half BCLK frequency in format 4) on the ridsing edges when the assigned time slot is active. In continuous mode data is shifted in at the DCLK frequency on the rising edge continuously.
16	Dx	In	D channel data input when the D channel port is enabled. D channel data is shifted in from the UID on this pin in 2 selectable modes: in TDM mode data is shifted in at the BCLK frequency (or half BCLK frequency in format 4) on the falling edges when the assigned time slot is active. In continuous mode data is shifted in at the DCLK frequency on the falling edge continuously.
17	CCLK	In	Clock input for the MICROWIRE control channel: data is shifted in and out on CI and CO pins with CCLK frequency following 2 modes. For each mode the CCLK polarity is indifferent. CCLK may be asynchronous with all the others UID clocks.
18	CI	In	MICROWIRE control channel serial input: Two bytes data is shifted in the UID on this pin on the rising or the falling edge of CCLK depending of the working mode.
19	CO	Out	MICROWIRE control channel serial output: two bytes data is shifted out the UID on this pin on the rising or the falling edge of CCLK depending of the working mode. When not enabled by $\overline{CS}$ low, CO is high impedance.
22	SFSx	In Out	Tx Super frame synchronization. The rising edge of SFSx indicates the beginning of the transmit superframe on the line. In NT mode SFSx is always an output. In LT mode SFSx is an input or an output depending of the SFS bit in CR2 register. When SFSx is input, it must be synchronous of FSa. In DECT mode this pin is always an input in LT configuration and is used to evaluate the round trip delay, in NT configuration is an output used to resynchronise the DECT frame counter.(refer to page 25)
25	SFSr	Out	Rx Super frame synchronization. The rising edge of SFSr indicates the beginning of the received superframe on the line. UID provides this output only when ESFR bit in CR4 register is set to 1.
	$\overline{LSD}$	Out	Line Signal Detect output (default configuration): This pin is an open drain output which is normally in the high impedance state but pulls low when the device previously in the power down state receives a wake-up by Tone from the line. This signal is intended to be used to wake-up a micro-controller from a low power idle mode. The $\overline{LSD}$ output goes back in the high impedance state when the device is powered up.
26	$\overline{INT}$	Out	Interrupt output: Latched open-drain output signal which is normally high impedance and goes low to request a read cycle. Pending interrupt data is shifted out from CO at the following read-write cycle. Several pending interrupts may be queued internally and may provide several interrupt requests. $\overline{INT}$ is freed upon receiving of $\overline{CS}$ low and can go low again when $\overline{CS}$ is freed.
27	$\overline{CS}$	In	Chip Select input: When this pin is pulled low, data can be shifted in and out from the UID through CI & CO pins. When high, this pin inhibits the MICROWIRE interface. For normal read or write operation, $\overline{CS}$ has to be pulled low for 16 CCLK periods.

PIN FUNCTIONS (specific GCI mode)

Pin	Name	In/Out	Description
6	FSa	In Out	Input or Output depending of the configuration. FSa is a 8 KHz clock which indicates the start of the frame on Bx and Br.
7	FSb	Out	In NT/TE non auto-mode configuration, FSb is a 8 KHz pulse always indicating the second 64Kbit/sec channel of the frame on Br.
	S0	In	When MO = 0 (LT/NT12 configuration): S0 associated with S1 and S2 selects a GCI channel number on Bx/Br.
	TEST2	In	Input pin to select a transmission test in all auto mode configurations. TEST2 is associated with TEST1.
11	Br	Out	2B+D and GCI control channel open drain output. Data is shifted out (at the half BCLK frequency) on the first rising edge of BCLK during the assigned channels slot. Br is in high impedance state outside the assigned time slot and during the assigned time slot of a channel if it is disabled.
12	BCLK	In Out	Bit clock input or output depending of the configuration. When BCLK is an input, its frequency may be any multiple of 16 KHz from 512 KHz to 6176 KHz.. When BCLK is an output, its frequency is 512 KHz in NT1 auto and NTRR auto configurations, 1536 KHz in NT/TE configuration; In this case, BCLK is locked to the recovered clock received from the line. Input or Output BCLK is synchronous with FSa. Data are shifted in and out (on Bx and Br) at half the BCLK frequency.
13	Bx	In	2B+D and GCI control channel input. Data is sampled by the UID on the second falling edge of BCLK within the period of the bit, during the assigned channels time slot.
14	IO4	In Out	General purpose programmable I/O configured by CR5 register in all non auto mode configurations.
	TEST1	In	Input pin to select a transmission test in all auto mode configurations. TEST1 is associated with TEST2.
15	IO3	In Out	General purpose programmable I/O configured by CR5 register in all non auto mode configurations.
	EC	Out	External control output pin in NT1 auto configuration. Normaly high, this pin is pulled low when an eoc message ”operate 2B+D loopback” is recognized from the line.
	LFS	In	Local febe select: When tied to 1 the febe is locally looped back. See figure 10.
16	IO2	In, Out	General purpose programmable I/O configured by CR5 register in all non auto mode configurations.
	EC	Out	External control output pin in LTRR auto configuration. Normaly high, this pin is pulled low when an ARL command is received by the UID.
	ES2	In	External status input pin. In NT1 auto and NTRR auto configurations, this status is sent on the line through the ps2 bit.
17	S2	In	When MO = 0 (LT/NT12 configuration): S2 associated with S0 and S1 selects a GCI channel number on Bx/Br.
	CONF2	In	When MO = 1: Configuration input pin. Is used associated with CONF1 to select configuration NT/TE (non auto), NT1 auto, LTRR auto and NTRR auto.
18	IO1	In Out	General purpose programmable I/O configured by CR5 register in all non auto mode configurations.
	ES1	In	External status input pin. In NT1 auto and NTRR auto configurations, this status is sent on the line through the ps1 bit.
	PLLD	In	PLL1 can be disabled in LTRR configuration with this pin.
19	S1	In	When MO = 0 (LT/NT12 configuration): S1 associated with S0 and S2 selects a GCI channel number on Bx/Br.
	CONF1	In	When MO = 1: Configuration input pin. Is used associated with CONF2 to select configuration NT/TE (non auto), NT1 auto, LTRR auto and NTRR auto.

PIN FUNCTIONS (specific GCI mode)

Pin	Name	In/Out	Description
22	RFS	In	Remote febe select: When tied to 0 the remote febe is not transferred. When tied to 1 febe is transparently reported. See figure 10.
	SFSx	In Out	Tx Super frame synchronization. In LT mode this pin is an input giving the Tx Super Frame Synchronization if SFS = 0 in CR2. It becomes an output if SFS = 1 with ISW free running on the line. In NT mode this pin is always an output giving the Tx Super Frame position. If DECT mode is selected (DECT = 1 in CR7) this pin provide the DECT synchronization pulse at each validated reception of the DECT eoc message.
25	AIS	In	Analog interface select for all auto mode configurations
	SFSr	Out	Rx Super frame synchronization. The rising edge of SFSr indicates the beginning of the received superframe on the line. UID provides this output only when ESFR bit in CR4 register is to 1 and LT/NT12 or NT/TE configuration is done.
	$\overline{\text{LSD}}$	Out	Line Signal Detect output (default configuration): This pin is an open drain output which is normally in the high impedance state but pulls low when the device previously in the power down state receives a wake-up by Tone from the line. This signal is intended to be used to wake-up a micro-controller from a low power idle mode. The LSD output goes back in the high impedance state when the device is powered up.
26	$\overline{\text{RES}}$	In	Reset input pin with internal pull-up resistor. When pulled low, all registers of the UID are reset to their default values. UID is configured according to configuration inputs bias excluding MW input which must be maintained at the 0 volt. minimum recommended pulse length is 200µs.
27	M0	In	Configuration input pin. When pulled low, GCI channel assigner is selected (channel number defined by inputs S0, S1, S2). When pulled high, UID is configured by pins CONF1 and CONF2.

MULTIPLE FUNCTION PIN DESCRIPTION

Pin 6: FSa

Function or In/Out conditions				Function	In/Out
MW(pin) = 1		CMS(cr1) = 1		FSa	Out
		CMS(cr1) = 0		FSa	In
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1		FSa	Out
		CONF2(pin) = 0	CONF1(pin) = 1	FSa	In
			CONF1(pin) = 0	FSa	Out
	MO(pin) = 0			FSa	In

MULTIPLE FUNCTION PIN DESCRIPTION

Pin 7: S0/FSb/TEST2

Function or In/Out conditions				Function	In/Out
MW(pin) = 1		CMS(cr1) = 1		FSb	Out
		CMS(cr1) = 0		FSb	In
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1	CONF1(pin) = 1	TEST2	In
			CONF1(pin) = 0	FSb	Out
		CONF2(pin) = 0		TEST2	In
	MO(pin) = 0			S0	In

Pin 10: $\overline{\text{TSR}}$/SCLK/TCLK

Function or In/Out conditions				Function	In/Out
MW(pin) = 1		NTS(cr2) = 1		SCLK	Out
		NTS(cr2) = 0		$\overline{\text{TSR}}$	Out OD
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1		SCLK	Out
		CONF2(pin) = 0	CONF1(pin) = 1	$\overline{\text{TSR}}$	Out OD
			CONF1(pin) = 0	SCLK	Out
	MO(pin) = 0	NTS(cr2) = 1		SCLK	Out
		NTS(cr2) = 0		$\overline{\text{TSR}}$	Out OD

Pin 12: BCLK

Function or In/Out conditions				Function	In/Out
MW(pin) = 1		CMS(cr1) = 1		BCLK	Out
		CMS(cr1) = 0		BCLK	In
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1		BCLK	Out
		CONF2(pin) = 0	CONF1(pin) = 1	BCLK	In
			CONF1(pin) = 0	BCLK	Out
	MO(pin) = 0			BCLK	In

MULTIPLE FUNCTION PIN DESCRIPTION

Pin 14: DCLK/IO4/TEST1 with pull up resistor

Function or In/Out conditions					Function	In/Out
MW(pin) = 1		DEN(cr2) = 1	DMO(cr2) = 1		DCLK	Out
			DMO(cr2) = 0		reserved	reserved
		DEN(cr2) = 0			reserved	reserved
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1	CONF1(pin) = 1		TEST1	In
			CONF1(pin) = 0	IO4(cr5) = 1	I4	In
				IO4(cr5) = 0	O4	Out
		CONF2(pin) = 0			TEST1	In
	MO(pin) = 0			IO4(cr5) = 1	I4	In
				IO4(cr5) = 0	O4	Out

Pin 15: Dr/IO3/EC/LFS with pull up resistor

Function or In/Out conditions					Function	In/Out
MW(pin) = 1		DEN(cr2) = 1			Dr	Out
		DEN(cr2) = 0			reserved	reserved
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1	CONF1(pin) = 1		EC	Out
			CONF1(pin) = 0	IO3(cr5) = 1	I3	In
				IO3(cr5) = 0	O3	Out
		CONF2(pin) = 0			LFS	In
	MO(pin) = 0			IO3(cr5) = 1	I3	In
				IO3(cr5) = 0	O3	Out

Pin 16: Dx/IO2/EC/ES2 with pull up resistor

Function or In/Out conditions					Function	In/Out
MW(pin) = 1		DEN(cr2) = 1			Dx	In
		DEN(cr2) = 0			reserved	reserved
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1	CONF1(pin) = 1		ES2	In
			CONF1(pin) = 0	IO2(cr5) = 1	I2	In
				IO2(cr5) = 0	O2	Out
		CONF2(pin) = 0	CONF1(pin) = 1		EC	Out
			CONF1(pin) = 0		ES2	In
	MO(pin) = 0			IO2(cr5) = 1	I2	In
				IO2(cr5) = 0	O2	Out

MULTIPLE FUNCTION PIN DESCRIPTION

Pin 17: CCLK/S2/CONF2

Function or In/Out conditions					Function	In/Out
MW(pin) = 1					CCLK	In
MW(pin) = 0	MO(pin) = 1				CONF2	In
	MO(pin) = 0				S2	In

Pin 18: CI/IO1/ES1/PLLDwith pull up resistor

Function or In/Out conditions					Function	In/Out
MW(pin) = 1					CI	In
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1	CONF1(pin) = 1		ES1	In
			CONF1(pin) = 0	IO1(cr5) = 1	I1	In
				IO1(cr5) = 0	O1	Out
		CONF2(pin) = 0	CONF1(pin) = 1		PLLD	In
			CONF1(pin) = 0		ES1	In
	MO(pin) = 0			IO1(cr5) = 1	I1	In
				IO1(cr5) = 0	O1	Out

Pin 19: CO/S1/CONF1

Function or In/Out conditions					Function	In/Out
MW(pin) = 1					CO	Out
MW(pin) = 0	MO(pin) = 1				CONF1	In
	MO(pin) = 0				S2	In

Pin 22: SFSx/RFS with pull up resistor

Function or In/Out conditions					Function	In/Out
MW(pin) = 1		NTS(cr2) = 1			SFSx	Out
		NTS(cr2) = 0	SFS(cr2) = 1		SFSx	Out
			SFS(cr2) = 0		SFSx	In
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1			SFSx	Out
		CONF2(pin) = 0			RFS	In
	MO(pin) = 0	NTS(cr2) = 1			SFSx	Out
		NTS(cr2) = 0	SFS(cr2) = 1		SFSx	Out
			SFS(cr2) = 0		SFSx	In

MULTIPLE FUNCTION PIN DESCRIPTION

Pin 25: $\overline{\text{LSD}}$/SFSr/AIS

Function or In/Out conditions					Function	In/Out
MW(pin) = 1				ESFR(cr4) = 1	SFSr	Out OD
				ESFR(cr4) = 0	$\overline{\text{LSD}}$	Out OD
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1	CONF1(pin) = 1		AIS	In
			CONF1(pin) = 0	ESFR(cr4) = 1	SFSr	Out OD
				ESFR(cr4) = 0	$\overline{\text{LSD}}$	Out OD
		CONF2(pin) = 0			AIS	In
	MO(pin) = 0			ESFR(cr4) = 1	SFSr	Out OD
				ESFR(cr4) = 0	$\overline{\text{LSD}}$	Out OD

Pin 26: $\overline{\text{INT}}$/$\overline{\text{RES}}$ with pull up resistor

Function or In/Out conditions					Function	In/Out
MW(pin) = 1					$\overline{\text{INT}}$	Out OD
MW(pin) = 0					$\overline{\text{RES}}$	In

Pin 27: $\overline{\text{CS}}$/MO

Function or In/Out conditions					Function	In/Out
MW(pin) = 1					$\overline{\text{CS}}$	In
MW(pin) = 0					MO	In

Notes: Out OD = Open Drain Output

FUNCTIONAL DESCRIPTION

Digital Interfaces

STLC5412 provides a choice between two types of digital interface for both control data and (2 B+D) basic access data.

These are:

a) General Circuit Interface: GCI.

b) Microwire/Digital System Interface: µW/DSI

The device will automatically switch to one of them by sensing the MW input pin at the Power up.

µW/DSI MODE

Microwire control interface

The MICROWIRE interface is enabled when pin MW equal one. Internal registers can be written or read through that control interface.
It is constituted of 5 pins:

CI:	data input
CO:	data output
CCLK:	data clock input
$\overline{CS}$:	Chip Select input
$\overline{INT}$:	Interrupt output

Transmission of data onto CI & CO is enabled when $\overline{CS}$ input is low.

A Write cycle or a Read cycle is always constituted of two bytes. CCLK must be pulsed 16 times while $\overline{CS}$ is low.

Transmission of data onto CI & CO is enabled following 2 modes.

- MODE A: the first CCLK edge after $\overline{CS}$ falling edge (and fifteen others odd CCLK edges) are used to shift in the CI data, the even edges being used to shift out the CO data.
- MODE B: the CCLK first edge after $\overline{CS}$ falling edge (and the fifteen others odd CCLK edges) are used to shift out the CO data, the even edges being used to shift in the CI data.

For each mode the first CCLK edge after $\overline{CS}$ falling edge can be positive or negative: the UID automaticaly detects the CCLK polarity.
Mode A is the default value. To select the mode B, write MWPS register.

You can write in the UID on CI while the UID send back a register content to the microprocessor. If the UID has no message to send, it forces the CO output to all zero's.

If the UID is to be read (status change has occured in the UID or a read-back cycle has been requested by the controller), it pulls the $\overline{INT}$ output low until $\overline{CS}$ is provided. $\overline{INT}$ high to low transition is not allowed when $\overline{CS}$ is low (the UID waits for $\overline{CS}$ high if a pending interrupt occurs while $\overline{CS}$ is low) .

When $\overline{CS}$ is high, the CO pin is in the high impedance state.

Write cycle

The format to write a 8 bits message into the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Address
A0: Write/Read back Indicator
D7-D0: Register Content

After the first byte is shifted in, Register address is decoded. A0 set low indicates a write cycle: the content of the following received byte has to be loaded into the addressed register.
A0 set high indicates a read-back cycle request and the byte following is not significant. The UID will respond to the request with an interrupt cycle. It is then possible for the microprocessor to receive the required register content after several other pending interrupts.

To write a 12bits message, the difference is:
limited address field: A7 - A4
extended data field (D11 - D8): A3 - A0.
The Write/Read back indicator doesn't apply; to read and write a 12 bits register two addresses are necessary.

Read cycle

When UID has a register content to send to the microprocessor, it pulls low the $\overline{INT}$ output to request $\overline{CS}$ and CCLK signals. Note that the data to send can be the content of a Register previously requested by the microprocessor by means of a read-back request.

The format of the 8 bits message sent by the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Address
A0: forced to 1 if read back
forced to 0 if spontaneous
D7-D0: Register Content

To read a 12 bits message, the difference is:
limited address field: A7 - A4
extended data field (D11 - D8): A3 - A0.
The Write/Read back indicator doesn't exit.

DIGITAL SYSTEM INTERFACE

Two B channels, each at 64 kbit/s and one D channel at 16 kbit/s form the Basic access data. Basic access data is transferred on the Digital System Interface with several different formats selectable by means of the configuration register CR1.
The DSI is basically constituted of 5 wires (see fig.2 and 3):

BCLK	bit clock
Bx	data input to transmit to the line
Br	data output received from the line
FSa	Transmit Frame sync
FSb	Receive Frame sync

It is possible to separate the D channel from the B channels and to transfer it on a separate Digital Interface constituted of 2 pins:

Dx	D channel data input
Dr	D channel data ouput

The TDM (Time Division Multiplex) mode uses the same bit and frame clocks as for the B channels. The continuous mode uses an internally generated 16 kHz bit clock output:

DCLK	D channel clock output

For all formats when D channel port is enabled "continuous mode" is possible. When the D channel port is enabled in TDM mode, D bits are assigned according to the related format on Dx and Dr .

STLC5412 provides a choice of four multiplexed formats for the B and D channels data as shown in fig.2 and 3.

Format 1: the 2B+D data transfer is assigned to the first 18 bits of the frame on Br and Bx I/0 pins. Channels are assigned as follows: B1(8 bits), B2(8 bits), D(2 bits), with the remaining bits ignored until the next Frame sync pulse.

Format 2: the 2B+D data transfer is assigned to the first 19 bits of the frame on Br and Bx I/O pins. Channels are assigned as follows: B1(8 bits), D(1 bit), 1 bit ignored, B2(8 bits), D(1 bit), with the remaining bits ignored until the next frame sync pulse.

Format 3: B1 and B2 Channels can be independently assigned to any 8 bits wide time slot among 64 (or less) on the Bx and Br pins. The transmit and receive directions are also independent. When TDM mode is selected, the D channel can be assigned to any 2 bits wide time slot among 256 on the Bx and Br pins or on the Dx and Dr pins (D port disabled or enabled in TDM mode respectively).

Format 4: is a GCI like format excluding Monitor channel and C/I channel. The 2B+D data transfer is assigned to the first 26 bits of the frame on Br and Bx I/O pins. Channels are assigned as follows. B1(8 bits) B2(8 bits), 8 bits ignored, D(2 bits), with remaining bits ignored up to the next frame sync pulse.

When the Digital Interface clocks are selected as inputs, FSa must be a 8 kHz clock input which indicates the start of the frame on the data input pin Bx. When the Digital Interface clocks are selected as outputs, FSa is an 8 kHz output pulse conforming to the selected format which indicates the frame beginning for both Tx and Rx directions.

When the Digital Interface clocks are selected as inputs, FSb is a 8 kHz clock input which defines the start of the frame on the data ouput pin Br. When the Digital Interface clocks are selected as outputs, FSb is a 8 kHz output pulse indicating the second 64kbit/s slot.

Two phase-relations between the rising edge of FSa/FSb and the first (or second for FSb as output) slot of the frame can be selected depending on format selected: Delayed timing mode or non Delayed timing mode.

Non delayed data mode is similar to long frame timing on the COMBOI/II series of devices: The first bit of the frame begins nominally coincident with the rising edge of FSa/b. When output, FSa is coincident with the first 8 bits wide time-slot while FSb is coincident with the second 8 bits wide time-slot. Non delayed mode is not available in format 2.

Delayed timing mode, which is similar to short frame sync timing on COMBO I/II, in which the FSa/b input must be set high at least a half cycle of BCLK earlier the frame beginning. When output, FSa 1bit wide pulse indicates the first 8 bits wide time-slot while FSb indicates the second. Delayed mode is not available in format 4.

2B+D basic access data to transmit to the line can be shifted in at the BCLK frequency on the falling edges during the assigned time-slots. When D channel port is enabled, only B1 & B2 data is shifted in during the assigned time slots. In format 4, data is shifted in at half the BCLK frequency on the receive falling edges.

2B+ D basic access data received from the line can be shifted out from the Br output at the BCLK frequency on the rising edges during the assigned time-slots. Elsewhere, Br is in the high impedance state. When the D channel port is enabled, only B1 & B2 data is shifted out from Br. In Format 4, data is shifted out at half the BCLK frequency on the transmit rising edges; there is 1.5 period delay between the rising transmit edge and the receive falling edge of BCLK.

Bit Clock BCLK determines the data shift rate on the Digital Interface. Depending on mode selected, BCLK is an input which may be any multiple of 8 kHz from 256 kHz to 6176 kHz or an output at a frequency depending on the format and the frequency selected. Possible frequencies are:
256 KHz, 512 KHz, 1536 KHz,
2048 KHz, 2560 KHz.

In format 4 the use of 256kHz is forbidden.

BCLK is synchronous with FSa/b frame sync signal. When output, BCLK is phased locked to the recovered clock received from the line.

Figure 2: DSI Interface formats: MASTER mode.

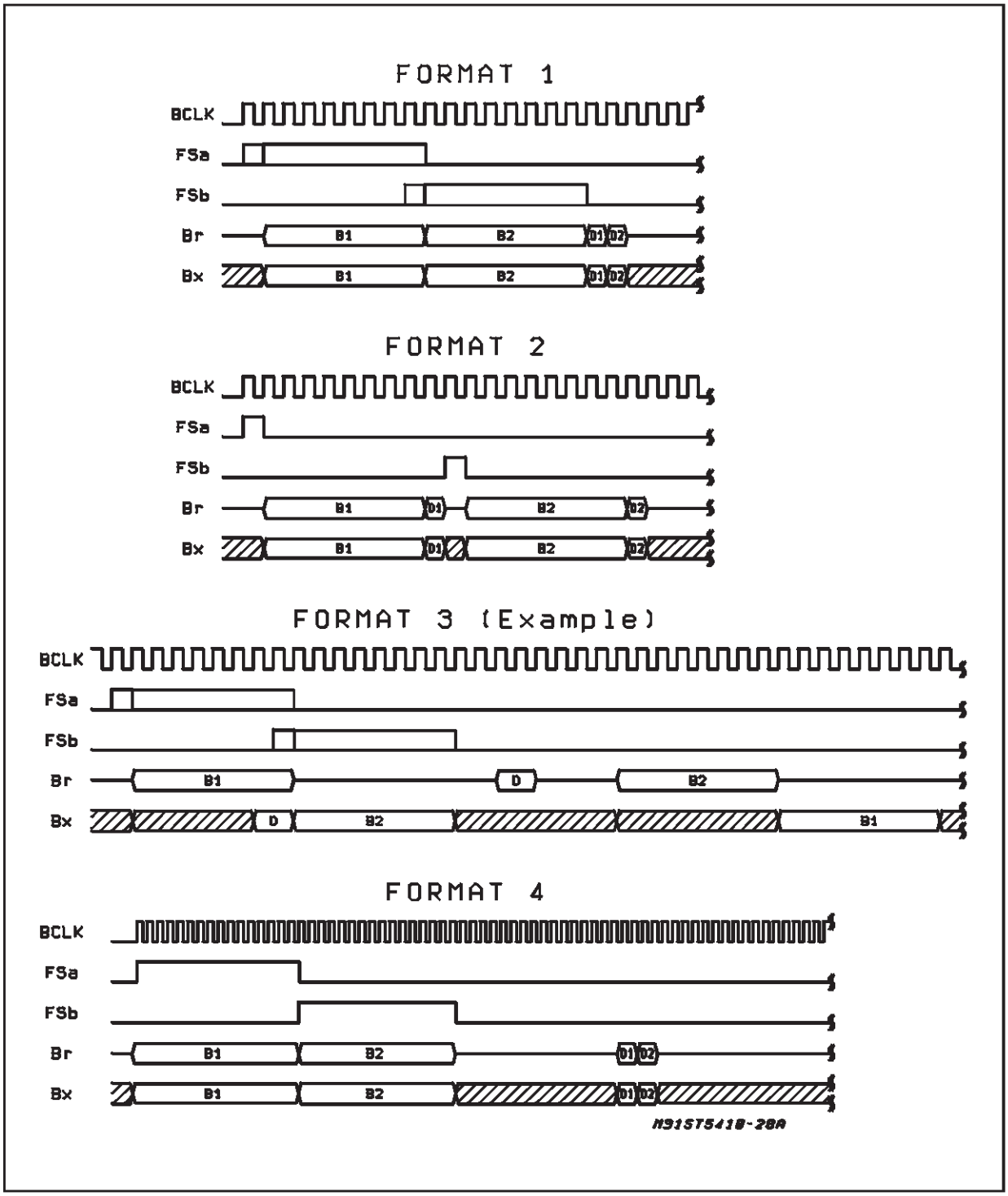
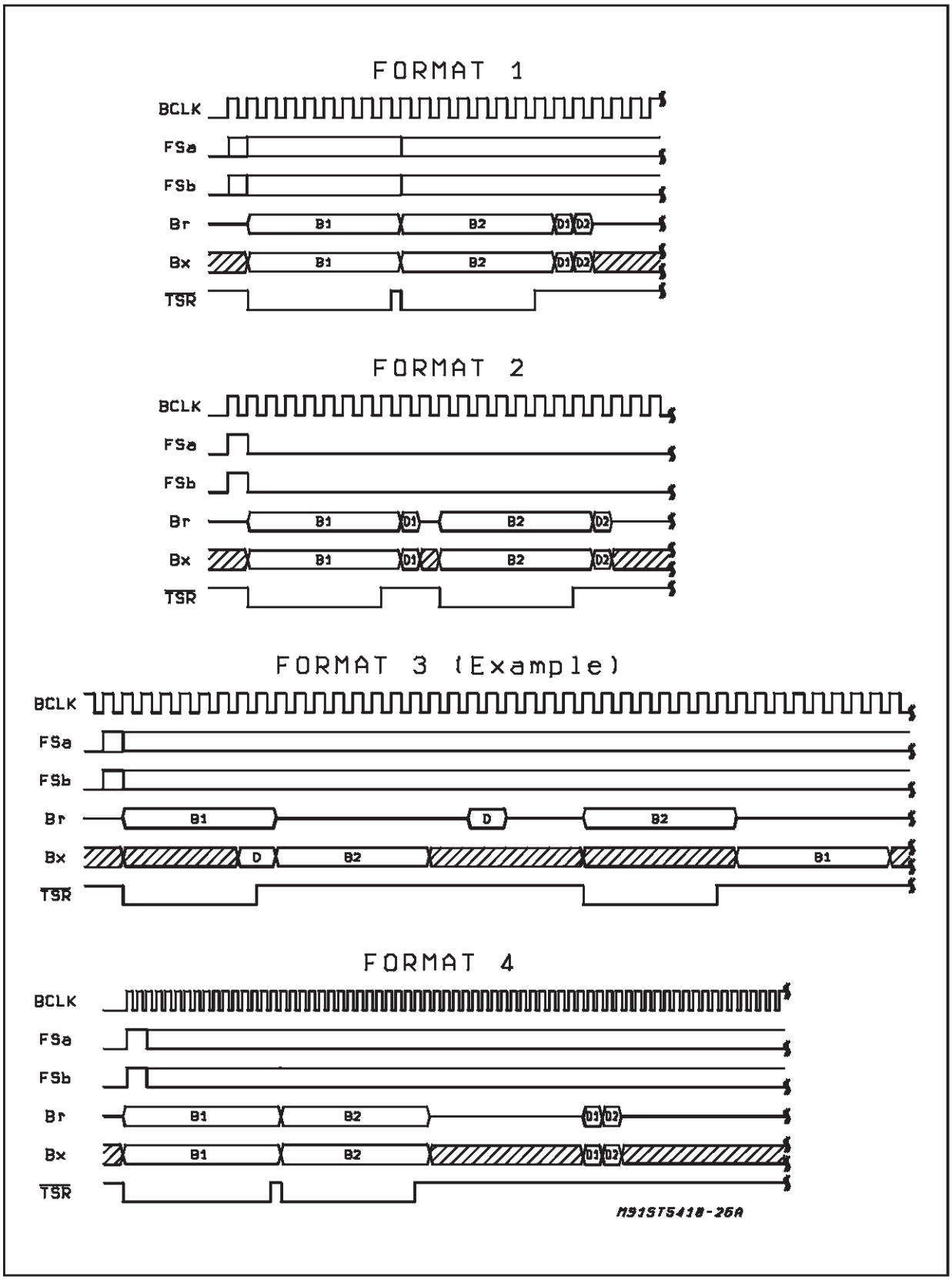


Figure 3: DSI Interface formats: SLAVE mode.



GCI MODE

The GCI is a standard interface for the interconnection of dedicated ISDN components in the different equipments of the subscriber loop :
In a Terminal, GCI interlinks the STLC5412, the ISDN layer 2 (LAPD) controller and the voice/data processing components as an audio-processor or a Terminal Adaptor module.

In NT1-2, PABX subscriber line card, or central office line card (LT), GCI interlinks the UID, the ISDN Layer 2 (LAPD) controllers and eventually the backplane where the channels are multiplexed.

In NT1, GCI interlinks SID-GCI and STLC5412, via automode (NT1-auto). In Regenerators, GCI links both STLC5412 UID in automode (NT-RR-auto, LT-RR-auto). (See Fig. 4a)

Frame Structure

2B+D data and control interface is transferred in a time-division multiplexed mode based on 8 kHz frame structure and assigned to four octets per frame and direction.(see fig.4b).

The 64 kbit/s channels B1 and B2 are conveyed in the first two octets; the third octet (M: Monitor) is used for transferring most of the control and status registers; the fourth octet (SC: Signalling & Control) contains the two D channel bits, the four C/I (command/Indicate) bits controlling the activation/deactivation procedures, and the E & A bits which support the handling of the Monitor channel.

These four octets per frame serving one ISDN subscribers line form a GCI Channel. One GCI channel calls for a bit rate of 256 kbit/s.

In NT1-2s or subscriber Line Cards up to 8 GCI channels may be carried in a frame of a GCI multiplex. The bit rate of a GCI multiplex may be from 256 kbit/s and up to 3088 kbit/s. Adjacent 4-octet slots from the frame start are numbered 0 to 7. The GCI channel takes the number of the slot it occupies. Spare bits in the frame beyond 256 bits from the frame start will be ignored by GCI compatible devices but may be used for other purposes if required (see Fig.4c). GCI channel number is selected by biasing pins S0,S1,S2.

Physical Links

Four physical links are used in the GCI.

Transmitted data to the line: Bx
Received data from the line: Br
Data clock: BCLK
Frame Synchronization clock: FSa

GCI is always synchronized by frame and data clocks derived by any master clock source.

A device used in NT mode can deliver clock sources able to synchronize GCI, either directly, or via a local Clock Generator synchronized on the line by means of the SCLK 15.36 MHz output clock. Frame clock and data clock could be independent of the internal devices clocks. Logical one on the Br output is the high impedance state while logical zero is low voltage. For E and A bits, active state is voltage Low while inactive state is high impedance state.

Figure 4a: GCI configurations of the UID.

Figure 4a: GCI configurations of the UID

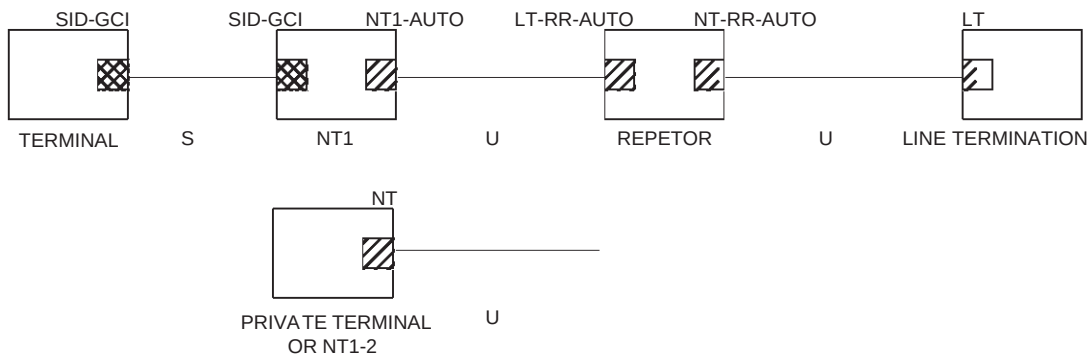


Figure 4b: GCI interface format.

Figure 4b: GCI interface format

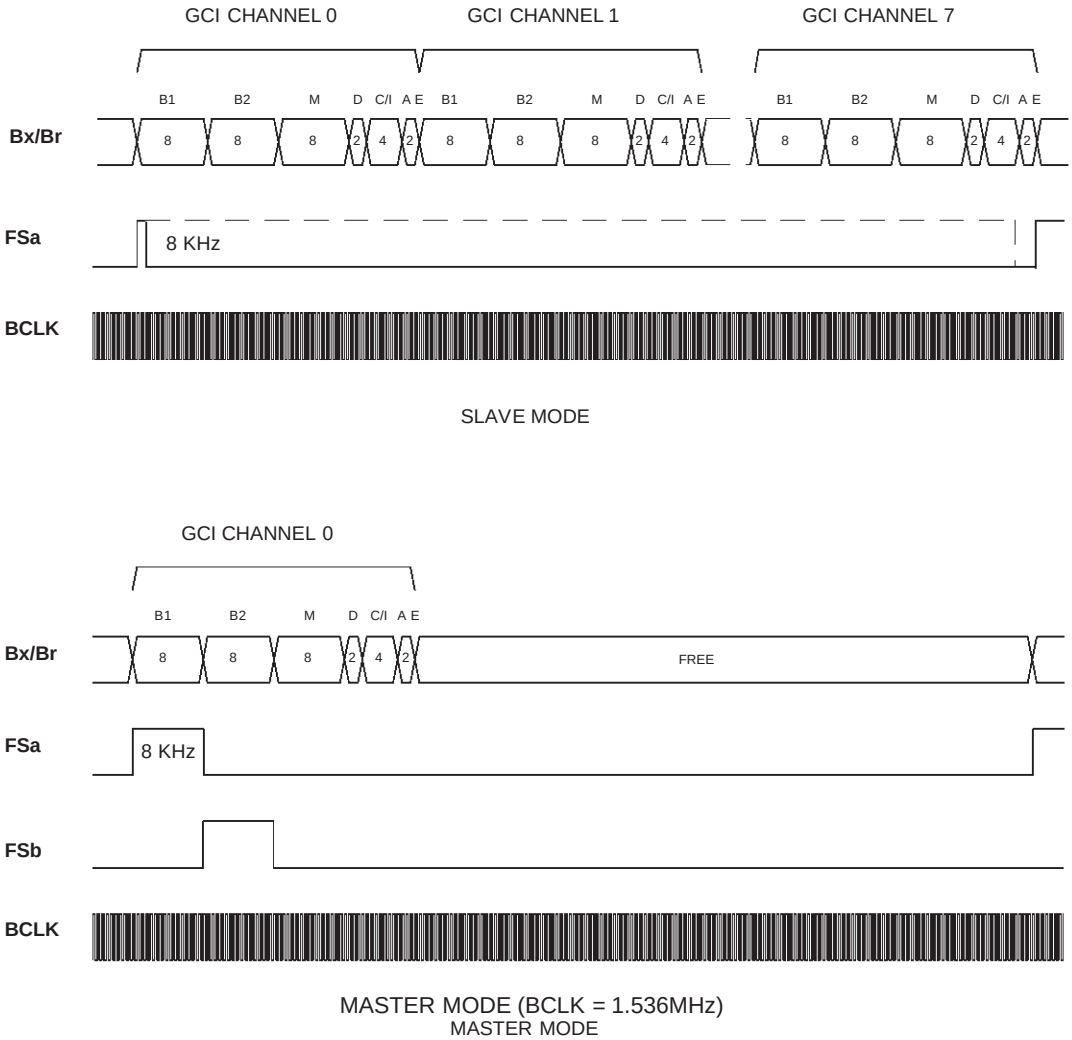
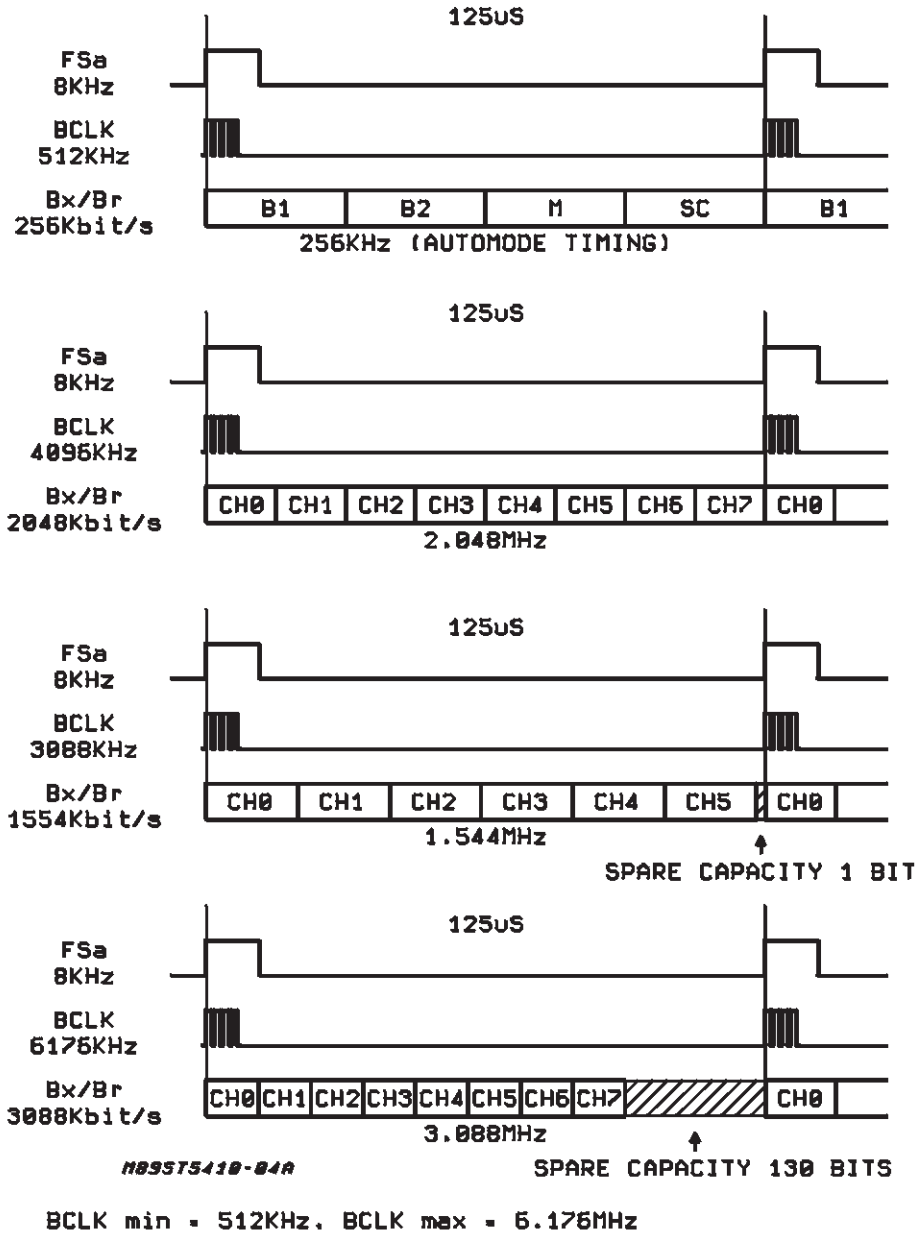


Figure 4c: GCI multiplex examples, (slave mode).



Data is transmitted in both directions at half the data clock rate. The information is clocked by the transmitter on the front edge of the data clock and can be accepted by the receiver after 1 to 1.5 period of the data clock.

The data clock (BCLK) is a square wave signal at twice the data transmission frequency on Bx and Br with a 1 to 1 duty cycle. The frequency can be choosen from 512 to 6176 kHz with 16 kHz modularity. Data transmission rate depends only on the data clock rate.

The Frame Clock FSa is a 8 kHz signal for synchronization of data transmission. The front edge of this signal gives the time reference of the first bit in the first GCI input and output channel, and reset the slot counter at the start of each frame.

When some GCI channels are not selected on devices connected to the same GCI link, these time slots are free for alternative uses.

GCI configuration selection is done by biasing of input pins MW, M0, CONF1, CONF2 according to Table 1.

Table 1: GCI Configuration selection.

Pin Number		Pin name	Configuration				
PLCC44	DIP28		LT/NT12 (1)	NT/TE	NT1-AUTO	LT-RR-AUTO	NT-RR-AUTO
43	28	MW	0	0	0	0	0
42	27	M0	0	1	1	1	1
27	19	S1/CONF1	S1	0	1	1	0
25	17	S2/CONF2	S2	1	1	0	0
10	7	S0/FSb/TEST2	S0	FSb	TEST2	TEST2	TEST2
26	18	IO1/ES1 (2)	IO1	IO1	ES1	PLDD	ES1
24	16	IO2/ES2 (2)	IO2	IO2	ES2	EC	ES2
23	15	IO3/EC (2)	IO3	IO3	EC	LFS	LFS
22	14	IO4/TEST1 (2)	IO4	IO4	TEST1	TEST1	TEST1
35	22	SFSx/RFS (2)	SFSx	SFSx	SFSx	RFS	RFS

(1) Differentation between LT and NT configuration done by bit NTS in CR2 register; GCI in slave mode.

When NT1-AUTO or NT-RR-AUTO configuration is selected, BCLK bit clock frequency of 512 kHz is automatically selected

When NT configuration is selected, BCLK bit clock frequency of 1536 kHz is automatically selected.

(2) Connected to V_{CC} through internal pull-up resistors.

Monitor channel

The Monitor channel is used to write and read all STLC5412 internal registers. Protocol on the Monitor channel allows a bidirectional transfer of bytes between UID and a control unit with acknowledgement at each received byte. Bytes are transmitted on the Br output and received on the Bx input in the Monitor channel time slot.
A write or read cycle is always constituted of two bytes.(see fig. 5). It is possible to operate several write or read cycles within a single monitor message.

Note: Special format is used for EOC channel.

Write cycle

The format to write a message into the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Address
A0: Write/Read back Indicator
D7-D0: Register Content

After the first byte is shifted in, Register address is decoded. A0 set low indicates a write cycle: the content of the following received byte has to be loaded into the addressed register.

A0 set high indicates a read-back cycle request. The second byte content is not significative. STLC5412 will respond to the request by sending back a message with the register content associated with its own address. It is then possible for the microprocessor to receive the required register content after several other pending messages. To avoid any loss of data, it is recommended to operate only one read-back request at a time.

Note: Special format is used for EOC channel.

Read cycle

When UID has a register content to send to the controller, it send it on the monitor channel directly. Note that the data to send can be the content of a Register previously requested by the controller by means of a read-back request.

The format of the message sent by the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Address
A0: forced to 0 if spontaneous interrupt, forced to 1 if read-back
D7-D0: Register Content

Exchange Protocol

STLC5412 validates a received byte if it is detected two consecutive times identical. (see fig. 5)

The exchange protocol is identical for both directions. The sender uses the E bit to indicate that it is sending a Monitor byte while the receiver uses A bit to acknowledge the received byte.When no message is transferred, E bit and A bit are forced to inactive state.

A transmission is started by the sender (Transmit section of the Monitor channel protocol handler) by putting the E bit from inactive to active state and by sending the first byte on Monitor channel in the same frame. Transmission of a message is allowed only if A bit sent from the receiver has been set inactive for at least two consecutive frames. When the receiver is ready, it validates the incoming byte when received identical in two consecutive frames. Then, the receiver set A bit from the inactive to the active state (preacknowledgement) and maintain active at least in the following frame (acknowledgement).

If validation is not possible (two last bytes received are not identical) the receiver aborts the message by setting the A bit active for only a single frame.The second byte can be transmitted by the sender putting the E bit from the active to the inactive state and sending the second byte on the Monitor channel in the same frame . The E bit is set inactive for only one frame. If it remains inactive more than one frame, it is an end of message. The second byte may be transmitted only after receiving of the pre-acknowledgement of the previous byte . Each byte has to be transmitted at least in two consecutive frames.

The receiver validates the current received byte as for the first one and then set the A bit in the next two frames first from the active state to the inactive state (pre-acknowledgement) and back to the active (acknowledgement). If the receiver cannot validates the received current byte (two bytes received not identical)it pre-acknowledges normally but let the A bit in the inactive state in the next frame which indicates an abort request . If a message sent by the UID is aborted, the UID will send again the complete message until receiving of an acknowledgement . A message received by the UID can be acknowledged or aborted with flow Control.

The most significant bit (MSB) of Monitor byte is sent first on the Monitor channel. E & A bits are active low and inactive state on Br is 5 V. When no byte is transmitted, Monitor channel time slot

on Br is in the high impedance state.

A 24 ms timer is implemented in the UID. This timer (when enabled) starts each time the sender starts a byte sending and waits for a pre acknowledgement.

C/I channel

The C/I channel is used for TXACT and RXACT registers write and read operation. However, it is possible to access to ACT registers by monitor channel: this access is controled by the CID bit in CR2 register.

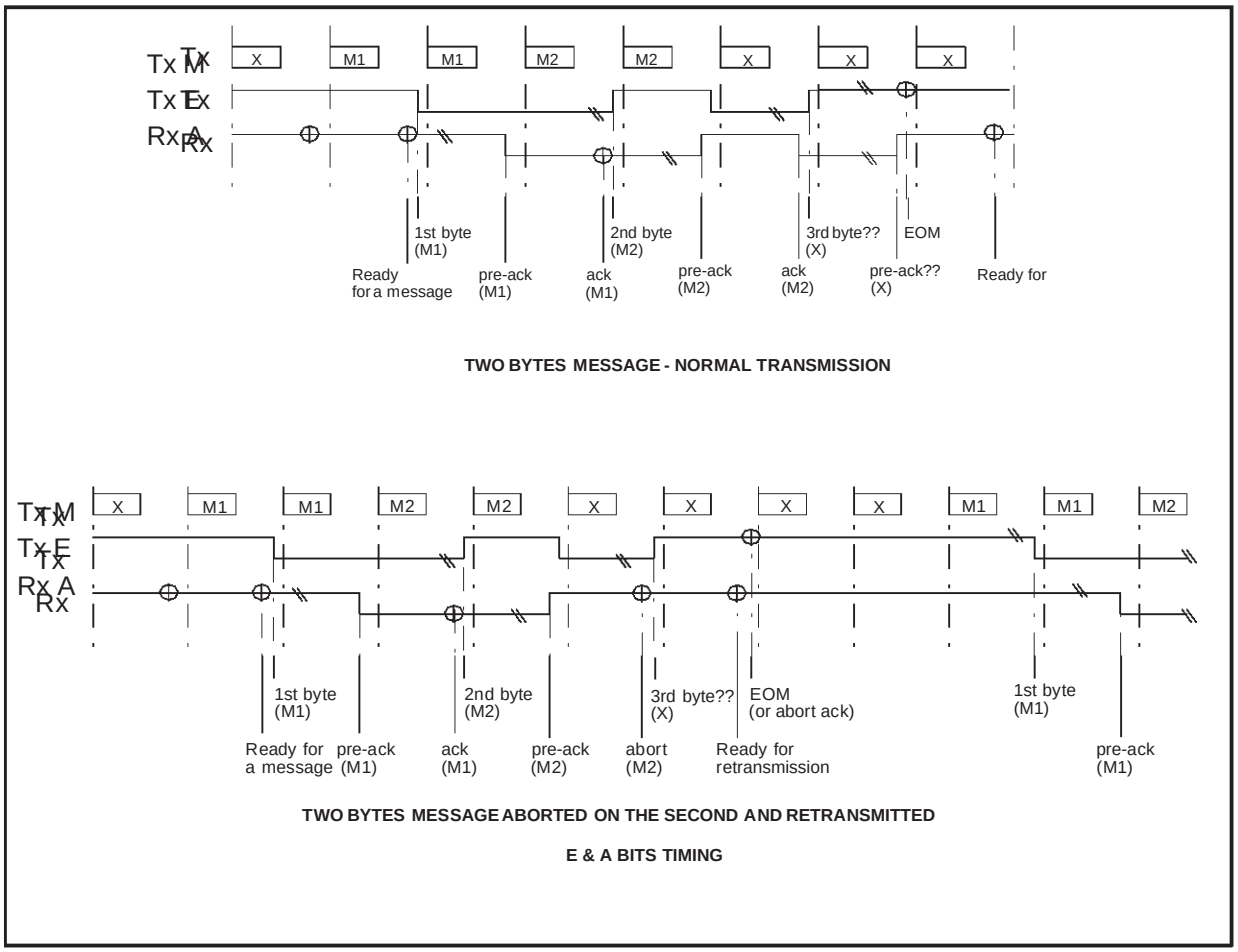
The four bits code (C1,C2,C3,C4) of TXACT register can be loaded in the UID by writing permanently this code in the C/I channel time-slot on Bx input every GCI frames. The UID takes into account the received code when it has been received two consecutive times identical. When a status change occurs in the RXACT register, the new (C1,C2,C3,C4) code is sent in the C/I channel time-slot on Br output every GCI frames. This code is sent permanently by the UID until a new status change occurs in RXACT register.
C1 bit is sent first to the line.

LINE CODING AND FRAME FORMAT

2B1Q coding rule requires that binary data bits are grouped in pairs so called quats (see Tab.2). Each quat is transmitted as a symbol, the magnitude of which may be 1 out 4 equally spaced voltage levels (see Fig. 6). +3 quat refers to the nominal pulse waveform specified in the ANSI standard. Other quats are deduced directly with respect of the ratio and keeping of the waveform.

The frame format used in UID follows ANSI specification (see Tab. 3 and 4). Each complete frame consists of 120 quats, with a line baud rate of 80 kbaud, giving a frame duration of 1.5ms. A nine quats lenght sync-word defines the framing boundary. Furthermore, a Multiframe consisting of 8 frames is defined in order to provide sub-channels within the spare bits M1 to M6. Inversion of the syncword defines the multiframe boundary. In LT, the transmit multiframe starting time may be synchronized by means of a 12 ms period of time pulse on the SFSx pin selected as an input (bit SFS in CR2); If SFSx is selected as an output, SFSx provides a square wave signal with the rising edge indicating the multiframe starting time.
In NT, the transmit multiframe starting time is pro-

Figure 5: GCI Monitor channel messaging examples.



vided on SFSx output by the rising edge of a 12 ms period square wave signal. LT or NT, when pin 25 is selected as SFSr by mean of bit ESFr in CR4, SFSr is a square wave open drain output indicating the received superframe on the line. (see figure 7). Prior to transmisssion, all data, with the exception of the sync-word,is scrambled using a self-synchronizing scrambler to perform the specified 23rd-order polynomial. Descrambling is included in the receiver. Polynomial is different depending on the direction LT to NT or vice versa.

TRANSMIT SECTION

Data transmitted to the line consists of the 2B+D channel data received from the Digital Interface through an elastic data buffer allowing any phase deviation with the line, the activation/deactivation bits (M4) from the on-chip activation sequencer, the CRC code plus maintenance data (eoc channels) and other spare bits in the overhead channels (M4, M5, M6). Data is multiplexed and scrambled prior to addition of the sync-word, which is generated within the device. A pulse waveform synthesizer then drives the transmit filter, which in turn passes the line signal to the line driver. The differential line-driver outputs, LO+, LO- are designed to drive a transformer through an external termination circuit. A 1:1.5 transformer designed as shown in the STLC5412 user guide, results in a signal amplitude of 2.5V pk nominal on the line for single quats of the +3 level. (see output pulse template fig.8). Short-circuit protection is included in the output stage; over-voltage protection must be provided externally.

In LT applications, the Network reference clock given by the FSa 8kHz clock input synchronizes the transmitted data to the line. The Digital Interface normally accepts BCLK and FSa signals from the network, requiring the selection of Slave Mode in CR1. A Digital Phase-Locked Loop (DPLL 1) on the UID allows the SCLK frequency to be plesiochronous with respect to the network reference clock (8 kHz FSa input). With a tolerance on the XTAL1 oscillator of 15.36 MHz +/- 100 ppm, the lock-in range of DPLL1 allows the network clock frequency to deviate up to +/- 50ppm from nominal.

In LT, if DSI is selected in Master mode, (Microwire only, bit CMS = 1 in CR1), BCLK and FSa signals are outputs frequency synchronized to XTAL1 input, DPLL 1 is disabled.

In NT applications, data is transmitted to the line with a phase deviation of half a frame relative to the received data as specified in the ANSI standard.

RECEIVE SECTION

The receive input signal should be derived from the transformer by a coupling circuit as shown in the user guide. At the front end of the receive section is a continuous filter which limits the noise bandwidth to approximately 100kHz. Then, an analog pre-canceller provides a degree of echo cancellation in order to limit the dynamic range of the composite signal which noise bandwidth limited by a 4th order Butterworth switched capacitor low pass filter. After an automatic gain control, a 13bits A/D converter then samples the composite received signal before the echo cancellation from local transmitter by means of an adaptive digital transversal filter. The attenuation and distortion of the received signal from the far-end, caused by the line, is equalized by a second adaptive digital filter configured as a Decision Feedback Equalizer (DFE), that restores a flat channel response with maximum received eye opening over a wide spread of cable attenuation characteristics.

A timing recovery circuit based on a DPLL (Digital Phase-Locked Loop) recovers a very low-jitter clock for optimum sampling of the received symbols. The 15.36MHz crystal oscillator (or the logic level clock input) provides the reference clock for the DPLL. In NT configuration, SCLK output provides a very low jitter 15.36MHz clock synchronized from the line.

Received data is then detected and flywheel synchronization circuit searches for and locks onto the frame and superframe syncwords. STLC5412 is frame-synchronized when two consecutive synchwords have been consecutively detected. Frame lock will be maintained until six consecutive errored sync-words are detected, which will cause the flywheel to attempt to re-synchronize. If a loss of frame sync condition persists for 480ms the device will cease searching, cease transmitting and go automatically into the RESET state, ready for a further cold start. When UID is frame-synchronized, it is superframe-locked upon the first superframe sync-word detection. No loss of superframe sync-word is provided.

While the receiver is synchronized, data is descrambled using the specified polynomial, and individual channels demultiplexed and passed to their respective processing circuits: user's 2B+D channel data is transmitted to the Digital Interface through an elastic data buffer allowing any phase deviation with the line; the activation/deactivation bits (M4) are transmitted to the on-chip activation sequencer; CRC is transmitted to CRC checking section while maintenance data (eoc) and other spare bits in the overhead channels (M4, M5, M6) are stored in their respective Rx registers.

In NT applications, if the Digital Interface is selected in master mode (see CR1) BCLK and FSa clock outputs are phase-locked to the recovered clock. If it is selected in Slave mode ie for NT1-2 application, the on-chip elastic buffers allow BCLK and FSa to be input from an external source, which must be frequency locked to the received line signal ie using the SCLK output but

with arbitrary phase.

ELASTIC BUFFERS

The UID buffers the 2B+D data in elastic fifos which are 3 line-frames deep in each direction. When the Digital Interface is a timing slave, these FIFOs compensate for relative jitter and wander between the Digital Interface and the line. Each buffer can absorb wander up to 18µs at 80 KHz max without "slip". This is particulary convenient for NT1-2 or PABX application in case the local reference clock is jitterized and wandered relative to the incoming signal from the line.

DECT SYNCHRONIZATION

In a DECT system the U interface is used for digital transmission between the base station controller (LT) and the base station (NT). The U interface allows the transmission of 4 DECT channels through B1, B2 using ADPCM compression. Beside the D channel allows the exchange of signalling information between the base station controller (BSC) and the base station (BS).

Seamless handover (for switching the radio-communication from one base station to another) requires additional features in U interface circuit for base stations synchronisation.

DECT Oriented Features In U Interface

- Possibility to measure the round-trip delay between BSC and BS.
  The different delay of each BSC-BS connection can be compensated in each BS with a preset counter that is loaded with the delay value provided by the STLC5412 in the BSC and sent to the BS via the D channel.
  Round trip delay (RTD) measurement allows to estimate the link delay (SFSrNT-SFSxLT = RTD/2+Konst) with a total accuracy of +/- 200 nsec when STLC5412 is used both in BSC and BS. The total accuracy is the sum of two contributions. The process spread on internal propagation delays (±166.5ns) and jitter on recovered clock in LT (±32.5ns).
- DECT frames synchronisation.
  The BSC must synchronise all the BSs connected to itself. A synchronisation pulse DECSYNC is provided by the network to all the STLC5412 devices in the BSC (LT). The STLC5412 devices synchronise the 2B1Q frames on the U link with DECSYNC and send an EOC message to the corresponding BS (NT). The STLC5412 in the BS (NT) on reception of the EOC message provides a pulse to preset the counter for DECT frame generation. The jitter related to this pulse is the jitter of the recovered clock in NT. Maximum jitter guaranteed on all ETSI loops is ±130ns.
  These two features allow the BSC to generate synchronous DECT frames (160ms) and multiframes with maximum phase difference of ±330ns.

LT DECT MODE

In LT DECT mode the STLC5412 provides round trip delay estimation with a resolution of +/- 33 nsec. and automatic EOC DECT message transfer for base stations synchronisation.
The DECSYNC pulse is applied to pin SFSx (CR2.7=0). The DECSYNC period must be multiple of 12ms and in phase with FSa. The SFSx input pulse resets the line frame counter when the device is in power-up. After power-up, before activation, it is suggested to wait for the first available DECSYNC pulse. If not, the DECSYNC pulse will generate a jump in the line synchronisation, that can cause a line deactivation.

- Round trip delay estimation procedure
  The round trip delay is the delay between Transmit sync word (ISW) and receive Sync word on the line. It can be estimated from three parameters that can be read in internal registers:
  tdd: total digital delay
  delay between SFSx and SFSr in steps of 12.5 µsec. It is available in register DBAUD0-4
  edd: elastic digital delay
  value to add to tdd that takes into account the internal elastic memory state. It is available in register DBAUD5-7
  ced: clock elastic delay
  It provides the phase difference between transmit and receive clocks in steps of 65.1 nsec. It is available in register DTXRX. See Application Note for use.
- DECT EOC message transfer
  If CR7.0 = 1 (DECT mode) a synchronisation pulse on pin SFSx triggers the DECT EOC message transfer. The message stored in DECTEOC register is transmitted 3 times in the EOC channel starting from the 1st available superframe following the DECSYNC pulse on the SFSx pin. See Application Note for use.

NT DECT MODE

In NT DECT mode the STLC5412 after recognition of DECT EOC message stored in DECT EOC register, generates a pulse on pin SFSx, synchronous with next SFSr edge. In this way the STLC5412 provides on pin SFSx a pulse used to resynchronise the DECT frame counter in the base station.

The LOCK bit in CR7 register can be used to enable the locking of FSa with SFSr after line is activated.

In particular the FSa rising edge will occur 62.5us after the SFSr rising edge.

If not programmed this bit is inactive. The relock will take place only after completion of present monitor transfer. (EOM received). This locking will cause a phase jump of FSa and BCLK signals. To avoid problems on the GCI bus that is synchronized by FSa, a number of 5 GCI frames after the phase jump will be ignored by the STLC5412.

For proper system operation before writing the LOCK bit in CR7 register, the MOB bit (Mask Overhead Bits) in CR4 register should be set to 1 to avoid spontaneous monitor message generation from STLC5412. Following the relocking the MOB bit should be set back to desired value after a minimum time to be defined (ex. 1msec).

The suggested procedure is to program the LOCK bit in CR7 register after the AI indication from STLC5412. In this case the system controller knows when the phase jump takes place and can reset the transmission/reception of the GCI controller.

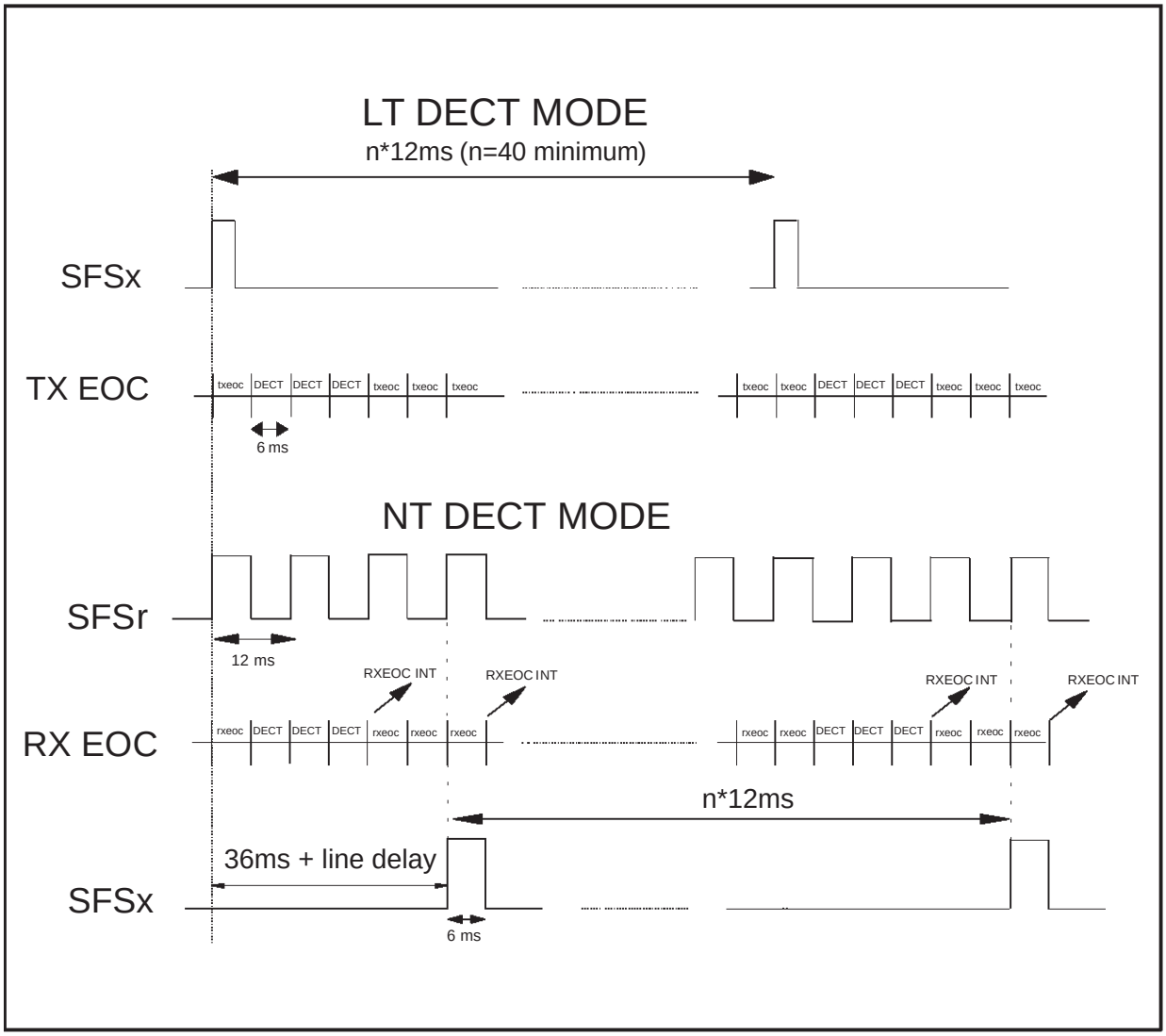
Notes:
The DECT EOC message reception generates an interrupt as a normal EOC message according to the rules stored in OPR register. The DECT sync message must be checked 3 times (reset value of OPR register). If it is not detected 3 times identical no pulse is generated. The DECT pulse width on output pin SFSx is 6msec.

MAINTENANCE FUNCTIONS

M channel

In each frame there are 6 "overhead" bits assigned to various control and maintenance functions. Some programmable processing of these bits is provided on chip while interaction with an external controller provides the flexibility to take full advantage of the maintenance channels. See OPR, TXM4, TXM56, TXEOC, RXM4, RXM56, RXEOC

TIMING DIAGRAMS FOR DECT



registers description for details. New data written to any of the overhead bit Transmit Registers is resynchronized internally to the next available complete superframe or half superframe, as appropriate.

Embedded Operation Channel (EOC)
The eoc channel consists of two complete 12 bits messages per superframe, distributed through the M1, M2 and M3 bits of each frame. Each message is composed of 3 fields; a 3 bit address identifying the message destination/origin, a 1 bit indicator for the data mode i.e. encoded message or raw data, and an 8 bits information field. The Control Interface (Microwire or Monitor channel in GCI) provides access to the complete 12 bits of every message in TX and RX EOC registers.

When non-auto mode is selected, UID does not interpret the received eoc messages e.g. "send corrupted CRC"; therefore the appropriate command instruction must be written to the device e.g. "set to one bit CTC in register CR4". It is possible to select a transparent transmission mode in which the eoc channel can be considered as a transparent 2 kbit/s channel. See OPR register description for details.

When auto-mode is selected in GCI configuration, UID performs automatic recognition / acknowledgement of the eoc messages sent by the network according to processing defined in ANSI standard and illustrated in figure 9. When UID recognizes a message with the appropriate address and a known command, it performs automatically the relevant action inside the device and send a message at the digital interface as appropriate. Table 5 gives the list of recognized eoc messages and associated actions.

When NT-RR-AUTO configuration is selected, eoc addressing is processed according to appendix E of T1E1.601 standard:

– If address of the eoc message received from LT is in the range of 2 to 6, UID decrements address and pass the message onto GCI.
– If address of the eoc message received from GCI is in the range of 1 to 5, UID increments address and pass the message onto the line toward LT.
– If data/msg indicator is set to 0, UID pass data on transparently with eoc address as described above.

M4 channel
M4 bit positions of every frame is a channel in which are transmitted data bits loaded from the TXM4 transmit register and from the on-chip activation sequencer each superframe. On the receive side, M4 bits from one complete superframe are first validated and then stored in the RXM4 Receive Register or transmitted to on-chip activation sequencer. See OPR, TXM4 and RXM4 registers description for details.

When NT1-AUTO or NT-RR-AUTO mode is selected, bits ps1 and ps2 in M4 channel are controlled directly by biasing input pins ES1 and ES2 respectively. e.g. ps1 is sent continuously to the line equal 0 when ES1 input is forced at 0 Volt.

Spare M5 and M6 bits
The spare bit positions in the M5 and M6 field form a channel in which are transmitted data bits loaded from the TXM56 transmit register. On the receive side, the spare bits in the M5 and M6 field are first validated and then stored in the RXM56 receive register. See OPR, TXM56 and RXM56 registers description for details.

CRC calculation/checking
In transmit direction, an on-chip CRC calculation circuit automatically generates a checksum of the 2B+D+M4 bits using the specified 12th order polynomial. Once per superframe, the CRC is transmitted in the M5 and M6 bit positions. In receive direction, a checksum is again calculated on the same bits as they are received and, at the end of the superframe compared with the received CRC. The result of this comparison generates a "Far End Block Error" bit (febe) which is transmitted back towards the other end of the Line in the next but one superframe and an indication of Near End Block Error is sent to the system by means of Register RXM56. If there is no error in superframe, febe is set = 1, and if there is one or more errors, febe is set = 0.

UID also includes two 8 bits Block Error Counters associated with the febe bits transmitted and received. It is then possible to select one Error Counter per direction or to select only one counter for both by means of bit C2E in OPR register. Block error counting is always enabled but it is possible to disabled the threshold interrupt and/or to enable/disable the interrupt issued at each received or transmitted block error detection. See OPR register for details.

Loopbacks
Six transparent or non transparent channel loopbacks are provided by UID. It is therefore possible to operate any loopback on B1, B2 and D channels line to line or DSI/GCI to DSI/GCI. Command are grouped in CR3 register.

In addition to the channel loopbacks in LT modes, a complete transparent loopback operated at the transmission side of UID allows the device to activate through an appropriate sequence with the complete data stream looped-back to the receiver. Therefore, most of analog/digital clock and data recovery circuits are tested. After activation completed, an AI status indication is reported. Complete loopback is enabled with ARL command in TXACT register.

Table 2: 2B1Q Encoding of 2B+ D Fields.

Data	Time →								
	B_l				B_g				D
Bit Pair	$b_{11}b_{12}$	$b_{13}b_{14}$	$b_{15}b_{16}$	$b_{17}b_{18}$	$b_{21}b_{22}$	$b_{23}b_{24}$	$b_{25}b_{26}$	$b_{27}b_{28}$	d_1d_2
Quat # (relative)	q_1	q_2	q_3	q_4	q5	q_6	q_7	q_8	q_9
# Bits	8				8				2
# Quats	4				4				1

Where:
b_{11} = first bit of B_1 octet as received at the S/T interface

b_{18} = last bit of B_l octet as received at the S/T interface

b_{21} = first bit of B_2 octet as received at the S/T interface

b_{28} = last bit of B_2 octet as received at the S/T interface

d_1 d_2 = consecutive D-channel bits (d_1 is first bit of pair as received at the S/T interface)

q_i = ith quat relative to start of given 18-bit 2B+D data field.

NOTE: There are 12 2B+D 18-bit fields per 1.5 msec basic frame.

Table 3: Network-to-NT 2B1Q Superframe Technique and Overhead Bit Assignments.

		FRAMING	2B+D	Overhead Bits (M_1-M_6)					
	Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit Positions	1-18	19-234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B+D	M_1	M_2	M_3	M_4	M_5	M_6
A	1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	dea	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	1	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	1	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	uoa	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	aib	crc_{11}	crc_{12}
B,C,...									

NT-to-Network superframe delay offset from Network-to-NT superframe by 60 ± 2 quats (about 0.75 ms). All bits than the Sync Word are scrambled.

Symbols & Abbreviations:

”1”	reserve = reserved bit for future standard; set = 1	act	activation bit
eoc	embedded operations channel a = address bit dm = data/message indicator i = information (data/message)	crc	cyclic redundancy check: covers 2B+D & M4 1 = most significant bit 2 = next most significant bit etc
SW	synchronization word	febe	far end block error bit (set = 0 for errored superframe)
ISW	inverted synchronization word	dea	deactivation bit (set = 0 to announce deactivation)
s	sign bit (first) in quat	uoa	u only activation bit (set = 1 to activate S/T)
m	magnitude bit (second) in quat	aib	alarm indication bit (set = 0 to indicate interruption)

Table 4: NT-to-Network 2B1Q Superframe Technique and Overhead Bit Assignments.

		FRAMING	2B+D	Overhead Bits (M_1-M_6)					
	Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit Positions	1-18	19-234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B+D	M_1	M_2	M_3	M_4	M_5	M_6
1	1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	ps_1	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	ps_2	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	ntm	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	cso	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	sai	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_{11}	crc_{12}
2,3,...									

NT-to-Network superframe delay offset from Network-to-NT superframe by 60 ± 2 quats (about 0.75 ms). All bits than the Sync Word are scrambled.

Symbols & Abbreviations:

"1"	reserve = reserved bit for future standard; set = 1	ps_1, ps_2	power status bits (set = 0 to indicate power problems)
eoc	embedded operations channel a = address bit dm = data/message indicator i = information (data/message)	ntm	NT in Test Mode bit (set = 0 to indicate test mode
SW	synchronization word	cso	cold-start-only bit (set = 1 to indicate cold-start-only
ISW	inverted synchronization word	crc	cyclic redundancy check: covers 2B+D & M4 1 = most significant bit 2 = next most significant bit etc
s	sign bit (first) in quat	febe	far end block error bit (set = 0 for errored superframe)
m	magnitude bit (second) in quat	sai	S/T interface activation indication bit.
act	activation bit		

Figure 6: Example of 2B1Q Quaternary Symbols.

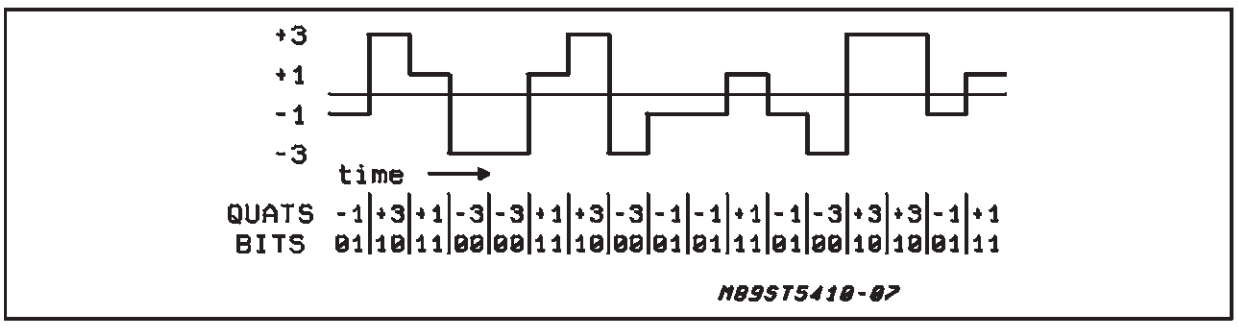


Figure 7: Superframe I/O pin SFS

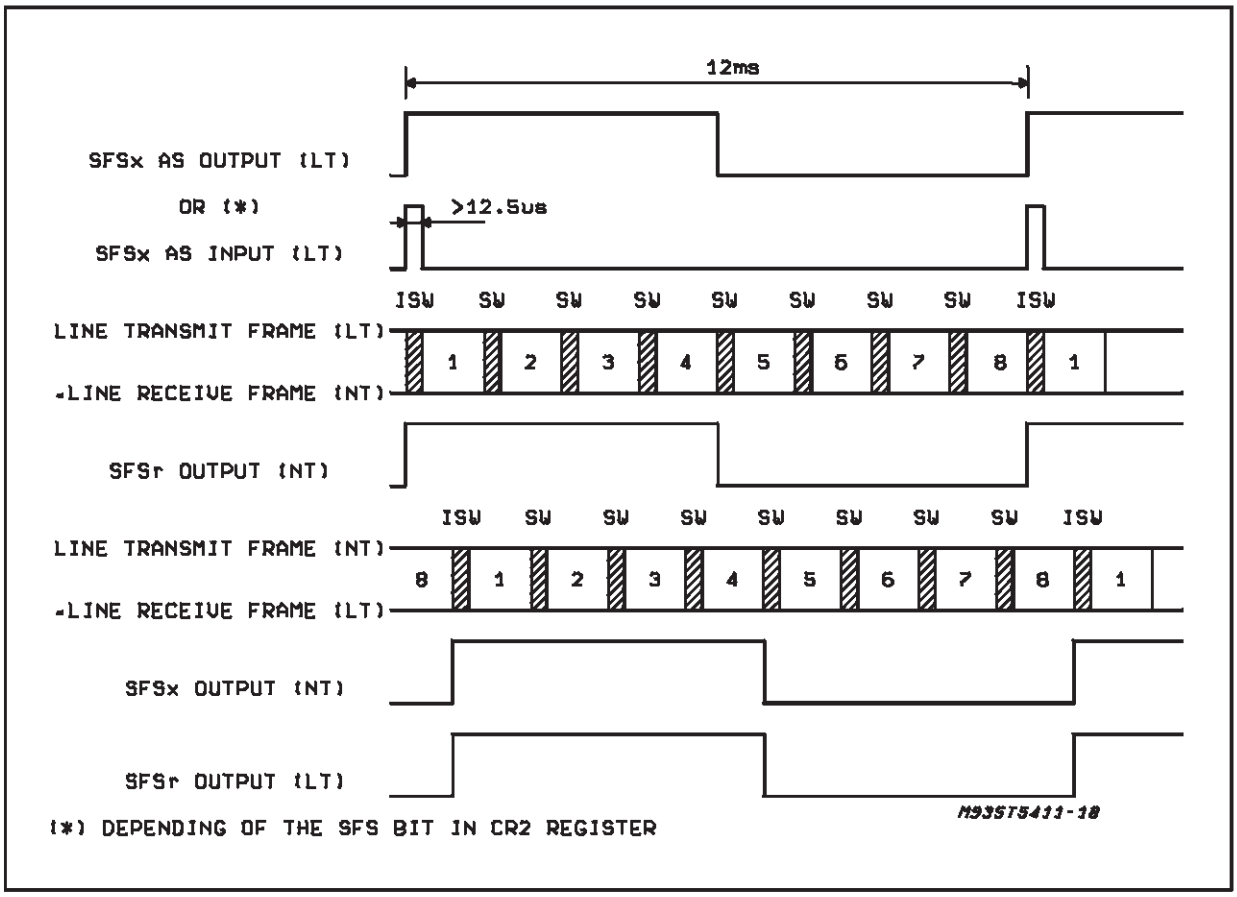
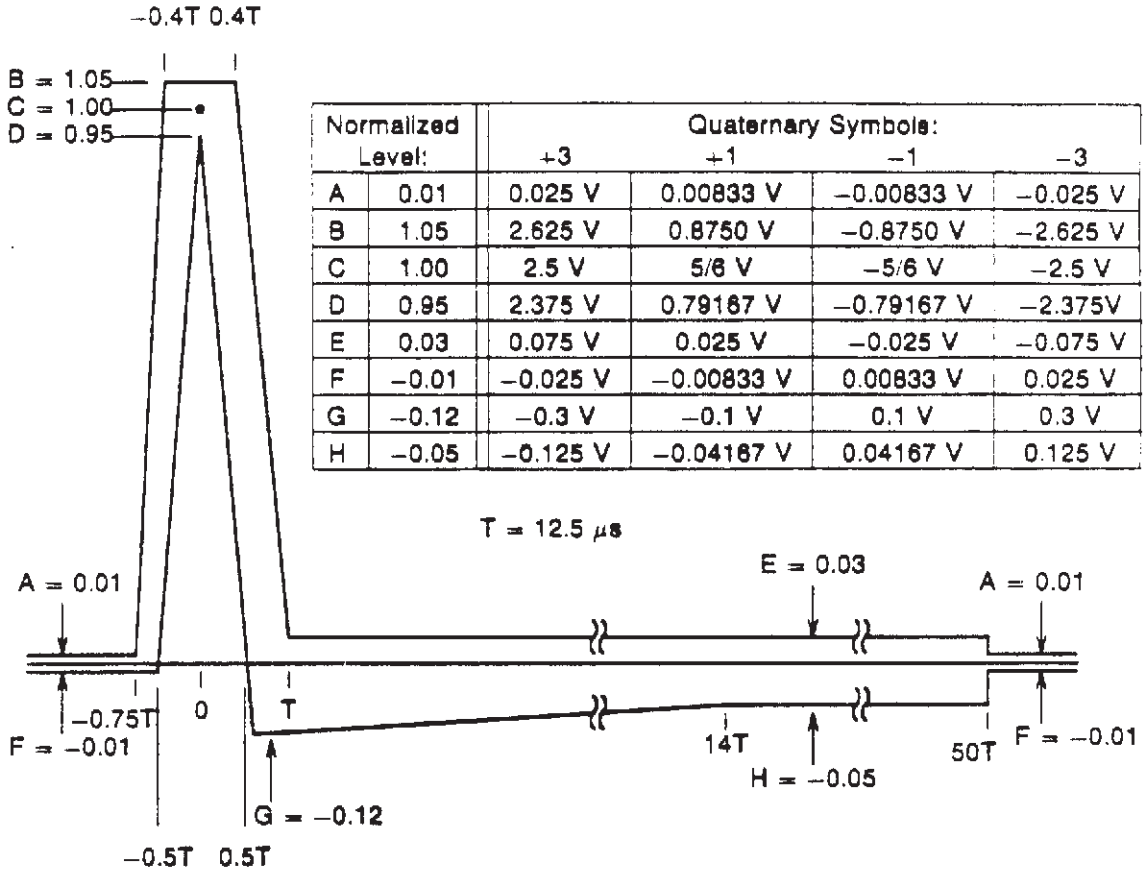


Figure 8: Normalized output pulse form



Normalized Level:		Quaternary Symbols: +3	+1	−1	−3
A	0.01	0.025 V	0.00833 V	−0.00833 V	−0.025 V
B	1.05	2.625 V	0.8750 V	−0.8750 V	−2.625 V
C	1.00	2.5 V	5/6 V	−5/6 V	−2.5 V
D	0.95	2.375 V	0.79167 V	−0.79167 V	−2.375V
E	0.03	0.075 V	0.025 V	−0.025 V	−0.075 V
F	−0.01	−0.025 V	−0.00833 V	0.00833 V	0.025 V
G	−0.12	−0.3 V	−0.1 V	0.1 V	0.3 V
H	−0.05	−0.125 V	−0.04167 V	0.04167 V	0.125 V

Figure 9: EOC message processing mode.

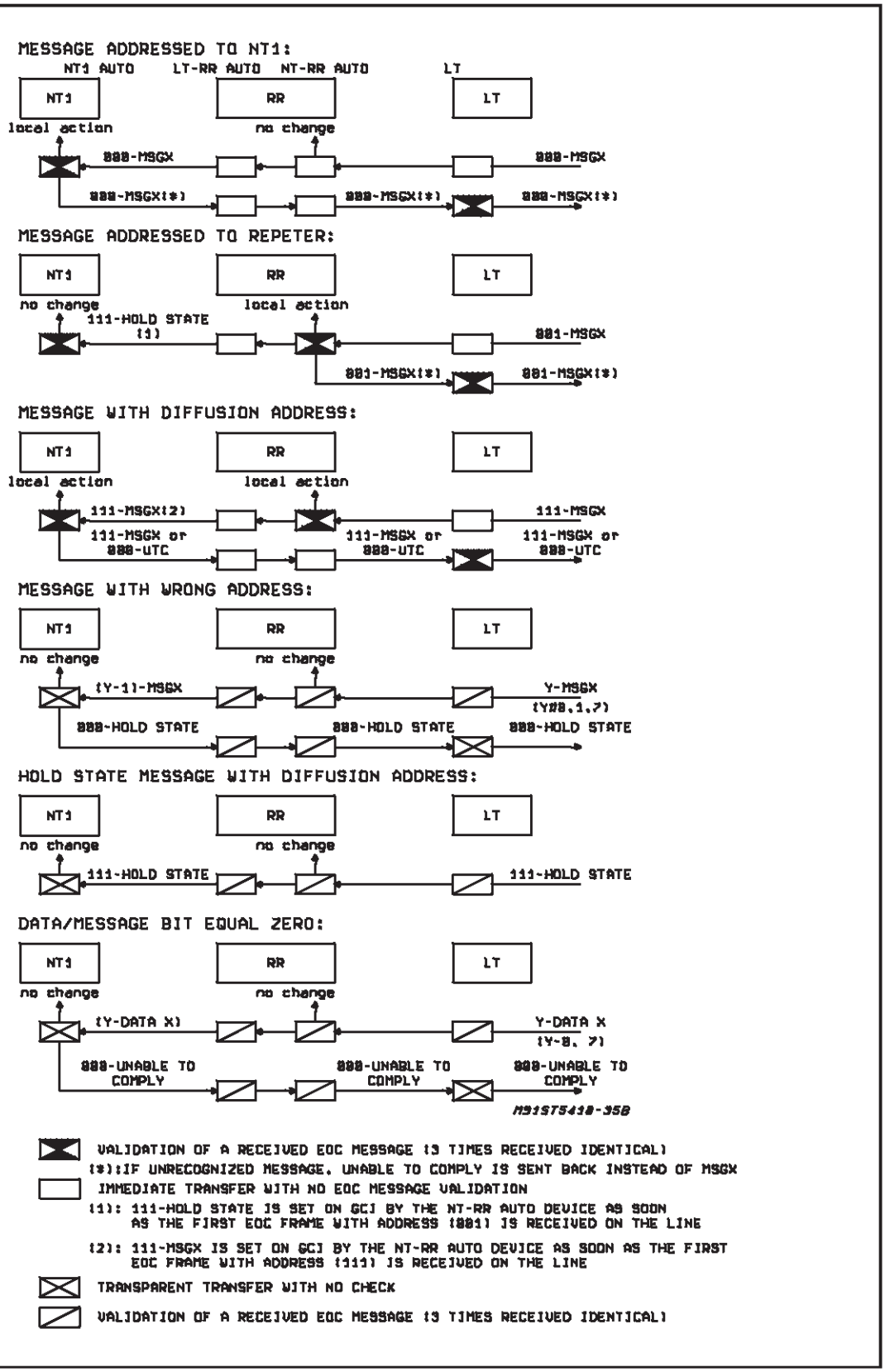


Figure 10: CRC Errors Processing (auto-mode)

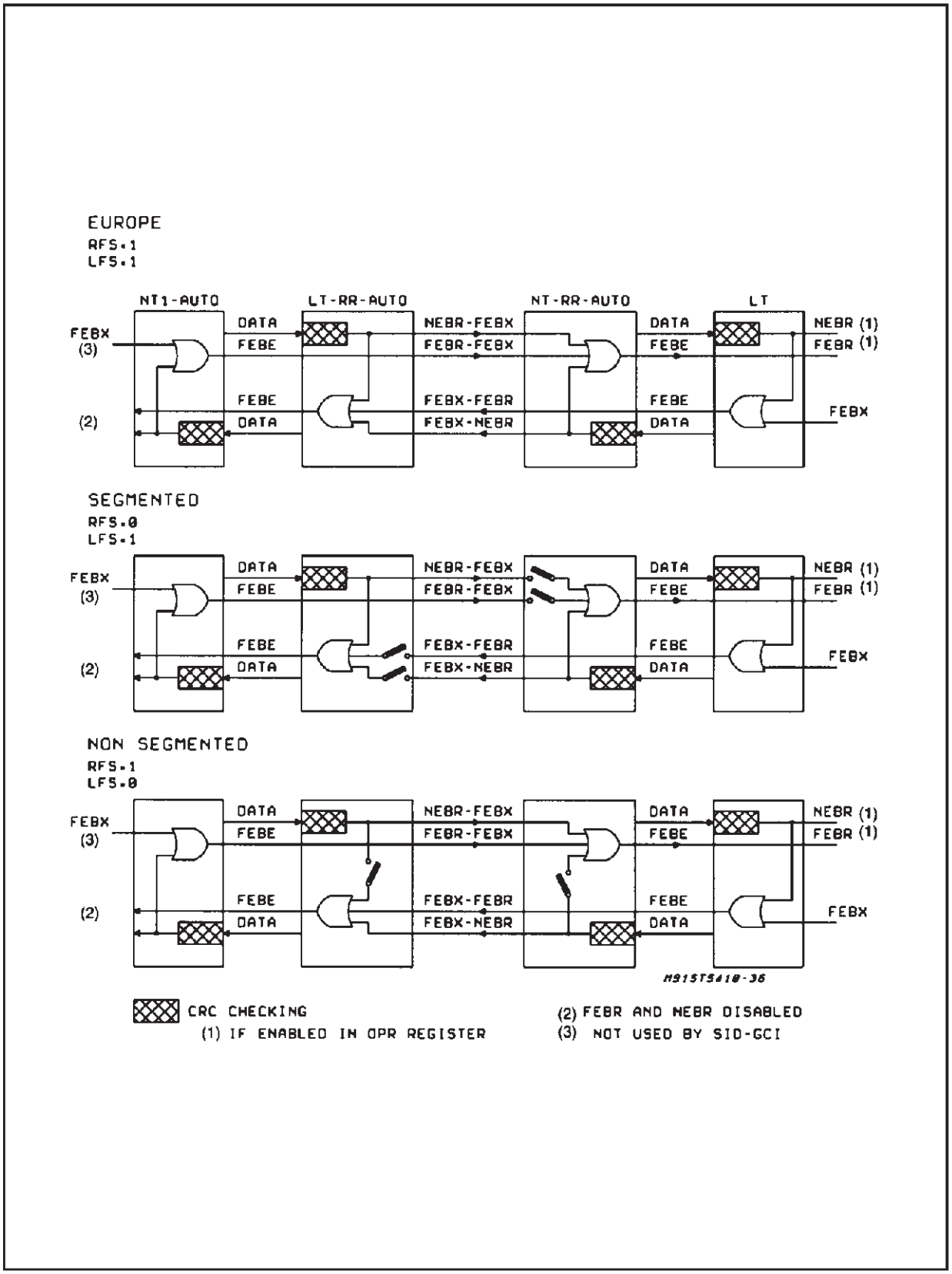


Table 5: EOC message processing: local actions.

NT1-AUTO: (eoc address 000 or 111)

Message	Code	Local action
Operate 2B+D loopback	0101 0000	Send ARL code on C/I channel to operate Loopback 2 in SID-GCI. Forces EC output low
Operate B1channel Loopback	0101 0001	Performs transparent loopback on B1 channel identical to LB1 command in CR3
Operate B2 channel Loopback	0101 0010	Performs transparent loopback on B2 channel identical to LB2 command in CR3
Request Corrupted CRC	0101 0011	Performs corruption of the transmit CRC identical to CTC command in CR4.
Notify of Corrupted CRC	0101 0100	No action taken. Send back to the Network unable to comply message.
Return to Normal	1111 1111	All outstanding EOC operations are reset.
Hold state	0000 0000	All outstanding EOC operations maintained in their present state
Unable to comply	1010 1010	Sent by UID to indicate that the message is not in its menu

NT-RR-AUTO: (eoc address 001 or 111)

Message	Code	Local action
Operate 2B+D loopback	0101 0000	Send ARL code on C/I channel to operate Loopback 1A in UID configured in LT-RR-AUTO. Forces EC output low.
Operate B1channel Loopback	0101 0001	Performs transparent loopback on B1 channel identical to LB1 command in CR3
Operate B2 channel Loopback	0101 0010	Performs transparent loopback on B2 channel identical to LB2 command in CR3
Request Corrupted CRC	0101 0011	Performs corruption of the transmit CRC identical to CTC command in CR4.
Notify of Corrupted CRC	0101 0100	No action taken. Send back to the Network unable to comply message.
Return to Normal	1111 1111	All outstanding EOC operations are reset.
Hold state	0000 0000	All outstanding EOC operations maintained in their present state
Unable to comply	1010 1010	Sent by UID to indicate that the message is not in its menu

IDENTIFICATION CODE (GCI)

The identification register is implemented at the two addresses 80 H and 90 H. All accesses at addresses 8x H will generate a read back interrupt containing the addresses 80 H. Accesses at 9x H performs exactly the same thing that the 8X register except the interrupt will be at address 90 H.

Response will be according to the rule herebelow:

identification request:	1 0 0 Y X X X X	X X X X X X X X
identification response:	1 0 0 Y C C C C	T T D D D D D D

with: - C = circuit revision
- T = device type (U = 00)
- D = device level identifying the manufacturer (001000 for SGS-THOMSON Microelectronics)
- Y = don't care

In particular for 1.0 version the identification response is:

1 0 0 Y 0 0 0 0	0 0 0 0 1 0 0 0

For 1.1 version the identification response is:

1 0 0 Y 0 1 0 1	0 0 0 0 1 0 0 0

GENERAL PURPOSE I/Os (GCI)

When GCI non-auto mode is selected, (NT or LT), four programmable I/Os (IO1, IO2, IO3, IO4) are provided and associated with CR5 register. Each I/O is internally pulled-up with a 250kΩ resistor. Input or output can be selected for each pin independently from the others by means of bits IO1, IO2, IO3, IO4 in CR5. D1, D2, D3, D4 bits give the logical value of the I/O pins respectively. When a status change occurs on one of the input pins, CR5 is sent on the monitor channel of the GCI interface.

When GCI auto-mode is selected, two inputs (ES1, ES2) and one output (EC) are provided in NT1-AUTO and NT-RRAUTO configurations only. ES1 and ES2 inputs drive the logical values of ps1 and ps2 bits in the M4 channel on the line while EC ouput normally high is driven low using the eoc message "operate 2B+D loopback. This intends to provide power supply testing command occuring simultaneously with the loopback command.

TEST FUNCTIONS

Various test functions are provided for transmitted pulse waveform checking, power spectral density measurement and transmitter linearity.

Three commands in TXACT register are provided. The associated test function is enabled as long as the command is not disabled by any other command.

SP1: (0010) Send Single Pulses+1, -1:
+1, -1, pulses are transmitted consecutively onto the line, one pulse per frame.

SP3: (1011) Send Single Pulses+3, -3:
+3, -3, pulses are transmitted consecutively onto the line, one pulse per frame.

RDT: (0011) Random Data Transmitted:

Random data can be transmitted onto the line continuously. B1, B2 and D channel transparency between the digital interface and the line is enabled.

When auto-mode is selected, two test inputs (TEST1, TEST2) are provided allowing the same test functions as described above but without the need of a microcontroller. See Table 6 for Test pins biasing.

Table 6: Test Pins

TEST1	TEST2	FUNCTIONS
1	1	Normal operation
1	0	Send Single Pulse ± 1
0	1	Random Data Transmitted
0	0	Send Single Pulse ± 3

TURNING ON AND OFF THE DEVICE

STLC5412 contains an automatic sequencer for the complete control of the start-up activation sequences. Interactions with an external control unit requires only Activate Request and Deactivate Request commands, with the option of inserting break-points in the sequence for additional external control allowing for instance easy building of a repetor application. Automatic control of act, uoa/sai and dea bits in the M4 bit positions is provided, along with the specified 40 ms, 480 ms and 15 s timers used during the sequencing.

Except the Power up and Power down control that is slightly different, the Activation/Deactivation procedures are identical in GCI and Microwire/DSI modes. Same command codes or indication codes are used. In Microwire and GCI mode, activation control is done by writing in the Activation Control Register TXACT and by reading the Activation Indication Register RXACT. For TXACT and RXACT access, MICROWIRE port is used in MICROWIRE mode and C/I channel (or MONITOR channel depending of CID bit in CR2 register) is used in GCI mode.
In MICROWIRE mode, a primitive indication generates first an interrupt requesting an action from the Microprocessor, in GCI mode the primitive Indication is directly transmitted via C/I (or MONITOR channel).

Power on initialization

Following the initial application of power, STLC5412 enters the power down deactivated state in MICROWIRE mode or in GCI mode depending on the polarization of the MW input.
All the internal circuits including the master oscillator are inactive and in a low power state except for the 10 kHz Tone signal detector. The line outputs LO+/LO- are low impedance and all digital outputs are high impedance. All programmable registers and the activation controller are reset to their default value.

GCI configuration is defined by means of the configuration pins M0, CONF1 and CONF2 when Power supply is turned on.
For LT and NT1-2 equipments, GCI configuration should be completed by means of Control Register Programming. See Table 1 for configuration pins bias.

Line signal detection

When UID is in the power down state and a 10kHz tone TN or TL is detected from the line $\overline{\text{LSD}}$ and $\overline{\text{INT}}$ (MICROWIRE/DSI only) open drain outputs are forced to zero.

In NT configuration , code LSD (0000) is loaded in the activation indication register RXACT.

In LT configuration, code AP (1000) is loaded in the activation indication register RXACT.

In Microwire/DSI these indications are sent onto CO at the following access even if the UID is still in power down mode.

In GCI these indications are sent onto the C/I channel as soon as GCI clocks are available.

$\overline{\text{LSD}}$ open drain output is set back in the high impedance state as soon as the UID is powered up.

$\overline{\text{INT}}$ open drain output is set back in the high impedance state when $\overline{\text{CS}}$ input is detected at zero.

Depending of the ACTAUT and PUPAUT bits in CR6 register, UID can powered up itself, also automatically to start the activation.
For all auto mode configurations, on 10KHz tone reception, power up and activation procedure are full automatic, but in NT1 auto, UID waits the uoa bit from the line before to provide (or not) the cloks and primitives to the S device.

Power up control

Microwire/DSI: control instruction PUP in ACT

register is required to power up the UID.

GCI: when GCI "NT master of the clocks"configuration is selected, UID provides the GCI clocks needed for control channel transfer; PUP control instruction is provided to the UID by pulling low the Bx data input; STLC5412 then reacts sending GCI clocks. It is possible to operate an automatic power up of the UID when a wake up tone is detected from the line by connecting the LSD output directly to the Bx input.

GCI: when NT1-2 or LT configuration is selected (M0 = 0), the UID is powered up after configuration setting by the PUP code (0000) on C/I Channel.

Power down control

A control instruction PDN in ACT register is required to power down the device after a period of activity. PDN forces directly the device to the low power state without sequencing through any of the de-activation states. It should therefore only be used after the UID has been put in the line deactivated state. PDN has no influence on the content of the internal registers, but immediately stops the output clocks when UID is in master mode and in µW/DSI mode.

In GCI mode, UID send first two times code DI(1111) on C/I channel before powering down at the end of the assigned GCI channel.

The DI code purpose is similar to PDN code but power down state is entered only when the line is entirely deactivated (state H1 or J1). The DI command is recommended.

Power up state

Power up transition enables all analog and digital circuitry, starts the crystal oscillator and internal clocks. The LSD output is in the high impedance state even if a tone is detected from the line. As for PDN, PUP has no influence on the content of the internal registers

Power down state

Following a period of activity in the power up state, the power down state may be re-entered as described above. Configuration Registers remain in their current state. PDN and DI have no influence on the content of the internal registers: it is then possible, for instance, after a normal deactivation procedure followed by a power down command, to power up again the device in order to operate directly a Warm Start procedure.

ACTIVATION/DEACTIVATION SEQUENCING

Activation/deactivation signals onto the line are in accordance with the activation/deactivation state matrix given in Appendix A.

CASE OF RESTRICTED ACTIVATION

The standard specifies a mode where the U interface can be turned on without the need to activate the S/T interface provided this function is supported at both ends of the loop. In this condition Maintenance channel is available, typically for setting loop-backs in the NT for error rate testing and other diagnostics.

When this mode is enabled, bit M47 on the line in LT to NT direction becomes the uoa bit. Setting UAR activation command in the LT chip will set uoa bit equal zero on the line. Detection of uoa bit equal zero by the NT will inhibit activation of the S/T interface. This results in SN3 signal in the NT to LT direction, which causes generation of UAI indication by the LT U device when superframe synchronized.

If during restricted activation operation, a TE starts to try activate the S/T interface by sending info 1, the NT can pass this request to the LT via M47 bit, the sai bit. This bit is set equal one by writing AR command to the Activation Control Register. sai bit received equal one causes generation of an AP indication by the LT U device.

RESET OF ACTIVATION/DEACTIVATION STATE MACHINE

When the device is either powered-up or down, a control instruction RES resets the activation controller ready for a cold start. That feature can be used if the far-end equipment fails to warm start, for example if the line card or NT has been replaced or if in a regenerator, the loss of synchronisation of the second section imply the reset of the first section for a further cold start. The configuration registers remain in their selected value.

HARDWARE RESET

When GCI configuration is selected, pin RES acts as a logical hardware Reset. The device is entirely reset including activation/deactivation state machine and configuration registers. Configuration pins bias excluding MW define the eventual new configuration. Pin MW must be maintained at the 0 Volt for GCI configuration setting.

It is possible to operate a similar "complete reset" of UID by setting high bit RST in the RXOH command register. In this last case the Control interface remains enabled. Refer to User guide for Software reset procedure.

QUIET MODE

It is possible to force the device in a quiet mode in which UID does not react to any line wake-up tone and LSD pin remains high. There are two

ways to enter quiet mode: QM bit in CR6 register and QM primitive command to write in TXACT register; in this last case, any further primitive will clear quiet mode.

AUTOMODE

For all auto mode configurations, AIS pin allows a choice of line interface: 27 or 15mH for the transformer and resistors line or device side.

In NT1, the activation/deactivation state machine and the automatic power-up / power-down capabilities of the UID provide for a direct connection through GCI between UID and SID-GCI (ST 5421) without the need of an extra microcontroller (see figure 13b). LSD- pin of SID-GCI must be connected together to the Bx input pin of UID to ensure autonomous power-up/down control. Activation/Deactivation commands and indications are transferred from one device to the other by means of the C/I channel. Maintenance functions are automatically processed in UID. Therefore, there is no transfer of messages on the Monitor channel between UID and SID-GCI. Please note that the 2B+D loop-back request at the S interface is provided using the C/I channel code ARL and that there is not automatic processing of S and Q messages in SID-GCI.

In Repetor, the same advantages are provided by a direct connection through GCI between both UID without the need of an extra microcontroller (see figure 13c). As for NT1, C/I channel transfers activation/deactivation commands and indications. Maintenance functions are automatically processed in UIDs, needing the transfer of eoc messages, overhead bits and CRC fault detections. This is performed autonomously on the Monitor channel by sending when required messages in a regular format as already described. eoc messages are transmitted according to Table 5; overhead bits in the M4 channel excluding act, dea, uoa and sai, are transferred transparently; spare overhead bits in M5 or M6 bit positions are also transferred transparently; febe and nebe bits are transmitted according to Figure10.

COMMAND INDICATION (C/I) CODES

Activation, deactivation and some special test functions can be initiated by the system by writing in TXACT register. Any status change of the on-chip state machine is indicated to the system by the UID by setting a new code in the RXACT register. When GCI is selected, TXACT and RXACT registers are normally associated with the C/I channel (it is possible to associate them with the MONITOR channel thank to the CID bit in CR2 register). All commands and indications are coded on four bits: C1, C2, C3, C4. Codes are listed in Table 7. For each mode, a list of recognized commands and generated indications is given. Hereafter, you have a detailed description of the codes depending on mode selected.

NT mode: Command

0000 (PUP): Power Up
When in the power down state, PUP command powers up the device ready for a cold or a warm start. When GCI is selected with clocks as outputs, PUP command is replaced by pulling low Bx input pin.

0001 (RES): Reset
RES command resets UID ready for a cold start. Configuration registers are not changed. RES can be operated when the device is either powered up or down.

If RES command is applied when the line is not fully deactivated, UID properly ends the activation before to come back in H1 state; In this case DP or EIU indication is returned (Auto mode configuration or not respectively).

0010 (SP1): Send Single Pulse +1 and -1
SP1 test command forces UID to send +1, -1, pulses to the line, one pulse per frame.

0011 (RDT): Random Data Transmitted
RDT test command forces UID to send data with random equiprobable levels at 80 kbaud.

0100 (EIS): Error Indicate S Interface
EIS command reports on the U line, a default on the S interface.

0101 (PDN): Power Down
PDN command forces UID to power down state. It should normally be used after UID has been set in a known deactivated state, e.g. in an NT after a DI status indication has been reported. In GCI, C/I indication (DI) is sent twice on Br output before UID powers down.

0110 (UAI): U interface Activation Indicate
UAI command is significant only when RR bit is set equal one in CR2 register or if NT-RR-AUTO auto-mode is selected. After the receiver has been super-frame synchronized, UAI command allows UID to send SN3 signal to the line.

0111 (QM): Quiet Mode
In this mode, UID does not react to any line status change. UID can be powered up or down and ready for a cold start or a warm start. All configuration registers and coefficients remain unchanged. Quiet Mode is disabled by any other command.
Note: Inside UID, an logical or is implemented with this QM primitive and the QM bit in CR6 register.

1000 (AR): Activation Request
Beeing in the Power Up and deactivated state

Table 7a: RXACT (indication) and TXACT (command) codes

	CODES				NT (GCI or MW, NON AUTO-MODE)		LT (GCI or MW, NON AUTO-MODE)	
	C4	C3	C2	C1	RXACT (indications)	TXACT (commands)	RXACT (indications)	TXACT (commands)
0	0	0	0	0	DP/LSD	PUP (1)	–	PUP/DR
1	0	0	0	1	EIU	RES	EIU	RES
2	0	0	1	0	–	SP1	–	SP1
3	0	0	1	1	–	RDT	–	RDT
4	0	1	0	0	EI	EI	EI	FA0
5	0	1	0	1	–	PDN	–	PDN
6	0	1	1	0	–	–	UAI	UAR
7	0	1	1	1	–	QM	–	QM
8	1	0	0	0	AP	AR	AP	AR
9	1	0	0	1	–	–	–	–
A	1	0	1	0	–	–	–	ARL
B	1	0	1	1	–	SP3	–	SP3
C	1	1	0	0	AI	AI	AI	AI
D	1	1	0	1	–	–	–	–
E	1	1	1	0	–	AIL	–	–
F	1	1	1	1	DI	DI	DI	DI

Note:
(1) ONLY IN SLAVE MODE. IN GCI MASTER MODE, SET BX PIN TO "0" TO DO A PUP..

	CODES				NTRR (GCI or MW, NON AUTO-MODE)		LTRR (GCI or MW, NON AUTO-MODE)	
	C4	C3	C2	C1	RXACT (indications)	TXACT (commands)	RXACT (indications)	TXACT (commands)
0	0	0	0	0	DP/LSD	PUP (1)	–	PUP/DR
1	0	0	0	1	EIU	RES	EIU	RES
2	0	0	1	0	–	SP1	–	SP1
3	0	0	1	1	–	RDT	–	RDT
4	0	1	0	0	EI	EI	EI	FA0
5	0	1	0	1	–	PDN	–	PDN
6	0	1	1	0	UAP	UAI	UAI	UAR
7	0	1	1	1	–	QM	–	QM
8	1	0	0	0	AP	AR	AP	AR
9	1	0	0	1	–	–	–	–
A	1	0	1	0	–	–	–	ARL
B	1	0	1	1	–	SP3	–	SP3
C	1	1	0	0	AI	AI	AI	AI
D	1	1	0	1	–	–	–	–
E	1	1	1	0	–	–	–	–
F	1	1	1	1	DI	DI	DI	DI

(1) ONLY IN SLAVE MODE.

Table 7b: RXACT (indication) and TXACT (command) codes.

	CODES	NT1 (GCI ONLY, AUTO-MODE)	
	C4 C3 C2 C1	**RXACT** (indications)	**TXACT** (commands)
0	0 0 0 0	DP/LSD	(1)
1	0 0 0 1	–	RES
2	0 0 1 0	–	SP1
3	0 0 1 1	–	RDT
4	0 1 0 0	EI	EI
5	0 1 0 1	–	PDN
6	0 1 1 0	–	–
7	0 1 1 1	–	QM
8	1 0 0 0	AP	AR
9	1 0 0 1	–	–
A	1 0 1 0	ARL	–
B	1 0 1 1	–	SP3
C	1 1 0 0	AI	AI
D	1 1 0 1	–	–
E	1 1 1 0	–	AIL
F	1 1 1 1	DI	DI

(1) MUST BE SET Bx PIN TO '0' TO FORCE A PUP.

	CODES	NTRR (GCI ONLY, AUTO-MODE)		LTRR (GCI ONLY, AUTO-MODE)	
	C4 C3 C2 C1	**RXACT** (indications)	**TXACT** (commands)	**RXACT** (indications)	**TXACT** (commands)
0	0 0 0 0	DP/LSD	(1)	–	PUP/DR
1	0 0 0 1	EIU	RES	EIU	RES
2	0 0 1 0	–	–	–	–
3	0 0 1 1	–	–	–	–
4	0 1 0 0	EI	EI	EI	FA0
5	0 1 0 1	–	–	–	–
6	0 1 1 0	UAP	UAI	UAI	UAR
7	0 1 1 1	–	–	–	–
8	1 0 0 0	AP	AR	AP	AR
9	1 0 0 1	–	–	–	–
A	1 0 1 0	ARL	–	–	ARL
B	1 0 1 1	–	–	–	–
C	1 1 0 0	AI	AI	AI	AI
D	1 1 0 1	–	–	–	–
E	1 1 1 0	–	–	–	–
F	1 1 1 1	DI	DI	DI	DI

(1) MUST BE SET Bx PIN TO '0' TO FORCE A PUP.

(H1), AR instruction forces UID through the appropriate sequence to activate the line by sending TN followed by SN1. Beeing in the U-only-active state (H8A), AR command forces the sai bit equal 1 to the line. It is intended to transfer to the network an activation attempt at the S/T interface.

1011 (SP3): Send Single Pulse +3 and -3
SP3 test command forces UID to send +3, -3 pulses to the line, one pulse per frame.

1100 (AI): Activation Indicate
AI command forces act bit equal one in SN3 signal transmitted to the line. It reflects an activated state at the S/T interface.

1110 (AIL): Activation Indicate Loopback
Identical to AI command. Ensure direct compatibility with status indications of SID-GCI.

1111 (DI): Deactivation Indicate
The DI command allows the UID to automatically enter the power down state if the line is deactivated. DI command has no effect as long as the line is not deactivated (DI status indication reported).

0110 (UAP): U interface Activation pending
Is significant only when RR bit in CR2 has been set equal one or if NT-RR-AUTO mode is selected. UAP reports that the receiver is superframe synchronized with uoa bit received equal zero.

1000 (AP): Activation Pending
AP reports that the receiver is superframe synchronized with uoa bit received equal one .

1010 (ARL): Activation Request Loopback
Is significant only when NT1-AUTO or NT-RR-AUTO mode is selected. ARL reports that an eoc message has been received requiring to operate a local 2B+D loopback. When connected to SID-GCI in a NT1 or to UID in LT-RR-AUTO mode in a regenerator, 2B+D loopback command is therefore automatically provided.

1100 (AI): Activation Indication
AI reports that UID is superframe synchronized with act and uoa bits received equal one.

1111 (DI): Deactivation Indication
DI reports that UID has entered the deactivated state (H1).

NT mode: Status indication

0000 (DP/LSD): Deactivation Pending / Line Signal Detected
When in the deactivated state (H1) either powered up or down, LSD status indication is reported if TN wake-up tone is detected except if NT1 AUTO is selected; in this configuration, UID must check uoa bit before to send (or not) LSD. When in the superframe-synchronized states, DP status indication reports that the dea bit has been received equal zero from the line. UID enters in the receive reset state. When NT1-AUTO mode is selected, DP status indication is reported also when a transmission error has been detected on the loop. This is intended to ensure immediate deactivation of the S/T interface.

0001 (EIU): Error Indication User
EIU status indication is reported in following cases:

a. to acknowledge RES command. UID is deactivated, ready for a cold start.

b. to report a Loss of signal for more than 480ms on the line.

c. to report a Loss of synchronization for more than 480ms on the line.

d. to report that an expire of 15s Timer interrupt has reset UID ready for a cold start.

When NT1-AUTO is selected, EIU is replaced by DP.

0100 (EI): Error Indication
EI status indication reports that act bit has been detected equal zero.

LT mode: Command

0000 (PUP/DR): Power Up / Deactivation Request When in the power down state, PUP command powers up the device ready for a cold or a warm start. When in one of the superframe synchronized states, DR command forces dea bit on the line equal zero for four consecutive superframes before ceasing transmission.

0001 (RES): Reset
RES command resets UID ready for a cold start. Configuration registers are not changed. RES can be operated when the device is either powered up or down. If RES command is applied when the line is not fully deactivated, UID returns EIU indication and goes in J1 state (Receive Reset).
If RES command is applied when the line is not fully deactivated, UID properly ends the activation before to come back in J1 state; in this case EIU indication is returned.

0010 (SP1): Send Single Pulse +1 and-1
SP1 test command forces UID to send +1, -1, pulses to the line, one pulse per frame.

0011 (RDT): Random Data Transmitted
RDT test command forces UID to send data with random equiprobable levels at 80 kbaud.

0100 (FA0): Force act bit to 0
FA0 command forces the act bit to 0 in the SL3 signal transmitted to the line. It is intended to reflect a transmission failure detected on the network side of the loop relative to UID.

0101 (PDN): Power Down
PDN command forces UID to power down state. It should normally be used after UID has been set

in a known deactivated state, e.g. in an LT after a DI status indication has been reported. In GCI, C/I indication DI is sent twice on Br output before UID powers down.

0110 (UAR): U-interface-only Activation Request
Being in Power Up and deactivated , UAR command forces UID through the appropriate sequence to activate the loop without activating the S/T interface. SL2/SL3 signal is sent with uoa bit set to zero. With the line already active, UAR command forces bit uoa equal zero: this is intended to deactivate the S/T interface.

0111 (QM): Quiet Mode
This command has the same effect as in NT mode.

1000 (AR): Activation Request
Being Power Up and deactivated, AR instruction forces UID through the appropriate sequence to activate the line by sending TL followed by SL1. SL2/SL3 signal is sent with uoa bit equal one.
Beeing in the U-only-active states, AR command forces the uoa bit equal 1 to the line. AR is intended to activate the S/T interface.

1010 (ARL): Activation Request with Loopback
ARL test command forces UID through the appropriate sequence to activate with the complete transmit data stream looped-back to the receiver. When this loop-back is disabled by DR command, UID is ready to operate a warm start if a new ARL command is issued.

1011 (SP3): Send Single Pulse +3, -3
SP3 test command forces UID to send +3, -3 pulses to the line, one pulse per frame.

1100 (AI): Activation Indicate
AI is an optional command recognized only when BP2 bit in CR2 register is set equal one or LT-RR-AUTO mode is selected. Being in the superframe-synchronized state with act bit received from the line equal one, AI command allows UID to send act bit equal one to the line.

1111 (DI): Deactivation Indicate
The DI command allows the UID to automatically enter the power down state if the line is deactivated. DI command has no effect as long as the line is not deactivated (DI status indication reported).

LT mode: Status indication

0001 (EIU): Error Indication Interface U
It can be a "loss of signal", a "loss of sync." or an expiry of 15s timer. EIU is also the answer to the RES comand.
After sending EIU, the UID is always ready for a cold start.

0100 (EI): Error Indication
EI status indication reports that act bit has been detected equal zero.

0110 (UAI): U interface Activation Indication
UAI reports that the line is superframe synchronized.

1000 (AP): Activation Pending
Being in one of the deactivated states, AP reports that a wake up tone has been detected from the line. Beeing in the U-only-activated state, AP reports that sai bit has been detected equal one from the line. It is intended to reflect an activation attempt at the S/T interface.

1100 (AI): Activation Indication
AI reports that UID is superframe synchronized with act bit received equal one. TE side of the loop relative to the UID is active

1111 (DI): Deactivation Indication
DI reports that UID has entered the deactivated state (J1).

B1, B2 AND D CHANNELS TRANSPARENCY

UID is able to control automatically transparency of B1, B2 and D channels. Nevertheless, when ETC bit in CR2 register is set equal 1, transparency is forced as soon as the line is synchronized.
It is also possible to control each data channel B1, B2, D enabling at the DSI/GCI interface independently by means of bits EB1, EB2 and ED in CR4 register. Set to 1, B1, B2 or D channel on the DSI/GCI interface are enabled. In this case, out of the transparency state (s), ones are forced on the relevant time slot of the DSI/GCI, and ones or zeros are transmitted on the line conforming recommendations. Set equal 0, relevant time slot on DSI/GCI is always in high impedance state and ones or zeros are transmitted on the line. In this last case, as soon as transparency is enabled, ones are transmitted to the line.

When RDT test command is applied, transparency on 2B+D is forced. This intend to permit the user, if required, to send a random sequence of bits to the line. Please note that the on-chip scrambler normally ensures transmission of equiprobable levels to the line, even if logical one only is provided to the DSI/GCI system interface.

INTERNAL REGISTERS DESCRIPTION.

Here following a detailed description of STLC5412 internal registers.

Internal registers can be accessed:

a) In GCI mode, according to the Monitor channel exchange rules. For RXACT and TXACT also through C/I channel.

b) in µW/DSI mode, using the MICROWIRE interface according to the rules described in section "µW control interface".

Tables 8 and 10 gives the list of all STLC5412 internal registers.
Registers are grouped by types and address areas:

area 00/0FH: NOP operations.

area 10/1FH: test registers: reserved.

area 20/2FH: the configuration registers.
OPR CR1 CR2 CR3 CR4 CR5 CR6 CR7
Read Write access. CR5 only usefull in GCI mode

area 30/3FH: the B1 B2 D time slot registers.
TXB1 TXB2 RXB1 RXB2 TXD RXD STATUS
Read Write access except STATUS: Read only.
Usefull only in µW mode except STATUS: µW & GCI modes.

area 40/4FH: the transmit and receive registers (except EOC).
TXM4 RXM4 TXM56 RXM56 TXACT RXACT BEC1 BEC2 ECT1 ECT2 RXOH
Read Write access for the transmit registers:
TXM4 TXM56 TXACT
Read access only for the receive registers:
RXM4 RXM56 RXACT
Read Write access for the control registers:
ECT1 ECT2
Read access only for the error registers:
BEC1 BEC2
Write access only for the command registers:
RXOH

area 5x to Bx: for 12 bits registers.
5x: to write TXEOC register, to read RXEOC register.
6x: to read TXEOC register.
7x: reserved
8x & 9x: to read IDR register.
Ax: to write DECTEOC register
Bx: to read DECTEOC register

area C0/C3H: to read round trip delay registers

area C4H to Ex: reserved

area Fx: reserved except FF address: special register MWPS.

Overhead bits Programmable Register (OPR)
After reset: 1EH

CIE	EIE	FIE	OB1	OB0	OC1	OC0	C2E

CIE Near-End CRC Interrupt Enable:

CIE = 1: the RXM56 register is queued in the interrupt register stack with nebe bit set to zero each time the CRC result is not identical to the corresponding CRC received from the line.

CIE = 0: no interrupt is issued but the error detection remains active for instance for on chip error counting.

EIE Error counting Interrupt Enable:

EIE = 1: an interrupt is provided for the counter when the threshold (ECT1 or ECT2) is reached.

EIE= 0: no interrupt is issued. It is feasible to read the counters even if no relevant interrupt has been provided.

FIE FEBE Interrupt Enable:

FIE = 1: the RXM56 register is queued into the interrupt register stack each time the febe bit is received at zero in a superframe.

FIE = 0: no interrupt is issued but the receive febe bit remains active for on chip error counting.

OB1, OB0 Overhead Bit processing:

select how each spare overhead bit received from the line is validated and transmitted to the system. RXM4 and RXM56 registers are independently provided onto the system interface as for the eoc channel. Each spare overhead bit is validated independently from the others.

OB1	OB0	
0	0	each super frame, an interrupt is generated for the RXM4 or the RXM56 register. Spare bits are transparently transmited to the system.
0	1	an interrupt is set at each new spare overhead bit(s) received.
1	0	an interrupt is set at each new spare overhead bit(s) received and confirmed once. (two times identical).
1	1	an interrupt is set at each new spare overhead bit(s) received and confirmed twice. (three times identical).

If new bits are received at the same time in M4

and M56, both registers RXM4 and RXM56 are queued in the interrupt register stack.
Bits act, dea, uoa, sai are dedicated to the activation procedure. Validation is always done in accordance with the ANSI rule: validation at each new activation bit received and confirmed twice independently from the above rules. These bits are taken into account directly by the activation decoder. An interrupt is not generated for the RXM4 Register when one of these bits changes, but they are provided for test to the RXM4 Register.

OC1, OC0 eoc channel processing:

select how a received eoc message is validated and transmitted to the system.

OC1	OC0	
0	0	every half a super frame, an interrupt is generated for the RXEOC register. eoc channel is transparently transmitted to the system.
0	1	an interrupt is set at each new eoc message received.
1	0	an interrupt is set at each new eoc message received and confirmed once. (two times identical)
1	1	an interrupt is set at each new eoc message received and confirmed twice. (three times identical).

C2E Counter 2 enable:

C2E = 0: Only counter BEC1 is used for both febe and nebe counting.

C2E = 1: Counter BEC1 is used for nebe. Counter BEC2 is used for febe.

Configuration Register 1 (CR1)
After reset:
µW mode 00H
GCI: MO = 0 (LT/NT12) = C0H
GCI: MO = 1 (NT/TE) = D2H

FF1	FF0	CK2	CK1	CK0	DDM	CMS	BEX

FF1, FF0 Frame Format Selection: (µW/DSI only)
Refer to fig. 2 and 3.

FF1	FF2	
0	0	Format 1
0	1	Format 2
1	0	Format 3
1	1	Format 4 GCI like

CK0-CK2 Digital Interface Clock select: (µW/DSI only)
CK0-CK2 bits select the BCLK output frequency when DSI clocks are outputs.

CK2	CK1	CK0	BCLK frequency:
0	0	0	256KHz
0	0	1	512KHz
0	1	0	1536KHz
0	1	1	2048KHz
1	0	0	2560KHz

DDM Delayed Data Mode select:(µW/DSI only)
Two different phase-relations may be established between the Frame Sync signals and the first bit of the frame on the Digital Interface:

DDM = 0: Non delayed data mode The first bit of the frame begins nominally coincident with the rising edge of FSA/B.

DDM = 1: delayed data mode: FSA/B input must be set high at least a half cycle of BCLK earlier the frame beginning.

CMS Clocks Master Select:(µW/DSI only)

CMS = 0: BCLK, FSA and FSB are inputs; BCLK can have in Format 1, 2 and 3 value between 256KHz to 4096KHz, value in Format 4: 512KHz to 6176KHz.

CMS = 1: BCLK, FSA and FSB are outputs. FSA is a 8 kHz clock pulse indicating the frame beginning. FSB is a 8 kHz clock pulse indicating the second 8 bits wide time-slot. BCLK is a bit clock signal whose frequency is fixed bits CK2-CK0.

BEX B channels EXchange:

BEX = 0: B1 and B2 Tx/Rx channels are associated with TXB1/RXB1 and TXB2/RXB2 registers respectively.

BEX = 1: B1 and B2 channels are exchanged.

Configuration Register 2 (CR2)
After reset:
µW mode 00H
GCI: MO = 0 (LT/NT12) = 00H
GCI: MO = 1 (NT/TE) = 80H

µW (LT,NT):

SFS	NTS	DMO	DEN	ETC	BP1 EIF	BP2 BFH9D	RR

GCI (LT,NT):

SFS	NTS	T24D	CID	ETC	BP1 EIF	BP2 BFH9D	RR

SFS Super Frame Synchronization Select:
Significant in LT mode only.

SFS = 0: SFSx is an input that synchronizes the transmit superframe.

SFS = 1: SFSx is an output indicating the Transmit Superframe. In NT mode SFSx is always an output.

NTS LT / NT mode Select.

NTS = 0: LT mode selected

NTS = 1: NT mode selected

DMO D channel Transfer mode Select.(µW/DSI only)
Significant only when DEN=1.

DMO = 1: D channel data is shifted in and out on Dx and Dr pins in continuous mode at 16 kbit/s on the falling and rising edges of DCLK respectively.

DMO = 0: D channel data is shifted in and out on Dx and Dr pins in a TDM mode at the BCLK frequency on the falling and rising edges of BCLK respectively when the assigned time-slots are active.

T24D: 24ms timer disable (GCI only).

T24D = 1: The timer watches at the exchange on MONITOR channel every time the UID sends new byte. If it expires before pre-acknoledgement, an abort message is generated; In this last case, the aborted message is lost.

T24D = 0: The timer is desable. This means for instance that UID may wait an pre-acknoledgement for ever.

DEN D channel port Enable. (µW/DSI only)

DEN = 0: D channel port disabled. D bits are transferred on Br and Bx; Multiplexed mode is selected automatically.

DEN = 1: D channel port (DX, DR, and DCLK when DMO bit equal 1) is selected. D bits are transferred on Dr and Dx in a mode depending on DMO bit setting.

CID: C/I channel disable (GCI only).

CID = 0: TXACT and RXACT registers only accessible via the C/I channel.
Others registers only accessible via MONITOR channel.

CID = 1: All registers only accessible via the MONITOR channel.

ETC 2B+D Data Extended Transparency channel.

ETC = 1: 2B+D channel transparency is enabled as soon as the line is superframe synchronized.

ETC = 0: 2B+D channel transparency is under control of the on-chip state machine: act bit equal one both directions.

BP1 Break Point 1 during activation(significative only when NTS = 0: LT mode) .

BP1 = 1: During an activation attempt from the loop, (before SL2 sending) UID waits for an AR command to pursue activation. It is recommended to set BP1 equal 1 for repetor application.

BP1 = 0: The activation procedure is automatically processed without the need of an AR command.

EIF Error Indication Filter.
Significant in NT mode only

EIF = 0: act bit is set to zero in the transmit superframe in case of EI command, even if EI is sent sporadically.

EIF = 1: act bit may be not set to zero in the transmit superframe in case of EI command with a duration of less than 36ms.

BP2 Break Point 2 during activation. Significant only when NTS=0 (LT selected)

BP2 = 1: During a full activation procedure, UID receiving act bit set to one in the received SN3 signal, UID waits for an AI command to send act bit equal one in SL3 signal. It is recommended to set BP2 equal 1 for repetor application.

BP2 = 0: The activation procedure described above is automatically processed without the need of an AI command.

BFH9D: Back from H9 disabled. (Significant in NT mode only)

BFH9D = 0: UID is in H9 state (pending deactivation) after reception of dea bit = 0. It is waiting a loss of signal to return in H1 state via H12.

BFH9D = 1: UID is H9 state (pending deactivation) after reception of dea bit = 0. It is waiting a loss of signal to return in H1 state via H12, or dea bit = 1; In this last case UID returns in the previous state.

RR Repetor mode.

RR = 0: UID activation/deactivation complies with the standard requirements for NT1 or LT equipment depending on NTS bit select. See state matrix for the detailed behaviour of UID.

RR = 1: UID activation/deactivation complies with the requirements for repetor equipment. ”LT” or ”NT” behaviour is selected by means of bit NTS. BP1 and BP2 break-points should be set equal one too. See state matrix for the detailed behaviour of UID in this mode of operation.

Configuration Register 3 (CR3)
After reset: 00H

LB1	LB2	LBD	DB1	DB2	DBD	TLB	T15D

LB1, LB2, LBD Line side Loopback select.

When set high they turn each individual B1, B2, or D channel from the Line receive input to the Line transmit output. They may be set separately or together. The loopback is operated close to Bx and Br (or Dx and Dr if the D port is selected). These loop backs ensures channels integrity.

DB1, DB2, DBD Digital side Channel Loopback select.

When set high they turn each individual B1, B2, or D channel from the Digital Interface receive input to the Digital Interface transmit output. They may be set separately or together. The loopback is operated close to Bx and Br (or Dx and Dr if D port selected). These loop backs ensures channels integrity whatever the selected format or assigned channels time slot.

TLB Transparent Loopback select

TLB = 0: Digital loopbacks are non transparent. When line side loopback is set, data transmitted onto the digital interface is forced to one. When digital side loopback is set, data transmitted onto the line is forced to 1 in NT mode and to 0 in LT mode.

TLB = 1: 2B+D is transparently transferred through the UID.

T15D Timer 15 second disabled

T15D = 0: On-chip 15 second timer (timer 4 or 5 of ANSI standard) is enabled and ensure full reset of the activation procedure in case of non synchronization of the line within 15 second.

T15D = 1: On-chip 15 second timer is disabled. This means for instance that UID may attempt to synchronize for ever.

Configuration Register 4 (CR4)
After reset: E0H

EB1	EB2	ED	FFIT	ESFr	CTLIO	MOB	CTC

EB1 B1 channel Enabling

EB1 = 1: Selected B1 channel time-slot on the DSI/GCI interface is enabled. Note that transparency of B1 channel remains under control of the activation state machine and the ETC bit in CR2.

EB1 = 0: Selected B1 channel time-slot on the DSI/GCI interface is disabled: Br output remains in high impedance state and data on Bx input is ignored. Ones (NT) or zeroes (LT) are transmitted on the line.

EB2 B2 channel Enabling Identical to EB1 bit but for B2 channel.

ED D channel enabling identical to EB1 but for D channel on Bx/Br pin or DX/Dr pin depending on DEN bit in CR2 register.

FFIT FIFOs interrupt.

FFIT = 1: overflow or underflow of the TXFIFO and RXFIFO are reported in STATUS register. An interrupt is generated in µW mode, a MONITOR message is automatically sent in GCI mode.

FFIT = 0: No interrupt or message is generated when FIFOs overflow or underflow.

ESFr Enable SFSr on pin 25 (40)

ESFr = 0: $\overline{\text{LSD}}$ output is selected on pin 25 (40).

ESFr = 1: SFSr output is selected on pin 25 (40).

CTLIO Control IO (significant in GCI mode only)

CTLIO = 1: The input pins configurated via CR5 register generate a message on every change even if the UID is powered down in master mode; that is to say UID is able to wake up itself, to provide the clocks, to sends the message. After that UID is automatically powered down except if a PUP command is sent to it.

CTLIO = 0: In master mode and powered down, the UID does not react to an input pin change.

MOB Mask Overhead Bits.

MOB = 0: No Mask on overhead bit interrupts.

MOB = 1: All interrupts issued from RXM4, RXM56 RXEOC and CR5 are masked. It is still possible to read these registers via RXOH.

CTC Corrupted Transmit CRC Control

CTC = 0: Allows the normal calculation of the CRC for the transmitted data to the line.

CTC = 1: The CRC result transmitted to the line in the next Superframe is inverted. This ensure transmission of corrupted CRC as long as CTC equal 1.

Configuration Register 5 (CR5)
Significant in GCI only.

After reset: FFH

IO4	IO3	IO2	IO1	D4	D3	D2	D1

IO4, IO3, IO2, IO1 Input/Output select for I/O pins (14, 15, 16, 18)

IOi = 1: IOi pin is selected as an input. An on-chip pull up resistor ensures a stable logical 1 at power-on reset or if IOi pin is not connected to stable source.

IOi = 0: IOi pin is selected as an output.
Each I/O pin can be selected independently from the others.

D4, D3, D2, D1 I/O pin logical level command/status.

D4, D3, D2, D1 bits are associated with IO4, IO3, IO2, IO1 pins respectively. When IOi pin is selected as an output, the associated Di bit can be written to control the logical level of the output; Di equals 1 commands a high level on IOi. When IOi pin is selected as an input, the associated Di bit indicates the status of the input; Di equals one indicates a high level on IOi. CR5 register is buffered in the interrupt stack each time a status change is detected on an input. It is also possible to read-back at any time CR5.

Configuration Register 6 (CR6)

After reset: 0FH

T15E	ACTAUT	PUPAUT	QM	AIS	TFB0	RFS	LFS

T15E Timer 15 seconds extension

T15E = 0: The on chip T4 or T6 timer is done for the ANSI standard: 15 seconds.

T15E = 1: The on chip T4 or T5 timer is extended to 20 seconds.

Note: the T15D bit in CR3 register enables or disables the T4/T5 timer independently of theT15E bit.

ACTAUT: Activation Automatic

ACTAUT = 1: If UID is powered up, a 10KHz tone from the line starts the activation without need of extra commands (like AR), except when QM (Quiet mode) is enterred.

ACTAUT = 0 A detection of a 10KHz tone from the line does not start the activation: UID waits a primitive command (normaly AR).

PUPAUT PUP Automatic

PUPAUT = 1: A 10KHz tone from the line allows an automatic power up of the UID.

Notes if ACTAUT is also set to 1, from a power down state a 10KHz tone automatically starts the activation.

PUPAUT = 0: A detection of a 10KHz tone from the line does not power up the device: UID waits a PUP primitive command.

QM Quiet mode.

QM = 1: has the same effect of the QM primitive command enterred in TXACT register. An or logic is done with the QM bit and the QM primitive. The goal of this bit is to allow a quiet mode for an UID in power down state in some applications.

QM = 0: no effect.

AIS Analog Interface Select.

AIS = 1: selects an analog interface using 27mh transformer.

AIS = 0: selects an analog interface using 15mh transformer

TFB0 Transmit febe equal 0

TFB0 = 0: A permanent febe bit = 0 is sent on the line as long as TFB0 = 0

TFB0 = 1: The febe bit sent on the line is normaly computed.

RFS Remote febe select.

Please report to the figure 10. RFS is useful in repetor application to transfert or not the anomalies from the second line section to the first line section and viceversa.

RFS = 1: Transfer anomalies from second section to first section and viceversa allowed.

RFS = 0: Transfer anomalies from second section to first section and viceversa not allowed.

LFS Local febe select.

Please report to the figure 10. LFS is useful in repetor application to transfert or not the crc anomalies (nebe) of a line section to the febe bit of the same line section.

RFS = 0: The computed febe takes in to account the local nebe.

RFS = 1: The computed febe does not take in to account the local nebe.

Configuration Register 7 CR7

After reset: 02H

-	-	-	-	-	**LOCK**	**PL2EN**	**DECT**

DECT
DECT = 0: Normal mode
DECT = 1: DECT mode

PL2EN
PL2EN = 0: PLL2 remains frozen
PL2EN = 1: PLL2 tracks the phase of the receive signal.

LOCK
LOCK = 0: no phase relation between SFSr and FSa

LOCK = 1: The phase of SFSr and FSa rising edges is fixed

Configuration register TXB1
Significant only when format 3 selected.
(µW/DSI Only)

After reset: 00H Time slot 0 selected.

-	-	B1X5	B1X4	B1X3	B1X2	B1X1	B1X0

B1X5-B1X0 Transmit B1 Time Slot Assignment

Those bits define the binary number of the transmit B1 channel time-slot on Bx input. Time slot are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register RXB1
Significant only when format 3 selected.
(µW/DSI Only)

After reset: 00H Time slot 0 selected.

–	–	B1R5	B2R4	B2R3	B2R2	B2R1	B2R0

B1R5-B1R0 Receive B1 Time Slot Assignment

B1R5-B1R0 bits define the binary number of the receive B1 channel time-slot on BR output. Time slot are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register TXB2
Significant only when format 3 selected.
(µW/DSI Only)

After reset: 01H Time slot 1 selected.

-	-	B2X5	B2X4	B2X3	B2X2	B2X1	B2X0

B2X5-B2X0 Transmit B2 Time Slot Assignment

Those bits define the binary number of the transmit B2 channel time-slot on Bx input. Time slots are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register RXB2
Significant only when format 3 selected. (µW/DSI Only)
After reset: 01H Time slot 1 selected.

-	-	B2R5	B2R4	B2R3	B2R2	B2R1	B2R0

B2R5-B2R0 Receive B2 Time Slot Assignment

Those bits define the binary number of the receive B2 channel time-slot on BR output. Time slot are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register TXD
Significant only when format 3 is selected with the D channel selected in the multiplexed mode.
After reset:
µW mode 08H (sub time slot 0, time slot 2 selected)

DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0

DX5-SX0 Transmit D channel Time Slot Assignment

DX5-DX0 and SX1-SX0 bits define the binary number of the transmit D channel time-slot. DX5-DX0 bits define the binary number of the 8 bits wide timeslot. Time slot are numbered from 0 to 63. Within this selected time slot, SX1,SX0 bits define the binary number of the 2 bits wide time-slot. Sub time-slots are numbered 0 to 3. The register content is taken into account at each frame beginning.

Configuration register RXD
Significant only when format 3 is selected with the D channel selected in multiplexed mode.
After reset:
µW mode 08H (sub time slot 0, time slot 2 selected)

DR5	DR4	DR3	DR3	DR2	DR1	SR1	SR0

DR5-SR0 Receive D channel Time Slot Assignment

DR5-DR0 and SR1-SR0 bits define the binary number of the receive D channel time-slot. DR5-DR0 bits define the binary number of the 8 bits wide timeslot. Time slot are numbered from 0 to 63. Within this selected time slot., SR1,SR0 bits define the binary number of the 2 bits wide time-slot. Sub time-slots are numbered 0 to 3. The register content is taken into account at each frame beginning.

Status Register (STATUS)

(Read only)

After reset: 85H

PWDN	X	X	X	RXFFU	RXFFO	TXFFU	TXFFO

PWDN Power down

PWDN = 1: UID is in power down state

PWDN = 0: UID is in power up state

RXFFU RX FIFO underflow

RXFFU = 1: The bits rate on Br pin is higher than the bits rate side line.

RXFFU = 0: The bits rate on Br is in accordance with the bits rate side line

RXFFO: RX FIFO overflow

RXFFO = 1: The bits rate on Br pin is lower than the bits rate side line.

RXFFO = 0: The bits rate on Br pin is in accordance with the bits rate side line.

TXFFU TX FIFO underflow

TXFFU = 1: The bits rate on Bx pin is lower than the bits rate side line.

TXFFU = 0: The bits rate on Bx pin is in accordance with the bits rate side line.

TXFFO TX FIFO overflow

TXFFO = 1: The bits rate on Bx pin is higher than the bits rate side line.

TXFFO = 0: The bits rate on Bx pin is in accordance with the bits rate side line.

When one of these four bits is set to 1, Tx FIFO and/or Rx FIFO is re-adjusted and data is lost. An interrupt or message is generated if FFIT bit in CR4 register is set to 1. It is always possible to read this register by writting STATUS bit = 1 in RXOH register.

Transmit M4 channel Register (TXM4)

After reset: 7DH

-	$m42_X$	$m43_X$	$m44_X$	$m45_X$	$m46_X$	-	$m48_X$

When transmitting SL2/SL3 or SN3, the UID shall continuously send in the M4 channel field the register content to the line once per superframe. Register content is transmitted to the line at each superframe.
$m41_X$, $m42_X$ in LT, $m47_X$ are activation bits. These bits are controlled directly by the on chip activation encoder-decoder. The corresponding bits in the TXM4 register are not significant.

$m45_X$ in NT mode is CS0 bit: this is normally 0 (UID performing warm start). Nevertheless, user can force CSO to 1 by setting $m45_X$ to 1.

When a read back is operated on TXM4, m41x, m42x in LT, m47x are indicating the current value of act, dea in LT and uoa/sai bits transmitted to the line.

Receive spare M4 overhead bits Register (RXM4) (read only)

After reset: 75H

m41r	m42r	m43r	m44r	m45r	m46r	m47r	m48r

RXM4 Register is constituted of 8 bits. When the line is fully activated (super frame synchronized), STLC5412 extracts the M4 channel bits. m41 is the act bit; m42 in NT mode is the dea bit; in NT m47 is the uoa bit; in LT m47 is the sai bit. These bits are under the control of the activation sequencer. No interrupt cycle is provided for the RXM4 register when a change on one of the activation bits is detected; never the less, they are available in RXM4.
When one of the remaining received spare bits is validated following the criteria selected in the Configuration Register OPR, the RXM4 register content is queued in the interrupt register stack, if no mask overhead bits is set (see MOB bit in CR4 register). It is always possible to read this register by writting RXM4 bit = 1 in RXOH register.

Transmit M5 and M6 channels Register (TXM56)

After reset: 1FH

-	-	-	$m51_X$	$m61_X$	$m52_X$	febx	febx

$m51_X$, $m61_X$, $m52_X$ spare over-head bits are normally equal to 1. Default value can be changed by setting the respective bits. These bits are transmitted to the line in SL2/SL3 or SN3 signal.

febx Transmit febe bit control
The febe can be forced to 0 by writing 0 in one of febx if RFS bit in CR6 register is set to 1. The febe bit set to zero is sent once to the line in the following available superframe. After febe transmission, febx

bit returns to 1; the two bits positions are identical and allow direct compatibility between UIDs set in auto-mode (repeter).

Note: the febx bits in TXM56 register are not the only way to force febe = 0 to the line.
First, the febx action is controlled by RFS bit in CR6 register.
Second, the nebe = 0 (local crc cmputing result) forces also febe = 0 to the line and this action is controlled by LFS bit in CR6 register.
Third, TFB0 = 0 in CR6 register forces permanentely febe = 0 to the line.

Receive M5 and M6 overhead bits Register (RXM56) (read only)

After reset: 1FH

-	-	-	m51r	m61r	m52r	febr	nebr

When the line is fully activated (super frame synchronized), STLC5412 extracts the overhead bits. When one of the received spare bits m51, m61, m52 is validated following the criterias selected in the Configuration Register OPR. The RXM56 register content is queued in the interrupt register stack, if no mask overhead bits is set (see MOB bit in CR4 register). If the FIE bit in OPR register is set high, the RXM56 register content is queued in the interrupt register stack each time the febe bit is received equal zero with bit feb equal 0.
The CRC received from the far-end is compared at the end of the superframe with the CRC calculated by the UID during that superframe. If an error is detected, the febe bit in the transmit direction is forced equal zero in the next superframe. If the CIE bit in the OPR register is set high, the RXM56 register is queued in the interrupt register stack at each CRC error detected with bit neb equal zero. It is always possible to read this register by writing RXM56 bit = 1 in RXOH register.

Activation control register (TXACT)

After reset: 0FH

-	-	-	-	C4	C3	C2	C1

This register is constituted of four bits: (C1, C2, C3, C4). In GCI mode, this register is normaly addressed by means of the C/I channel, but it is possible to address it by means of the MONITOR channel (see CID bit in CR2 register).

Activation indication register (RXACT)

(read only)

After reset: 0FH

-	-	-	-	C4r	C3r	C2r	C1r

This Register is constituted of four bits: (C1r, C2r, C3r, C4r). At each activation status change, RXACT is queued in the interrupt register stack. In GCI mode, the C1-C4 bits are directly sent on the C/I channel or monitor channel depending on the CID bit in CR2 register. Activation Indication instructions are coded on 4 bits according to activation control description. It is always possible to read this register by writting RXACT bit = 1 in RXOH register.

Block Error Counter 1 (BEC1)

(read only)

After reset: 00H

ec7	ec6	ec5	ec4	ec3	ec2	ec1	ec0

This Register indicates the binary value of the Block Error up-counter 1. Error are counted according to C2E bit setting in register OPR (nebe + febe or nebe only). When counter one reachs the threshold ECT1, BEC1 register is queued in the interrupt stack. BEC1 is reset to zero when it is read.

Block Error Counter 2 (BEC2)

(read only)

After reset: 00H

ec7	ec6	ec5	ec4	ec3	ec2	ec1	ec0

This Register indicates the binary value of the Block Error up-counter 2. Febe errors are always counted. According to C2E bit setting in register OPR, when counter one reachs the threshold ECT2, BEC2 register is queued in the interrupt stack. BEC2 is reset to zero when it is read.

Threshold Block Error Counter 1 register (ECT1)

After reset: FFH

ect17	ect16	ect15	ect14	ect13	ect12	ect11

It is possible to load in this register the binary value of a threshold for the Block Error counter 1.When Block error counter reachs this value, an Interrupt relative to BEC1 register is loaded in the interrupt stack. This can be used as an early alarm in case of degraded transmission.

Threshold Block Error Counter 2 register (ECT2)

After reset: FFH

ect27	ect26	ect25	ect24	ect23	ect22	ect21

It is possible to load in this register the binary value of a threshold for the Block Error counter 2.

When Block error counter reachs this value, an Interrupt relative to BEC2 register is loaded in the interrupt stack. This can be used as an early alarm in case of degraded transmission.

Receive status Register - read command (RXOH) (Write only)

EOC	M4	M56	ACT	0	STATUS	0	RST

Reset to zero of all the RXOH bits is automatic.

EOC Receive EOC status register read.

When EOC bit is set to one, UID automatically loads the current value of RXEOC register in the interrupt stack independently of any status change.

M4 Receive M4 overhead bits status register read.

When M4 bit is set to one, UID automatically loads the current value of RXM4 register in the interrupt stack independently of any status change.

M56 Receive M5 and M6 overhead bits status register read.

When M56 bit is set to one, UID automatically loads the current value of RXM56 register in the interrupt stack independently of any status change.

ACT Activation indication status.

When ACT bit is set to one, UID automatically loads the current value of RXACT register in the interrupt stack independently of any status change.
In GCI mode, the RXACT read back always uses the monitor channel.

STATUS

When STATUS bit is set to one, UID automatically loads the current value of STATUS register in the interrupt stack independently of any status change.

RST RESET (MICROWIRE/DSI configuration only).

When RST bit is set to one, UID is fully reset including configuration registers, state machine and all coefficients and reset to their default value. UID enters in the power-down state.

Transmit EOC register (TXEOC)

After reset: FFFH

XEOC1	XEOC2	XEOC3	XEOC4	XEOC5	XEOC6	XEOC7	XEOC8

TXEOC Register is constituted of 12 bits, 3 bits address (EFG), 1 bit data/message Flag (H), 8 bits information (XEOC1 - XEOC8). When transmitting SL2/SL3 or SN3 signal. STLC5412 shall continuously send into the EOC channel field the eoc bits twice per superframe. TXEOC register is loaded in the transmit register at each half a superframe.

The address of this register is composed only of 4 bits. Read-back can be performed by means of a read-back command 6100H.

Dect Mode Eoc Register (DECTEOC)

After reset: FFFH

DEOC1	DEOC2	DEOC3	DEOC4	DEOC5	DEOC6	DEOC7	DEOC8

12 bits register to store the DECT EOC message, 3 bits address (EFG), 1 bit data/message Flag (H), 8 bits information (DEOC1 - DEOC8) This register is significant only in DECT mode. In LT DECT mode the byte is transmitted 3 times in the EOC channel starting from the superframe identified by the DECSYNC pulse on the SFSx pin. Once the DECTEOC byte has been transmitted 3 times, the content of the EOC channel returns to the previous existing value. In NT DECT mode if the received EOC message field is detected 3 times identical to the DECTEOC register, the device generates a pulse on the pin SFSx synchronous with the SFSr pulse. Read back can be performed by means of command B100H.

Receive EOC register (RXEOC)

(read only)
After reset: FFFH

REOC1	REOC2	REOC3	REOC4	REOC5	REOC6	REOC7	REOC8

The RX EOC Register is constituted of 12 bits. When the line is fully activated (super frame synchronized) and when a new eoc message is received and validated in accordance with the criteria selected in the Configuration Register OPR, the RX EOC Register is queued in the interrupt register stack. The address of this register is composed only of 4 bits.
It is always possible to read this register by writing EOC = 1 in RXOH register

Identification Register (IDR)
Fixed value: CCCC 00001000
(read only 12 bit register)

When a read-back operation of IDR register is entered, UID loads the Identification Register in the interrupt stack. This register provides a reserved identification code agreed by GCI standard:
CCCC 00001000

IDR register is accessible via two addresses (See page 34).

MWPS Micro Wire Port Select register (Significant in microwire mode only).
(write only)

Default value: Mode A (5410 compatible)

- Writting FFH value select the mode B to exchange data onto CI & CO
- Writing 00H value select the mode A (See Microwire control interface paragraph for more details Mode A, Mode B).

Note: Soft Reset has no effect on the select mode.

BAUD DELAY Register (DBAUD)

After reset: 00H

DBAUD7	DBAUD6	DBAUD5	DBAUD4	DBAUD3	DBAUD2	DBAUD1	DBAUD0

8 bits read-only register that provides the round trip bauds delay (12.5usec step). It is significant in LT mode only. The register is split in two sections:

DBAUD4..DBAUD0: 5 bits counter of bauds delay between SFSx and SFSr rising edges (**total digital delay: tdd**).

DBAUD7..DBAUD5: 3 bits to store the internal elastic memory (FIFO) state. The table A shows the coding of the 3-stages elastic memory (**elastic digital delay: edd**).

Table A.

FIFO state	baud delay (edd)
000	-1
010	-2
110	0

-2: 2 bauds have to be subtracted from bauds counter value (DBAUD4..DBAUD0)

-1: 1 baud has to be subtracted to bauds counter value (DBAUD4..DBAUD0)

0: no correction

All other FIFO states are used during activation procedure. Once PLL2 is frozen you can be only in one of the 3 states in table A.

TX RX Clocks Different Register (DTXRX)

After reset: 00H

7	6	5	4	3	2	1	0

8bits read-only register that provides the phase difference between transmit clock and receive recovered clock by PLL2 in steps of 65.1 nsec. (**clock elastic delay: ced**). The register is significant in LT mode only.

Table 8: REGISTER ACCESS MESSAGES

FUNCTION		BYTE 1			BYTE 2							
		AD7/4	AD3/1	AD0	7	6	5	4	3	2	1	0
NOP		0000	000	0	0	0	0	0	0	0	0	0
RESERVED		0001	XXX	X	0	0	0	0	0	0	0	0
OPR	W	0010	000	0	CIE	EIE	FIE	OB1	OB0	0C1	0C0	C2E
OPR	R	0010	000	1	0	0	0	0	0	0	0	0
CR1	W	0010	001	0	FF1	FF0	CK2	CK1	CK0	DDM	CMS	BEX
CR1	R	0010	001	1	0	0	0	0	0	0	0	0
CR2	W	0010	010	0	SFS	NTS	DMO	DEN	ETC	BP1	BP2	RR
CR2	R	0010	010	1	0	0	0	0	0	0	0	0
CR3	W	0010	011	0	LB1	LB2	LBD	DB1	DB2	DBD	TLB	T15D
CR3	R	0010	011	1	0	0	0	0	0	0	0	0
CR4	W	0010	100	0	EB1	EB2	ED	FFIT	ESFr	CTLIO	MOB	CTC
CR4	R	0010	100	1	0	0	0	0	0	0	0	0
CR5	W	0010	101	0	IO4	IO3	IO2	IO1	D4	D3	D2	D1
CR5	R	0010	101	1	0	0	0	0	0	0	0	0
CR6	W	0010	110	0	T15E	ACTAUT	PUPAUT	QM	AIS	TFB0	RFS	LFS
CR6	R	0010	110	1	0	0	0	0	0	0	0	0
CR7	W	0010	111	0	0	0	0	0	0	LOCK	PL2EN	DECT
CR7	R	0010	111	1	0	0	0	0	0	0	0	0
TXB1	W	0011	000	0	0	0	B1X5	B1X4	B1X3	B1X2	B1X1	B1X0
TXB1	R	0011	000	1	0	0	0	0	0	0	0	0
TXB2	W	0011	001	0	0	0	B2X5	B2X4	B2X3	B2X2	B2X1	B2X0
TXB2	R	0011	001	1	0	0	0	0	0	0	0	0
RXB1	W	0011	010	0	0	0	B1R5	B1R4	B1R3	B1R2	B1R1	B1R0
RXB1	R	0011	010	1	0	0	0	0	0	0	0	0
RXB2	W	0011	011	0	0	0	B2R5	B2R4	B2R3	B2R2	B2R1	B2R0
RXB2	R	0011	011	1	0	0	0	0	0	0	0	0
TXD	W	0011	100	0	DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0
TXD	R	0011	100	1	0	0	0	0	0	0	0	0
RXD	W	0011	101	0	DR5	DR4	DR3	DR2	DR1	DR0	SR1	SR0
RXD	R	0011	101	1	0	0	0	0	0	0	0	0
RESERVED		0011	11X	X	0	0	0	0	0	0	0	0

Notes:

1. Bit 7 of byte 1 is the first bit clocked into the UID.
2. All configuration registers can be read-back by setting bit 7 of BYTE 1 equal 1
3. RXOH is a Write only register to force RXEOC, RXM4, RXM56, RXACT status register sending. RST reset the device
4. It is recommended not to access all RESERVED adresses. X means 1 or 0

W refers to a write operation.
R refers to a request for read-back.

Table 8: REGISTER ACCESS MESSAGES (Continued)

FUNCTION		BYTE 1			BYTE 2							
		AD7/4	AD3/1	AD0	7	6	5	4	3	2	1	0
TXM4	W	0100	000	0	0	M42x	M43x	M44x	M45x	M46x	0	M48x
TXM4	R	0100	000	1	0	0	0	0	0	0	0	0
TXM56	W	0100	001	0	0	0	0	M51x	M61x	M52x	FEBx	FEBx
TXM56	R	0100	001	1	0	0	0	0	0	0	0	0
TXACT	W	0100	010	0	0	0	0	0	C4x	C3x	C2x	C1x
TXACT	R	0100	010	1	0	0	0	0	0	0	0	0
BEC1	R	0100	011	1	0	0	0	0	0	0	0	0
BEC2	R	0100	100	1	0	0	0	0	0	0	0	0
ECT1	W	0100	101	0	ECT17	ECT16	ECT15	ECT14	ECT13	ECT12	ECT11	ECT10
ECT1	R	0100	101	1	0	0	0	0	0	0	0	0
ECT2	W	0100	110	0	ECT27	ECT26	ECT25	ECT24	ECT23	ECT22	ECT21	ECT20
ECT2	R	0100	110	1	0	0	0	0	0	0	0	0
RXOH	W	0100	111	0	EOC	M4	M56	ACT	0	STATUS	0	RST
RESERVED		0100	111	1	0	0	0	0	0	0	0	0
TXEOC	W	0101	EFG	H	XEOC1	XEOC2	XEOC3	XEOC4	XEOC5	XEOC6	XEOC7	XEOC8
TXEOC	R	0110	000	1	0	0	0	0	0	0	0	0
RESERVED		0111	XXX	X	0	0	0	0	0	0	0	0
IDR	R	100X	000	0	0	0	0	0	0	0	0	0
DECTEOC	W	1010	EFG	H	DEOC1	DEOC2	DEOC3	DEOC4	DEOC5	DEOC6	DEOC7	DEOC8
DECTEOC	R	1011	000	1	0	0	0	0	0	0	0	0
RESERVED		1100	XXX	0	0	0	0	0	0	0	0	0
DBAUD	R	1100	000	1	0	0	0	0	0	0	0	0
DTXRX	R	1100	001	1	0	0	0	0	0	0	0	0
RESERVED		1100	X1X	X	0	0	0	0	0	0	0	0
FREE		1101	XXX	X	0	0	0	0	0	0	0	0
FREE		1110	XXX	X	0	0	0	0	0	0	0	0
MWPS	W	1111	111	0	FF = Mode B					00 = Mode A		

Notes:

1. All transmit registers can be read-back by setting bit 7 of BYTE 1 equal 1 except for TXEOC and DECT EOC registers. To read-back TXEOC, use the command 61-00 H, to read back DECT EOC use command B1-00H..

2. BEC1, BEC2 and IDR are read-only registers.

3. FREE adresses are ignored by the device.

4. In the TXEOC and DECTEOC registers:
   E = ea1, the msb of the EOC destination address
   F = ea2
   G = ea3
   H = dm, the EOC data/message mode indicator

5. M42x is significant in NT mode only

Table 9: READ BACK MESSAGES

FUNCTION	BYTE 1			BYTE 2							
	AD7/4	AD3/1	AD0	7	6	5	4	3	2	1	0
OPR	0010	000	1	CIE	EIE	FIE	OB1	OB0	0C1	0C0	C2E
CR1	0010	001	1	FF1	FF0	CK2	CK1	CK0	DDM	CMS	BEX
CR2	0010	010	1	SFS	NTS	DMO	DEN	ETC	BP1	BP2	RR
CR3	0010	011	1	LB1	LB2	LBD	DB1	DB2	DBD	TLB	T15D
CR4	0010	100	1	EB1	EB2	ED	FFIT	ESFr	CTLIO	MOB	CTC
CR5	0010	101	1	I04	I03	I02	I01	D4	D3	D2	D1
CR6	0010	110	1	T1SE	ACTUAT	PUPAUT	QM	AIS	TFB0	RFS	LFS
CR7	0010	111	1	0	0	0	0	0	LOCK	PL2EN	DECT
TXB1	0011	000	1	0	0	B1X5	B1X4	B1X3	B1X2	B1X1	B1X0
TXB2	0011	001	1	0	0	B2X5	B2X4	B2X3	B2X2	B2X1	B2X0
RXB1	0011	010	1	0	0	B1R5	B1R4	B1R3	B1R2	B1R1	B1R0
RXB2	0011	011	1	0	0	B2R5	B2R4	B2R3	B2R2	B2R1	B2R0
TXD	0011	100	1	DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0
RXD	0011	101	1	DR5	DR4	DR3	DR2	DR1	DR0	SR1	SR0
TXM4	0100	000	1	0	M42x	M43x	M44x	M45x	M46x	0	M48x
TXM56	0100	001	1	0	0	0	M51x	M61x	M52x	FEBx	FEBx
TXACT	0100	010	1	0	0	0	0	C4x	C3x	C2x	C1x
BEC1	0100	011	1	c7	c6	c5	c4	c3	c2	c1	c0
BEC2	0100	100	1	c7	c6	c5	c4	c3	c2	c1	c0
ECT1	0100	101	1	ECT17	ECT16	ECT15	ECT14	ECT13	ECT12	ECT11	ECT10
ECT2	0100	110	1	ECT27	ECT26	ECT25	ECT24	ECT23	ECT22	ECT21	ECT20
TXEOC	0110	EFG	H	XEOC1	XEOC2	XEOC3	XEOC4	XEOC5	XEOC6	XEOC7	XEOC8
IDR	1000	CCC	C	0	0	0	0	1	0	0	0
DECTEOC	1011	EFG	H	DEOC1	DEOC2	DEOC3	DEOC4	DEOC5	DEOC6	DEOC7	DEOC8
DBAUD	1100	000	1	DBAUD7	DBAUD6	DBAUD5	DBAUD4	DBAUD3	DBAUD2	DBAUD1	DBAUD0
DTXRX	1100	001	1	DTXRX7	DTXRX6	DTXRX5	DTXRX4	DTXRX3	DTXRX2	DTXRX1	DTXRX0

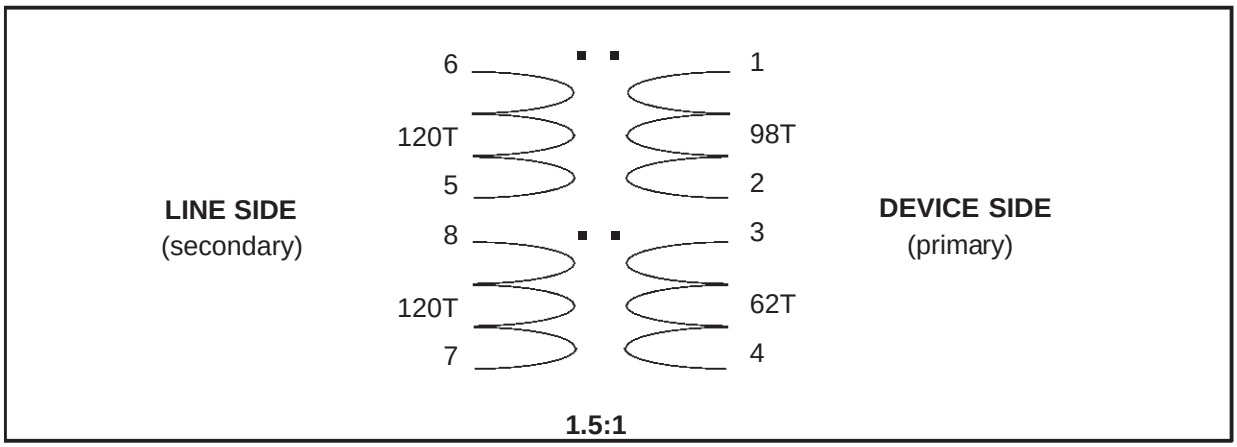
Notes:
1. For all these registers with the exception of TXEOC, bit 0 of BYTE 1 is set to 1 to indicate read-back message.
2. CR5 configuration/status register is listed with status registers.
3. Bit 7 of BYTE 1 is the first clocked out from the UID.
4. M42x is significant in NT mode only

Table 10: SPONTANEOUS OR DRIVEN MESSAGES

FUNCTION	BYTE 1			BYTE 2							
	AD7/4	AD3/1	AD0	7	6	5	4	3	2	1	0
CR5	0010	101	0	IO4	IO3	IO2	IO1	D4	D3	D2	D1
STATUS	0011	111	0	PWDN	0	0	0	RxFFU	RxFFO	TxFFU	TxFFO
RXM4	0100	000	0	M41R	M42R	M43R	M44R	M45R	M46R	M47R	M48R
RXM56	0100	001	0	0	0	0	M51R	M61R	M52R	FEBR	NEBR
RXACT	0100	010	0	0	0	0	0	C4R	C3R	C2R	C1R
BEC1	0100	011	0	c7	c6	c5	c4	c3	c2	c1	c0
BEC2	0100	100	0	c7	c6	c5	c4	c3	c2	c1	c0
RXEOC	0101	EFG	H	REOC1	REOC2	REOC3	REOC4	REOC5	REOC6	REOC7	REOC8

Notes:
1. All status registers can be read by setting first the appropriate command. At any status change, an interrupt cycle is issued.
2. In the RXEOC register:
   E = ea1
   F = ea2
   G = ea3
   H = d=0/m = 1
3. For all These registers with the exception of RXEOC, bit 0 of BYTE 1 is set to 0 to indicate a status register.

Figure 11: Transformer Design.



Line Interface Circuit

It is very important, comply with ANSI, ETSI and French standards, that the recommended line interface circuit should be strictly adhered to. The channel response and dynamic range of this circuit have been carefully designed as an integral part of the overall signal processing system to ensure that the performance requirements are met under all the specified loop conditions. Deviations from this design are likely to result in sub-optimal performance or even total failure of the system on some types of loops.

Turns Ratio: Np:Ns = 1:1.5.
Secondary Inductance: Lp 27mH.
Max leakage inductance: 100µH
Winding Resistances: 30 ohms (2.25Rp + Rs) > 10 ohms.
Return Loss, at 40 kHz and load of 135 ohms: 26 dB. Saturation characteristics: THD –70dB when tested with 50mA d.c. through the secondary and a 40kHz sine-wave injected into the primary at a level which generates, at the secondary, $5V_{P-P}$ (R_{load} = 135ohms).

List of suppliers:

SHOTT
PULSE ENGINEERING

Table 11.

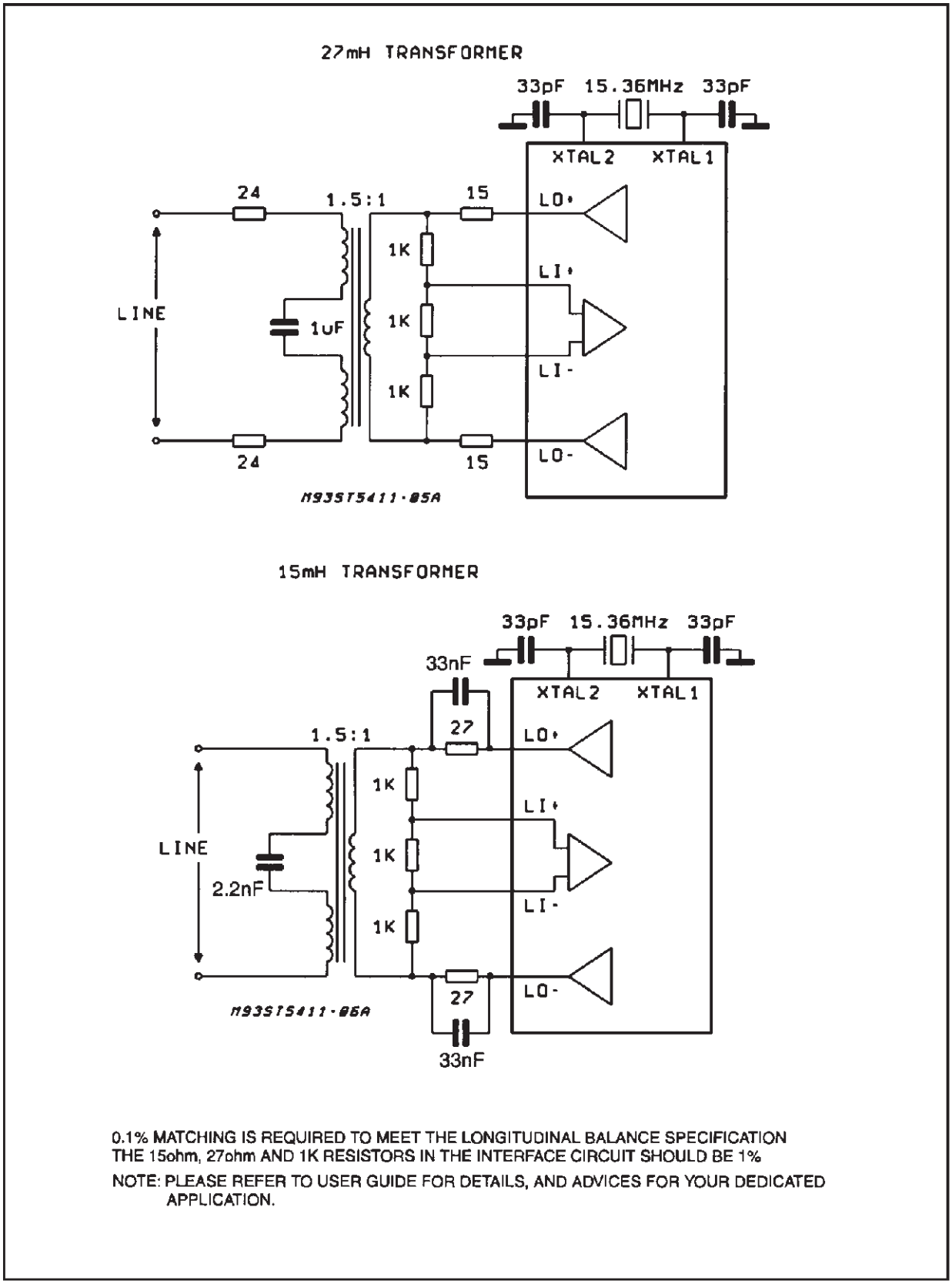
WINDING	NUMBER OF TURNS	WIRE GAUGE
1-2	98 Single	#34 AWG
6-5, 8-7	120+120 Bifilar	#36 AWG
3-4	62 Single	#34 AWG

WINDING	INDUCTANCE	RESISTANCE
1-2 + 3-4	12 mH	less than 5Ω
5-6 + 7-8	27 mH	less than 10 Ω

Board Layout

While the pins of the UID are well protected against electrical misuse, it is recommended that the standard CMOS practise, of applying GND to the device before any other connections are made, should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used. Great care must be taken in the layout of the printed circuit board in order to preserve the high transmission performance of the STLC5412. To maximize performance, do not use the philosophy of separating analog and digital grounds for chip. All GND pins should be connected together as close as possible to the pins, and the VCC pins should be strapped together. All ground connections to each device should meet at a common point as close as possible to the GND pins to prevent the interaction of ground return currents flowing through a common bus impedance. Two decoupling capacitors of 10µF and 0.1µF should be connected from this common point to VCC pins as close as possible to the chip. Taking care with the board layout in the following ways will also help prevent noise injection into the receiver frontend and maximize the transmission performances. Keep the crystal oscillator components away from the receiver inputs and use a shielded ground plane around these components. Keep the device, the components connected to LI+/LI- and the transformer as close possible. Symmetrical layout for the line interface is suggested.

Figure 12: Recommended connections.



0.1% MATCHING IS REQUIRED TO MEET THE LONGITUDINAL BALANCE SPECIFICATION
THE 15ohm, 27ohm AND 1K RESISTORS IN THE INTERFACE CIRCUIT SHOULD BE 1%

NOTE: PLEASE REFER TO USER GUIDE FOR DETAILS, AND ADVICES FOR YOUR DEDICATED APPLICATION.

Figure 13a: LT Application.

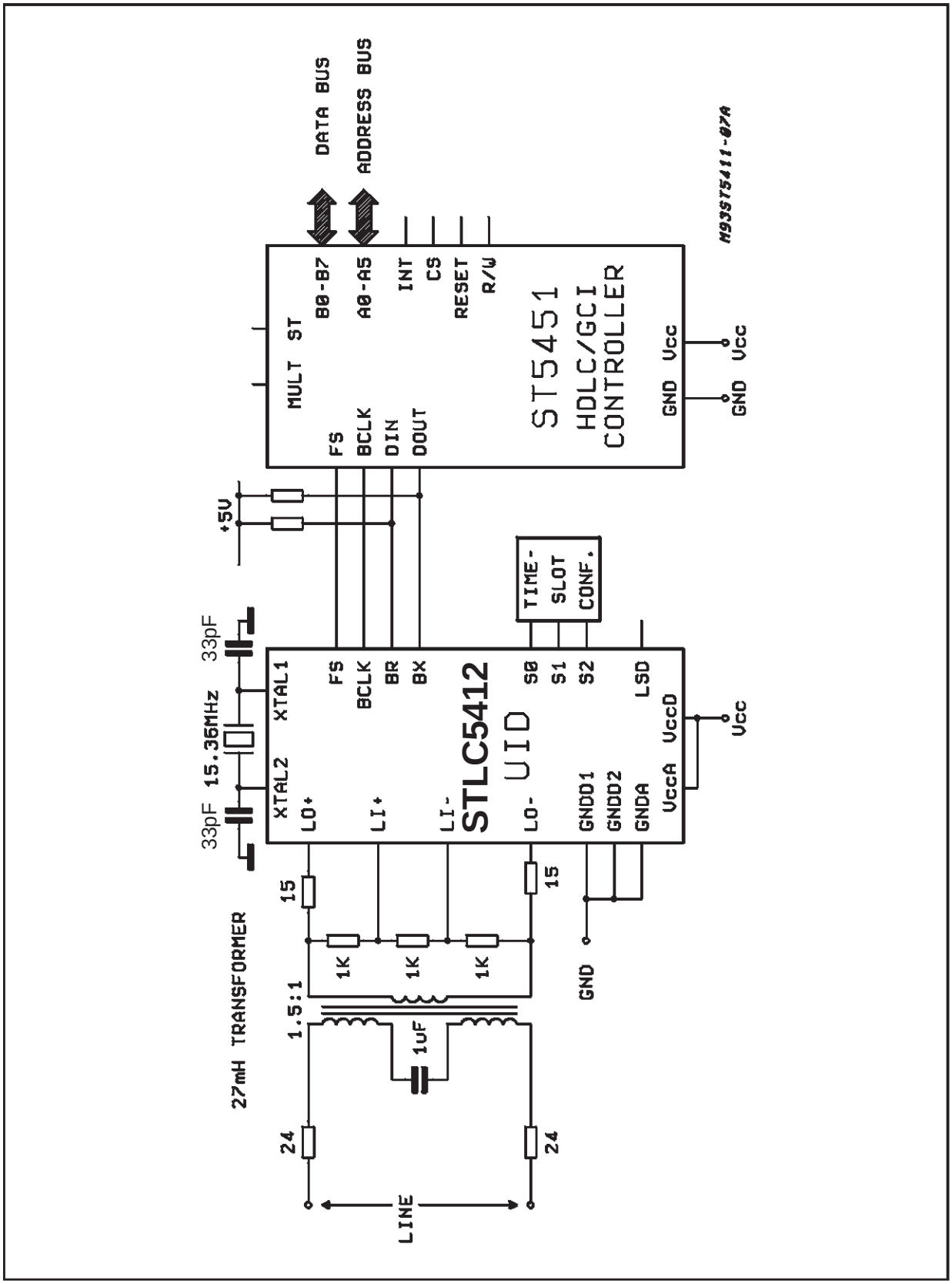


Figure 13b: LT Application.

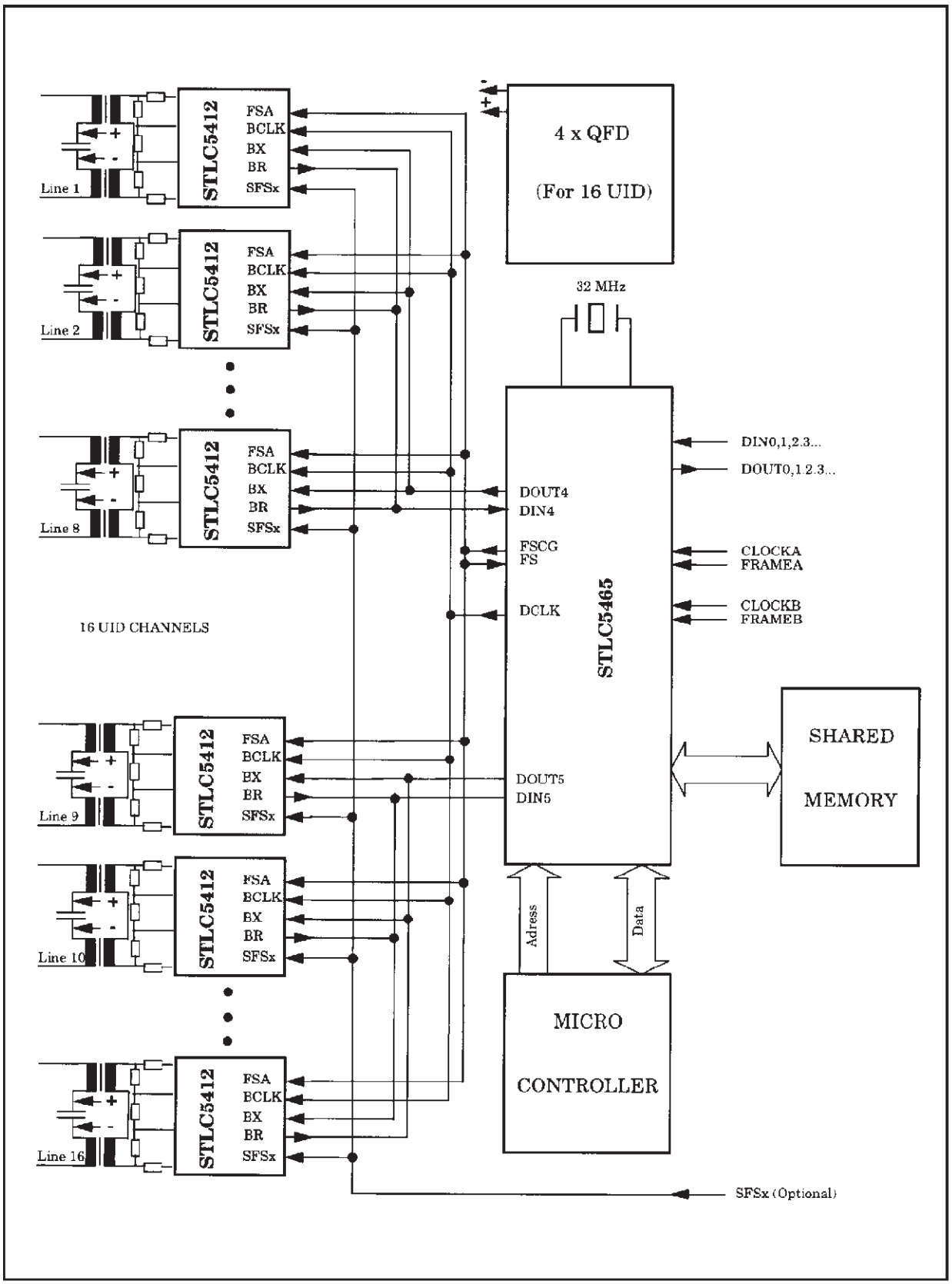
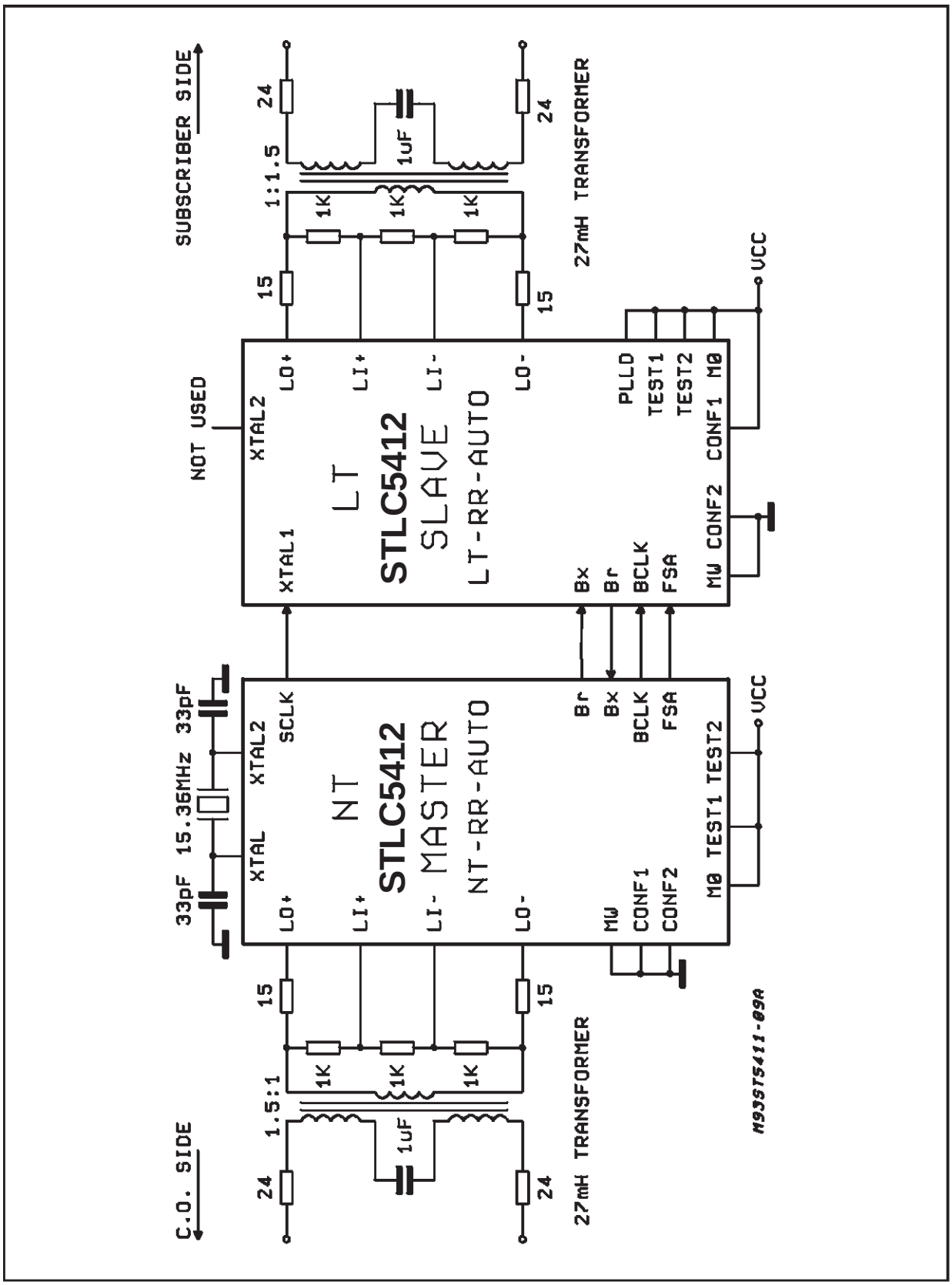


Figure 13c: RR Application.



APPENDIX A - STATE MATRIX

EVENTS		STATE NAME	Power Off	Full Reset	Alting	Awake	EC Timing	WAIT SN2	CHECK SN2	EC CYCED	EC CVG. UAO	SW SYNC	SW SYN UAO	ISW SYNC	TRANSIT BP2/TAO	TRANSIT AR	U & ST ACTIVE	Pending DEACTar	U only ACTIVE	Pding ACTIVEar	DEACT. Admin	Pding DEACT.	TEAR DOWN	RECV RESET
		STATE CODE	J0	J1	J2	J3	J4	J41	J42	J5	J5A	J6	J6A	J7	J79	J78R	J8	J8AP	J8A	J8P	J9	J11	J10	J12
	U LINE TX		SL0	SL0	TL	SL0	SL1	SL2 act = 0 dea = 1 uoa = (4)	SL2 act = 0 dea = 1 uoa = *	SL2 act = 0 dea = 1 uoa = 1	SL2 act = 0 dea = 1 uoa = 0	SL2 act = 0 dea = 1 uoa = 1	SL2 act = 0 dea = 1 uoa = 0	SL3 act (3) dea = 1 uoa = 1	SL3 act (3) dea = 1 uoa = 1	SL3 act = 1 dea = 1 uoa = 1	SL3 act = 1 dea = 1 uoa = 1	SL3 act = * dea = 1 uoa = 1	SL3 act = 0 dea = 1 uoa = 0	SL3 act = 0 dea = 1 uoa = 0	SL3 act = * dea = 0 uoa = *	SL0	SL0	SL0	SL0
← MOST	POWER ON # GCI only	J1 D#	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	LOSS OF POWER	/	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0
	RES COMMAND	/	/	J1	sp T5 J10 EIU (1)	sp T5 J10 EIU (1)	sp T5 J10 EIU (1)	sp T5 J10 EIU (1)	sp T5 J10 EIU (1)	sp T5 J10 EIU (1)	sp T5 J10 EIU (1)	sp T5 J10 EIU (1)	sp T5 J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	/	/	/	/	/
	EXPIRY OF TIMER 5 (15 seconds)	/	/	/	/	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	/	/	/	/	/	/	/	/	/	/	/	/
	LOSS OF SIGNAL (>480ms)	/	/	/	/	/	/	/	/	/	/	/	/	st T7 J12 EIU (1)	st T7 J12 EIU (1)	st T7 J12 EIU (1)	st T7 J12 EIU (1)	st T7 J12 EIU (1)	st T7 J12 EIU (1)	st T7 J12 EIU (1)	st T7 J12 EIU (1)	/	/	/	/
	LOSS OF SYNC (>480ms)	/	/	/	/	/	/	/	/	/	/	/	/	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	/	/	/	/
	not GM COMMAND & RECEIVED TONE TN	/	st T5 J3 AP	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	sp T7 J1 D1
	ARL COMMAND	/	st T5 J2	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	END TONE TL (5ms)	/	/	J3	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
EVENTS PRIORITY	EC not BP1 or ARL	/	/	/	/	J41	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	CVC BP1 (UAR or UAR)	/	/	/	/	J41	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	DETCT SIGN not UAR	/	/	/	/	/	J42	J5	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	ENERGY UAR	/	/	/	/	/	J42	J5A	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	BASIC FRAME SYNC	/	/	/	/	/	/	/	J6	J6A	/	/	/	/	/	/	/	/	/	/	/	-	/	/	/
	SUPER FRAME SYNC (SW)	/	/	/	/	/	/	/	/	/	sp T5 J7 UAI	sp T5 J6A UAI	/	/	/	/	/	/	/	/	/	/	/	/	/
	DR COMMAND	/	/	/	/	/	/	/	/	/	/	/	/	J9	J9	J9	J9	J9	J9	J9	J9	/	/	/	/
	AR COMMAND	/	st T5 J2	/	/	/	/	/	/	/	/	/	/	/	J6AP	J6AP	/	/	J7	J7	/	/	/	/	/
	UAR COMMAND	/	st T5 J2	/	/	/	/	/	/	/	/	/	/	J6AP	J6AP	J6AP	/	/	/	/	/	/	/	/	/
	AI COMMAND	/	/	/	/	/	/	/	/	/	/	/	/	/	J8	/	/	/	/	/	/	/	/	/	/
	FAO COMMAND	/	/	/	/	/	/	/	/	/	/	/	/	/	/	J7	J78	/	/	/	/	/	/	/	/
LESS	Received act=1 not BP2	/	/	/	/	/	/	/	/	/	/	/	/	J8 AI	/	J8 AI	/	/	/	/	/	/	/	/	/
	Received act=1 BP2	/	/	/	/	/	/	/	/	/	/	/	/	J78 AI	/	J8 AI	/	/	/	/	/	/	/	/	/
	Received act=0 not RR or ARL	/	/	/	/	/	/	/	/	/	/	/	/	/	J7 EI	/	J7 EI	/	/	/	/	/	/	/	/
	Received act=0 RR & not ARL	/	/	/	/	/	/	/	/	/	/	/	/	/	J7 EI	/	J78R EI	/	/	/	/	/	/	/	/
	Received sai = 1	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	J8P AP	/	/	/	/	/
	Received sai = 0 and act = 0	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	J8A UAI	/	/	/	/	/	/	/
	NO ANSWER TO TONE	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	VANISHING OF RECEIVED SIGNAL (<40ms)	/	/	/	/	J4	/	/	J41	/	/	/	/	/	/	/	/	/	/	/	/	J1 D1	/	st T7 J12	/
→	END 4 SUPER FRAMES	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	J11	/	/	/
	EXPIRY OF TIMER 7 (40ms)	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	J3 D1

(1) IN AUTO MODE, THE EIU INDICATION BECOMES RES (EIU & RES HAVE THE SAME CODE)
(2) IN J7/J78 STATES, IF ARL COMMAND THEN act BIT IS AUTOMATICALLY SET TO "1". ELSE act BIT = "0"
(3) uoa BIT = "1" WHEN THE ACTIVATION PROCEDURE HAS BEEN INITIATED BY TE SIDE OR LT SIDE BY AR COMMAND; ELSE uoa BIT = "0"
(*): NO CHANGE

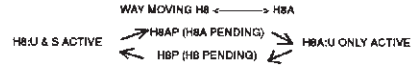
ACTIVATION/DEACTIVATION FINITE STATE MATRIX IN LT MODE

				START UP STATES									ACTIVATION STATES							END STATES		
													U & S				U ONLY			ERROR STATES		
	EVENTS	STATE NAME	POWER OFF	FULL RESET	ALTING	EC TRming	WAIT SL	CHECK SL	EC CVGED	SW SYNC	ISW SYN Chk: uoa	Pdng ACTIV$_{en}$	ISW SYNC	Pdng ACTIVE	U & ST ACTIVE	TE INACTIV	Pdng DACT$_{RT}$	U only ACTIVE	Pdng ACTIV$_{ERT}$	Pdng DEACT.	RECEIV RESET	TEAR DOWN
		STATE CODE	H0	H1	H2	H3	H31	H32	H4	H5	H5A	H5B	H6	H7	H8	H11	H8AP	H8A	H8P	H9	H12	H10
		U LINE TX	SN0	SN0	TN	SN1	SN0	SN0	SN0	SN2	SN2	SN2	SN3 act = 0 sai = *	SN3 act = 1 sai = 1	SN3 act = 1 sai = 1	SN3 act = 0 sai = 0	SN3 act = * sai = *	SN3 act = 0 sai = 0	SN3 act = 0 sai = 1	SN3 act = * sai = *	SN0	SN0
↑ MOST	POWER ON # GCI only		H1 DIII	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	LOSS OF POWER		/	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0
	RES COMMAND		/	H1	ap T4 H10 EIU (1)	ap T4 H10 EIU (1)	ap T4 H10 EIU (1)	ap T4 H10 EIU (1)	ap T4 H10 EIU (1)	ap T4 H10 EIU (1)	H10 EIU	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	/	/
	EXPIRY OF TIMER 4 (15 seconds)		/	/	/	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	/	/	/	/	/	/	/	/	/	/	/	/
	LOSS OF SIGNAL (>480ms)		/	/	/	/	ap T4 at T6 H12 EIU (1)	/	/	/	at T6 H12 EIU (1)	at T6 H12 EIU (1)	at T6 H12 EIU (1)	at T6 H12 EIU (1)	at T6 H12 EIU (1)	at T6 H12 EIU (1)	at T6 H12 EIU (1)	at T6 H12 EIU (1)	at T6 H12 EIU (1)	/	/	/
	LOSS OF SYNC (>480ms)		/	/	/	/	/	/	/	/	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	/	/
	not OM COMMAND & RECEIVED TONE TL (2)		/	at T4 H2(6) LSD	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	ap T6 H1 D1	/
	AR COMMAND & not RECEIVED TONE TL		/	at T4 H2	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	END TONE TN (3ms)		/	/	H3	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	EC CONVERGED		/	/	/	H31	/	/	/	/	/	/		/	/	/	/	/	/	/	/	/
	DETECT. SIGN. ENERGY		/	/	/	/	H32	H4	/	/	/	/		/	/	/	/	/	/	/	/	/
	BASIC FRAME SYNC		/	/	/	/	/	/	H5	/	/	/	/	/	/	/	/	/	/	/	/	/
	SUPER FRAME SYNC (ISW)		/	/	/	/	/	/	/	spT4 H5A	/	/	/	/	/	/	/	/	/	/	/	/
	RECEIVED dea = 0		/	/	/	/	/	/	/	/	H9 SAVE ST	H9 SAVE ST	H9 SAVE ST	H9 SAVE ST	H9 SAVE ST	H9 SAVE ST	H9 SAVE ST	H9 SAVE ST	H9 SAVE ST	/	/	/
	RECEIVED dea = 1		/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	RETURN SAVd ST	/	/
	When not RR	RECEIVED uoa = 0	/	/	/	/	/	/	/	/	H8A	/	H8AP DP (4)	H8AP DP (4)	H8AP DP (4)	/	/	/	/	/	/	/
		RECEIVED uoa = 1	/	/	/	/	/	/	/	/	H8 AP (3)	/	/	/	/	/	/	H8 AP (4)	H8 AP (4)	/	/	/
	When RR	RECEIVED uoa = 0	/	/	/	/	/	/	/	/	H5B UAP (3)	/	H8AP UAP (4)	H8AP UAP (4)	H8AP UAP (4)	/	/	/	/	/	/	/
		RECEIVED uoa = 1	/	/	/	/	/	/	/	/	H5B AP (3)	/	/	/	/	/	/	H8 AP (4)	H8 AP (4)	/	/	/
		UAI COMMAND & RECEIVED uoa = 0	/	/	/	/	/	/	/	/	/	H8A	/	/	/	/	H8A	/	/	/	/	/
		UAI COMMAND & RECEIVED uoa = 1	/	/	/	/	/	/	/	/	/	H6	/	/	/	/	H8A	/	/	/	/	/
	DI COMMAND		/	/	/	/	/	/	/	/	/	/	/	/	/	/	H8A	/	/	/	/	/
	AR COMMAND		/	/	/	/	/	/	/	/	/	/	/	/	/	/	H8A	H8P	/	/	/	/
	AI or AILCOMMAND		/	/	/	/	/	/	/	/	/	/	H7	/	/	H7 (6)	/	/	/	/	/	/
	EI COMMAND		/	/	/	/	/	/	/	/	/	/	/	H11 EI (5)	H11 EI (5)	/	/	/	/	/	/	/
	RECEIVED act=0		/	/	/	/	/	/	/	/	/	/	/	/	H7 EI (4)	H6 EI (4,5)	/	/	/	/	/	/
	RECEIVED act=1		/	/	/	/	/	/	/	/	/	/	/	H8 AI (4)	/	/	/	/	/	/	/	/
↓ LESS	ABSCENCE OF SIGNAL (<40ms)		/	/	/	/	/	H31	/	/	/	/	/	/	/	/	/	/	/	at T6 H12 DP	/	at T6 H12
	EXPIRY OF TIMER 6 (40ms)		/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	H1 D1	/

EVENTS PRIORITY

(1) IN AUTO-MODE, THE EIU PRIMITIVE BECOMES DP WHEN NOT RR MODE OR RES WHEN NOT RR MODE.
(2) WHEN ACTAUT = '0': THE JUMP H2 FROM H1 WAITS FOR AN AR COMMAND.
(3) IN AUTO-MODE, THESE PRIMITIVES INDICATION ARE REPLACED BY ARL WHEN A MESSAGE ANALOG LOOP BACK IS DETECTED.
(4) IN AUTO-MODE, THESE PRIMITIVES INDICATION ARE REMOVED WHEN ARL INDICATION IS ALREADY SET.
(5) IN NON AUTO-MODE, EI PRIMITIVE INDICATION IS SENT FROM H7/H8 TO H11 AND REMOVED FROM H11 TO H6 WHEN EI-FILTER IS SET. THE JUMP FROM H11 TO H7 WITH AI OR AIL COMMAND IS POSSIBLE ONLY WHEN EI-FILTER IS SET.
(6) IF ACTAUT = '0': AR REQUIRED TO JUMP TO H2.

* : no change



ACTIVATION/DEACTIVATION FINITE MACHINE IN NT MODE

APPENDIX B - ELECTRICAL PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.3 to 7.0	V
V_{IN}	Input Voltage	– 0.3 to 7.0	V
T_A	Operating Temperature Range	-40 to 85 (3)	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

TRANSMISSION ELECTRICAL PARAMETERS

Parameter	Min.	Typ.	Max.	Unit
LINE INTERFACE FEATURES				
Power up Output Differential Impedance (0–20KHz) between LO+/LO-		1	5	Ω
Power Down Output Differential Impedance (0–20KHz) between LO+/LO-	8	12	16	Ω
POWER CONSUMPTION				
I_{CC} in Power Down		4	8	mA
I_{CC} in Power Up Transmitting (2)		70	80	mA
TRANSMISSION PERFORMANCES				
Transmit Pulse Amplitude on LO+, LO- (1)	3.27		3.61	V
Transmit Pulse Linearity (1:3 ratio accuracy)	36	50		dB

(1) This specification garanties the ANSI specification, concerning the pulse amplitude using the line interface recommended schematics, of 2,5 ± 5% Volts peak amplitude for 2B1Q pulse.
(2) Test condition: V_{CC} = 5V, 2B1Q random signal transmitted with recommended 27mH line interface (fig 12) terminated with 135Ω.
(3) Test condition: ETSI Loop2 (average loop) and ETSI Loop 3R (long loop)

STATIC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	DC Supply Voltage		4.75		5.25	V
V_{IL}	Input Low Voltage	All Dig Inputs except XTAL1			0.7	V
V_{IH}	Input High Voltage	All Dig Inputs except XTAL1	2.2			V
V_{ILX}	Input Low Voltage	XTAL1 Input			0.5	V
V_{IHX}	Input High Voltage	XTAL1 Input	V_{CC}–0.5			V
V_{OL}	Output Low Voltage	Br, I_O = +7mA All other Digital Outputs, I_{ol} = +1mA			0.4 0.4	V V
V_{OH}	Output High Voltage	Br, I_O = –7mA All other Digital Outputs I_O = –1mA All Outputs (3), I_O = –100µA	2.4 2.4 V_{CC}–0.5			V V V
I_{LH}	Input Current	Any Digital V_{in} = V_{DD}	0		1	µA
I_{LL}	Input Current	Input pin numbers: 6,7,12,13 17,19,25,27,28 Vin = GND (1)	–1		0	µA
I_{LLR}	Input Current with Internal Pull Up Resistor	Input pin numbers: 14,15,16, 22,26,18, V_{in} = GND (1)	–50		0	µA
I_{LLX}	Input Current on XTAL1	GND < V_{in} < V_{CC}	–200		200	µA
I_{LLI}	Input Current on LI+/LI-	LI+ and LI- to GND	-100		100	µA
IOZ	Output Current in High Impedance State (TRISTATE)	GND < Vout < V_{CC} ; All Digital Outputs except XTAL2	–10		10	µA

(1) The pin number refer to DIP package.

TIMING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
MASTER CLOCK						
FMCLK	Frequency of MCLK Tolerance	Including Temperature, Aging, Etc...	 –100	15.36	 +100	MHz ppm
	MCLK/XTAL Input Clock Jitter	External Clock Source			50	ns pk-pk
tWMH	Clock Pulse Width, MCLK High Level	$V_{IH} = V_{CC} – 0.5V$ $V_{IL} = 0.5V$	20			ns
tWML	Clock Pulse Width, MCLK Low Level		20			ns
tRM tFM	Rise Time of MCLK Fall Time of MCLK	Used as a Logic Input			10 10	ns ns
DIGITAL INTERFACE						
FBCLK	Frequency of BCLK	Formats 1, 2 and 3 Format 4 and GCI Mode	256 512		4095 6144	KHz KHz
tWBH	Clock Pulse Width, BCLK High Level	Measured from V_{IH} to V_{IH}	30			ns
tWBL	Clock Pulse Width, BCLK Low Level	Measured from V_{IL} to V_{IL}	30			ns
tRB	Risae Time of BCLK	Measured from V_{IL} to V_{IH}			15	ns
tFB	Fall Time of BCLK	Measured from V_{IH} to V_{IL}			15	ns
tSFB	Setup Time, FS High or Low to BCLK Low	DSI or GCI Slave Mode only	30			ns
tHBF	Hold Time, BCLK Low to FS High or Low	DSI or GCI Slave Mode only	20			ns
tDBF	Delay Time, BCLK High to FS High or Low	DSI or GCI Master Mode only	–20		20	ns
tDBD	Delay Time, BCLK High to Data Valid	Load = 150pF + 2 LSTTL Loads			80	ns
tDBDZ	Delay Time, BCLK High to Data HZ				50	ns
tDFD	Delay Time, FS High to Data Valid	Load = 150pF + 2 LSTTL Loads			80	ns
tSDB	Setup Time, Data Valid to BCLK Low		0			ns
tHBD	Hold time, BCLK to Data Invalid		20			ns
tDBT	Delay Time, BCLK High to TSR Low	Load = 100pF + 2 LSTTL Loads			80	ns
tDBTZ	Delay Time, BCLK Low to TSR HZ				50	ns
tDFT	Delay Tie, FS High to TSR Low	Load = 100pF + 2 LSTTL Loads			80	ns
D PORT IN CONTINUOUS MODE: 16KBITS/SEC						
tSDD	Setup Time, DCLK Low to DX High or Low		50			ns
tHDD	Hold Time, DCLK Low to DX High or Low		50			ns
tDDD	Delay Time, DCLK High to DR High or Low	Load = 50pF + 2 LSTTL Loads			80	ns
MICROWIRE CONTROL INTERFACE						
FCCLK	Frequency of CCLK				5	MHz
tWCH	Clock Pulse Width, CCLK High Level	Measured from V_{IH} to V_{IH}	85			ns
tWCL	Clock Pulse Width, CCLK Low Level	Measured from V_{IL} to V_{IL}	85			ns
tRC	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			15	ns
tFC	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			15	ns
tSSC	Setup Time, CSB Low to CCLK High		60			ns
tHCS	Hold Time, CCLK Low to CSB High		10			ns
tWSH	Duration of CSB High		200			ns
tSIC	Setup Time, CI Valid to CCLK High		25			ns
tHCI	Hold Time, CCLK High to CI Invalid		25			ns
tDSO	Delay Time, CSB Low to CO Valid	Out First Bit on CO			50	ns
tDCO	Delay Time CCLK Low to CO Valid	Load = 50 pF + 2LSTTL Loads			50	ns
tDCOZ	Delay Time, CCLK Low to CO HZ				50	ns
tDCI	Delay Time, CCLK Low to INTB Low or HZ	Load = 80pF + 2LSTTL Loads			150	ns

Figure 14: BCLK, FSA, FSB, SLAVE MODE, DELAYED MODE, FORMATS 1 2 3 (µW ONLY).

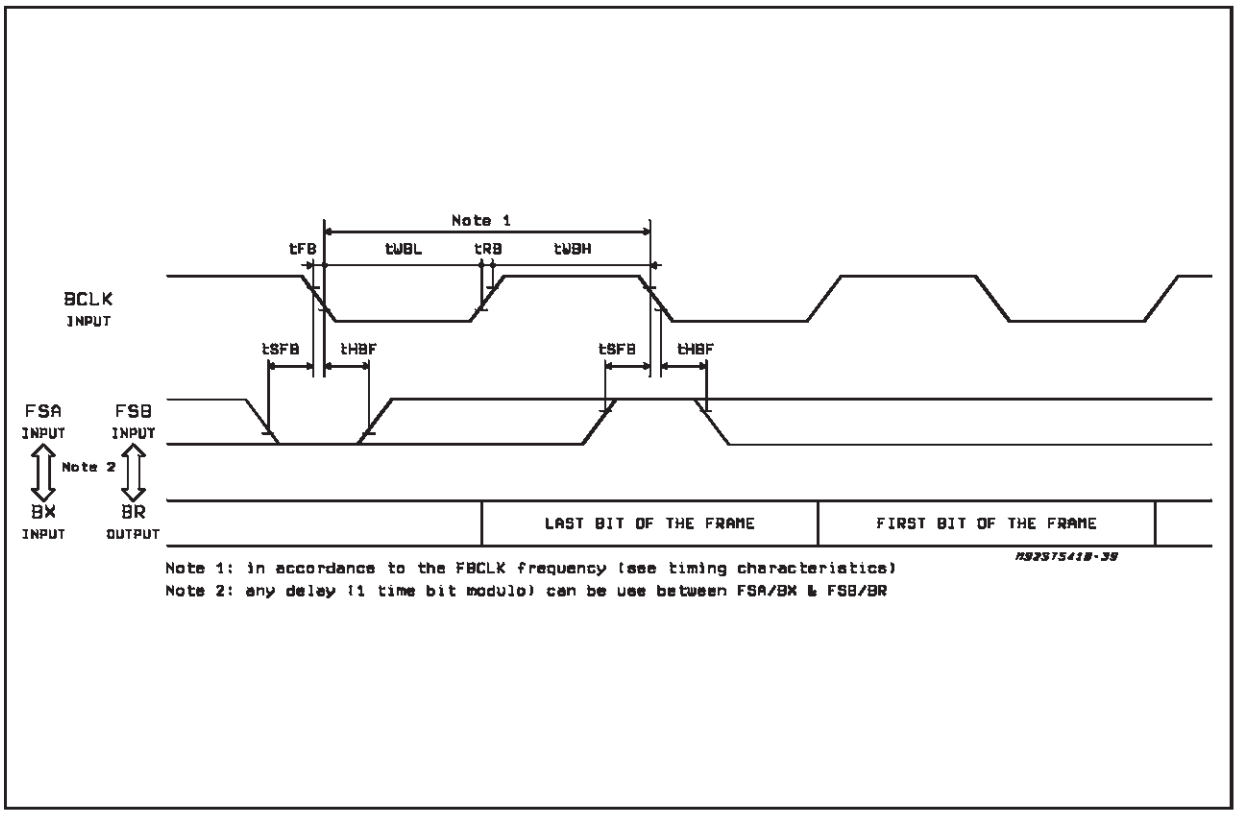


Figure 15: BCLK, FSA, FSB, SLAVE MODE, NON DELAYED MODE, FORMATS 1 2 3 (µW ONLY).

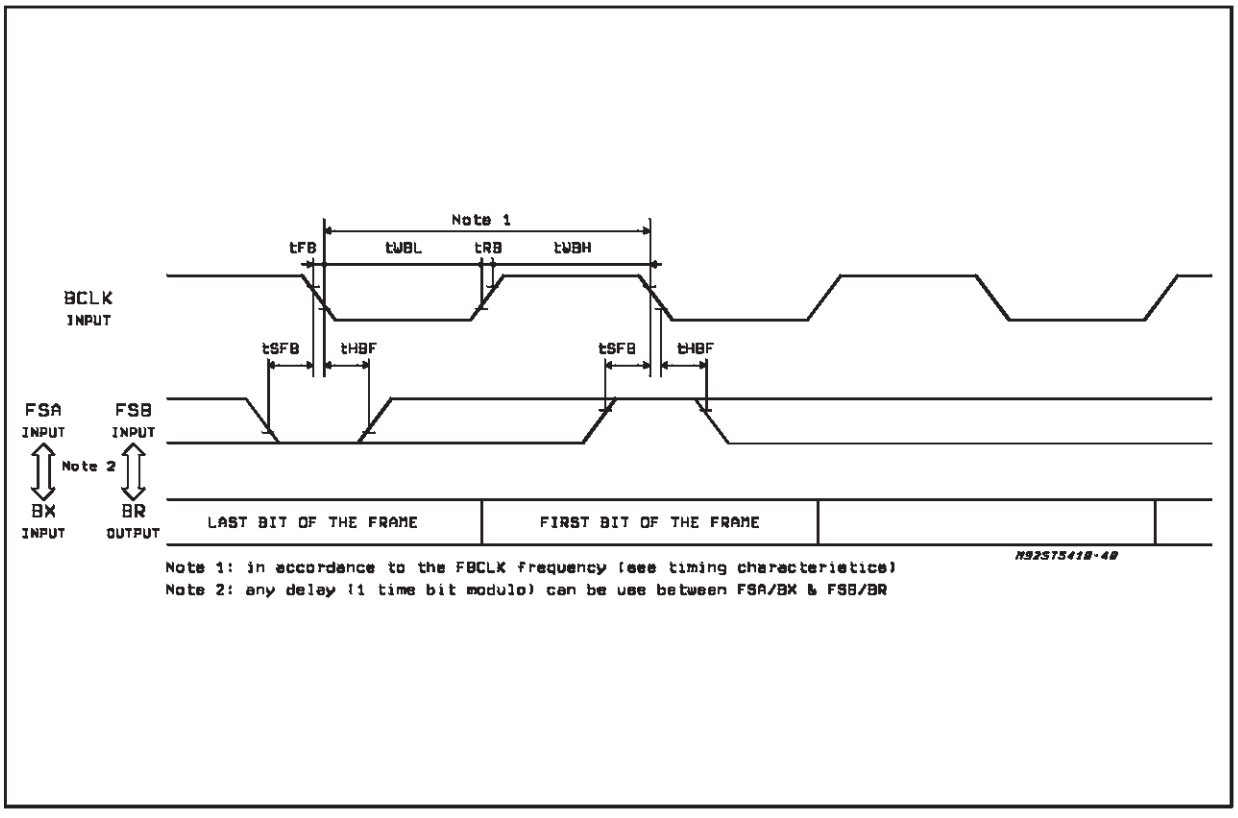


Figure 16: BCLK, FSA, FSB, SLAVE MODE, FORMAT 4 ALWAYS NON DELAYED MODE, (µW AND GCI MODE).

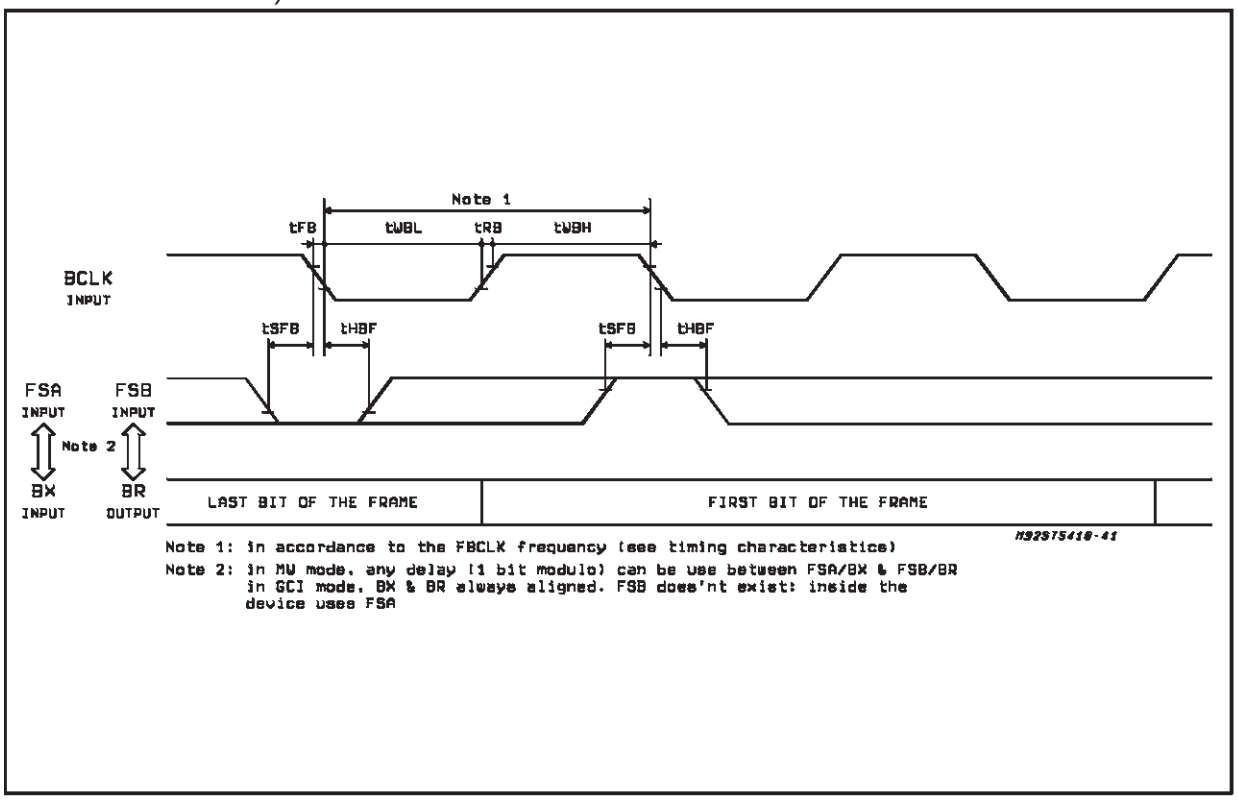


Figure 17: BCLK, FSA, FSB, MASTER MODE, DELAYED MODE, FORMATS 1 2 3 (µW ONLY).

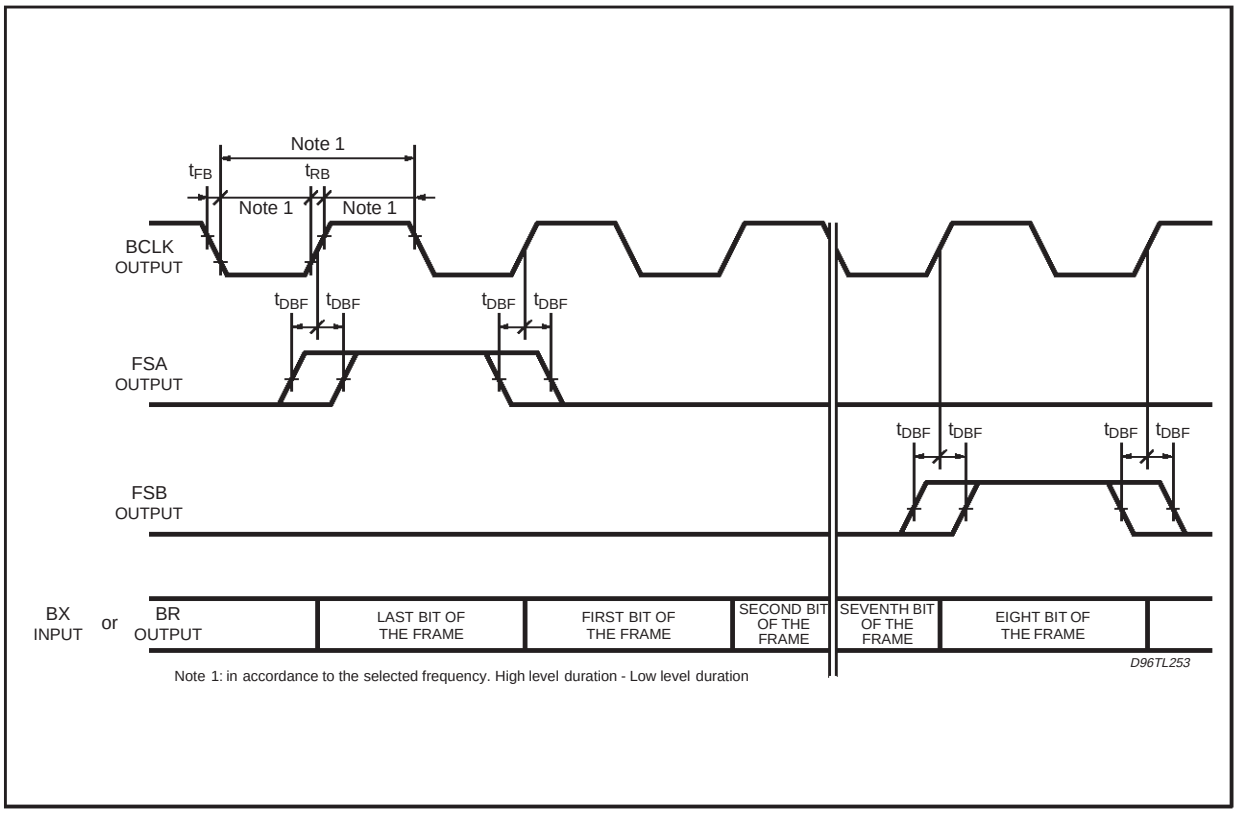


Figure 18: BCLK, FSA, FSB, MASTER MODE, NON DELAYED MODE, FORMATS 1 3 (µW ONLY).

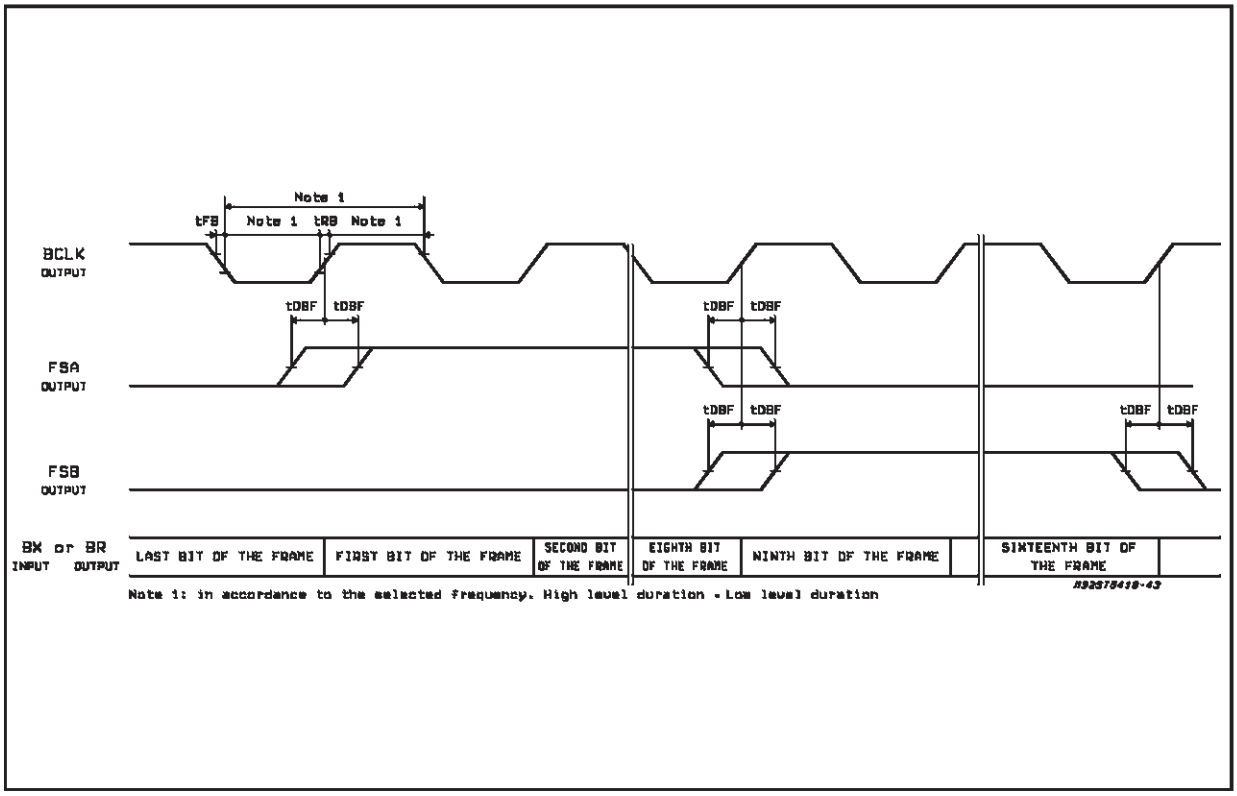


Figure 19: BCLK, FSA, FSB, MASTER MODE, FORMAT 4 ALWAYS NON DELAYED MODE, (µW AND GCI MODE).

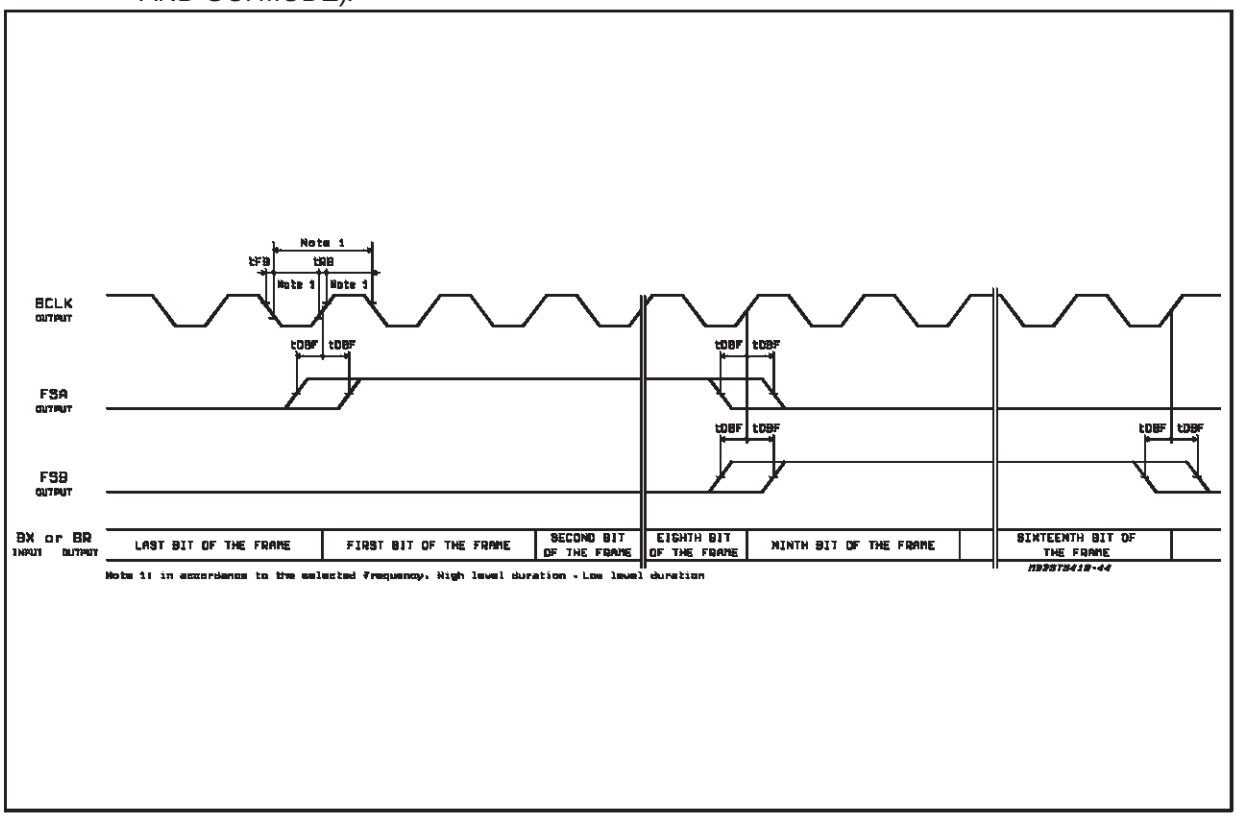


Figure 20: BX, DX, BR, DR, SLAVE & MASTER, DELAYED & NON DELAYED, FORMATS 1 2 3 (µW ONLY)

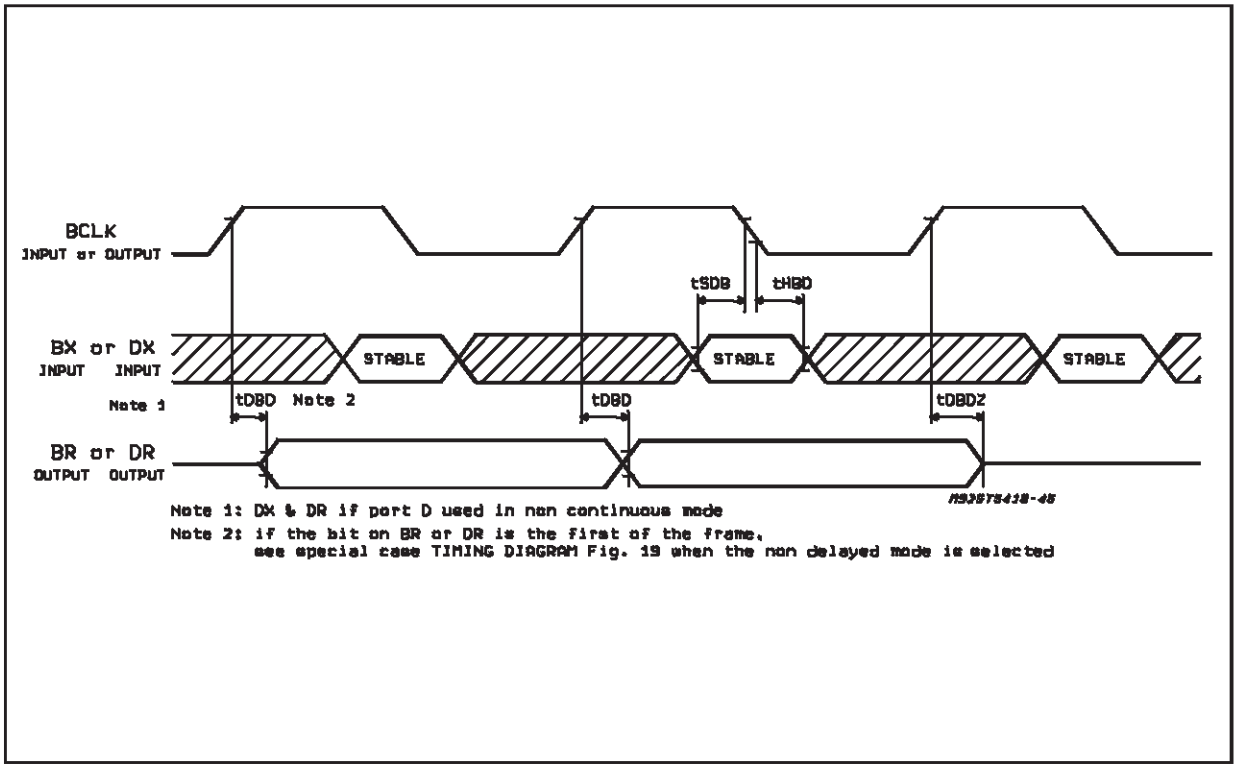


Figure 21: BX, DX, BR, DR, SLAVE & MASTER, FORMAT 4 ALWAYS NON DELAYED, (µW & GCI MODE)

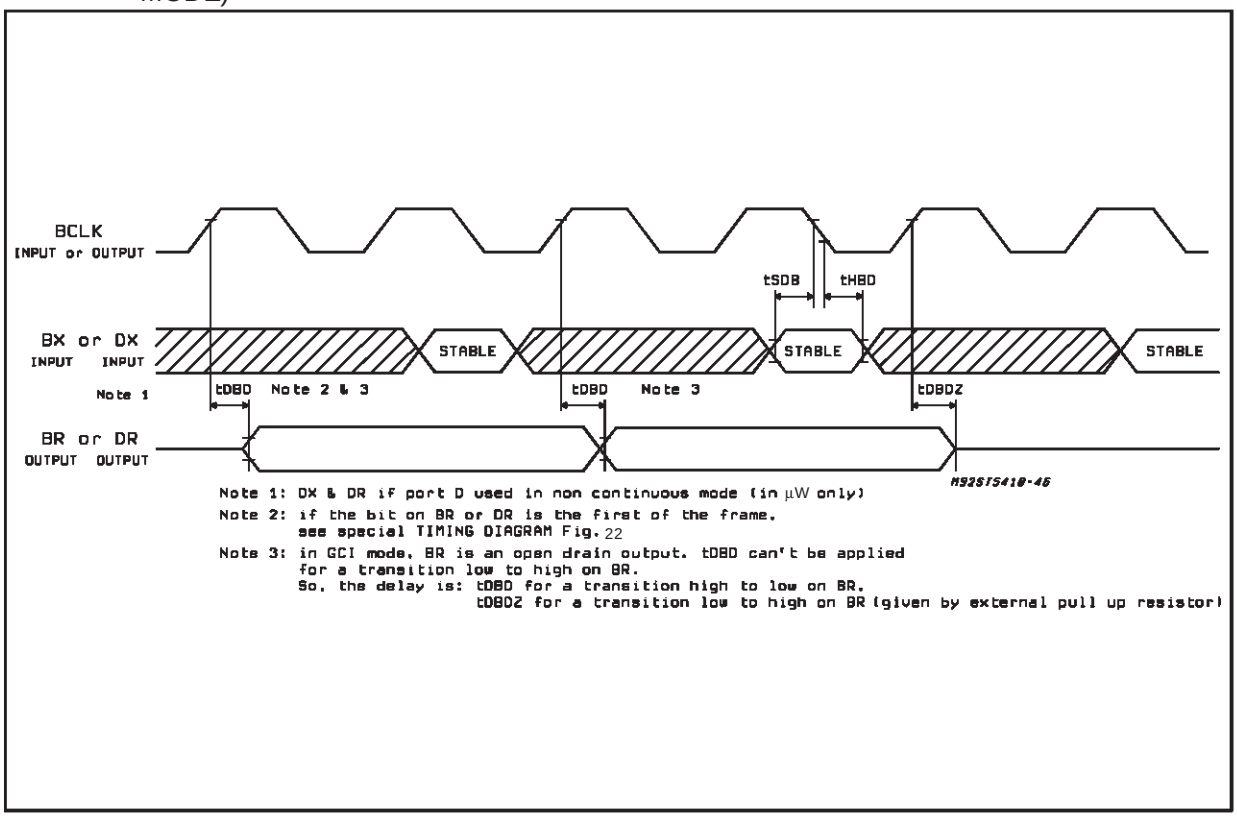


Figure 22: SPECIAL CASE BR, DR, ONLY FIRST BIT OF THE FRAME, IN SLAVE AND NON DELAYED MODES FORMATS 1 3 (MW MODE), FORMAT 4 (µW & GCI MODE)

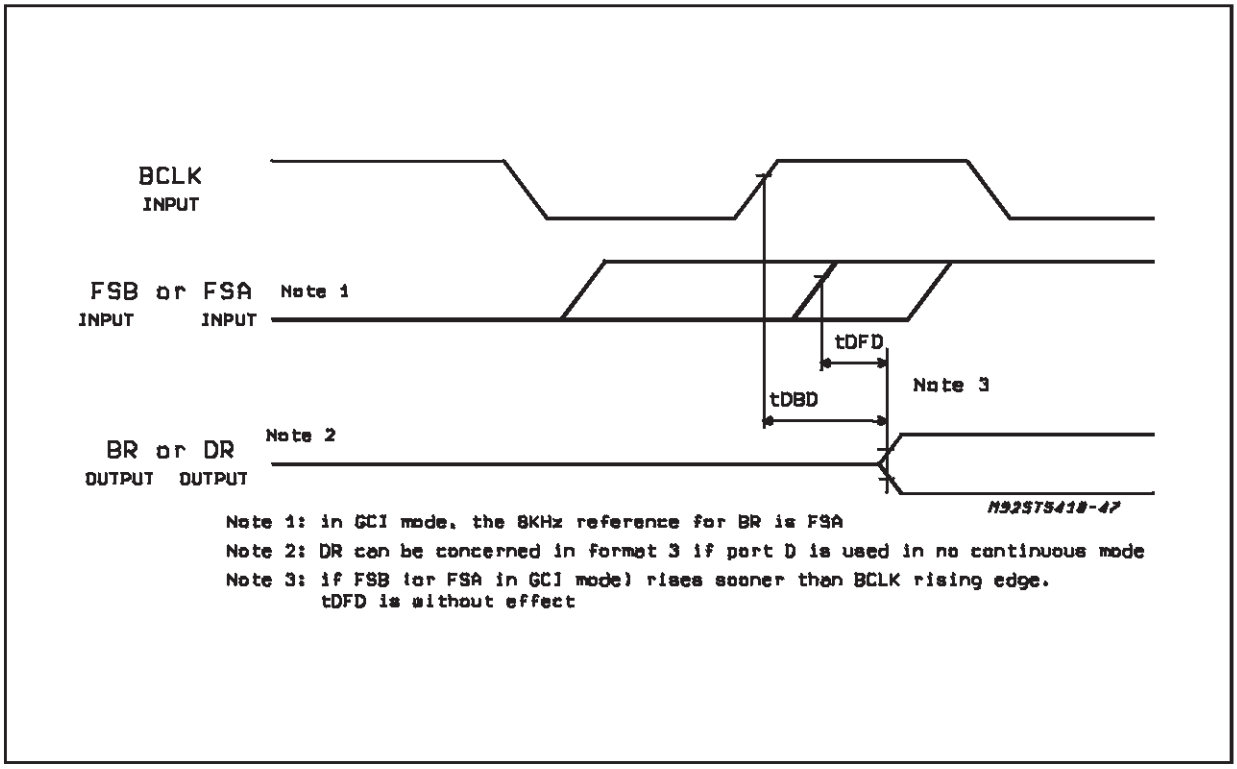


Figure 23: TSRB, SLAVE & MASTER, DELAYED & NON DELAYED, FORMATS 1 2 3 (µW ONLY)

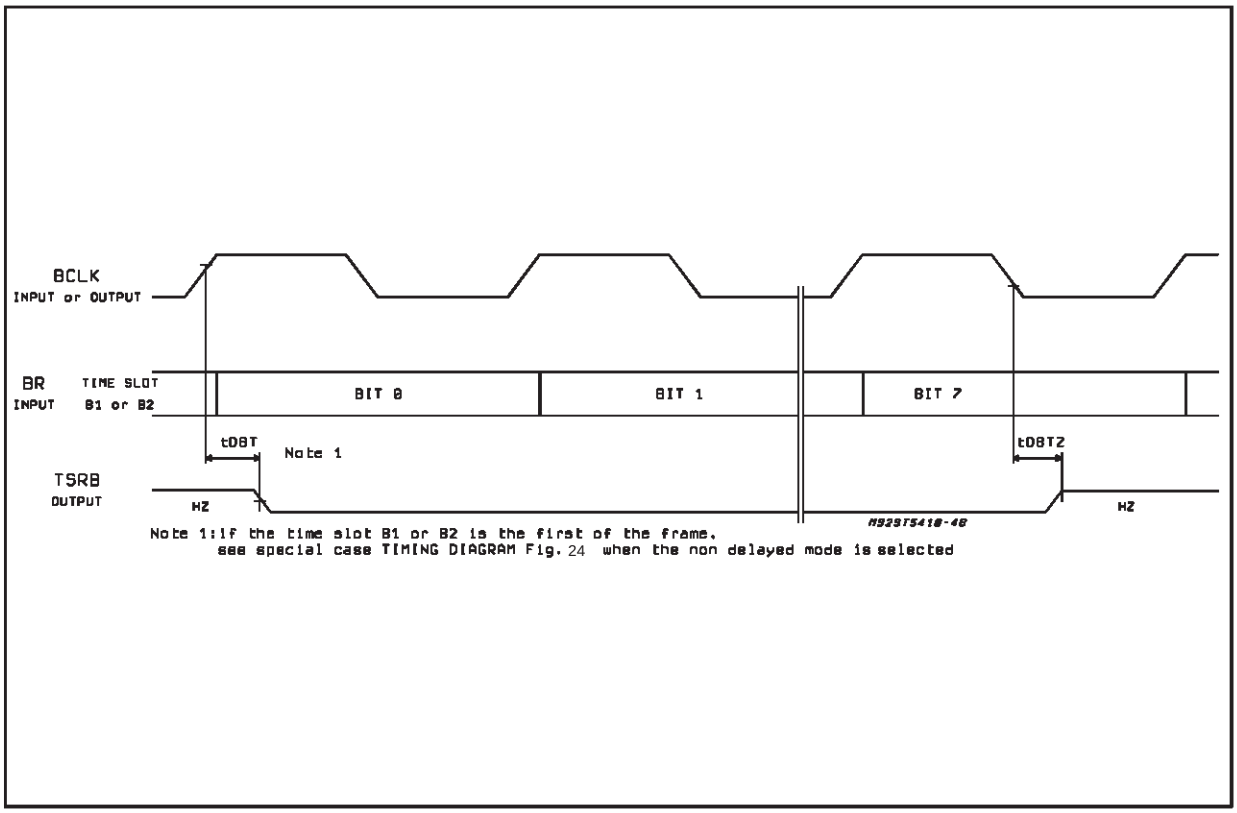


Figure 24: TSRB, SLAVE & MASTER, FORMAT 4 ALWAYS NON DELAYED MODE (µW & GCI)

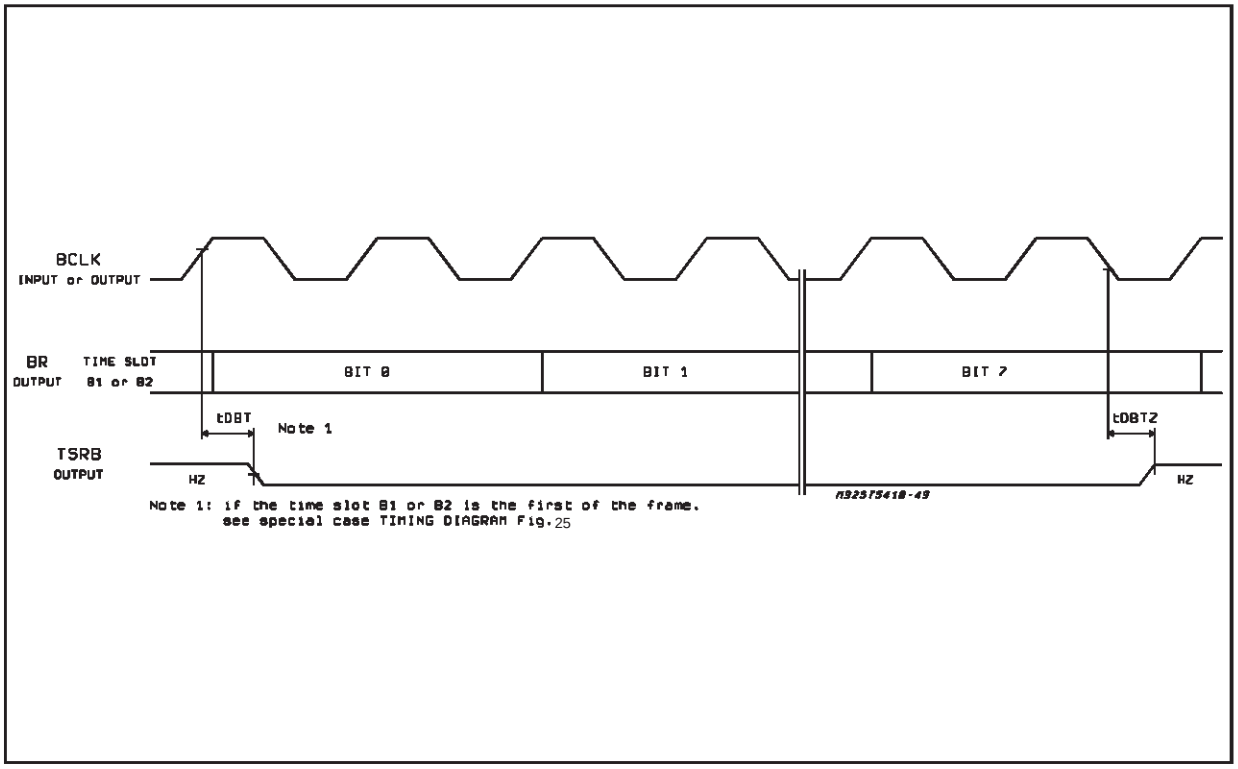


Figure 25: SPECIAL CASE TSRB, B1 OR B2 FIRST CHANNEL OF THE FRAME, IN SLAVE & NON DELAYED MODE, FORMATS 1 3 (MW MODE), FORMAT 4 (µW & GCI MODE)

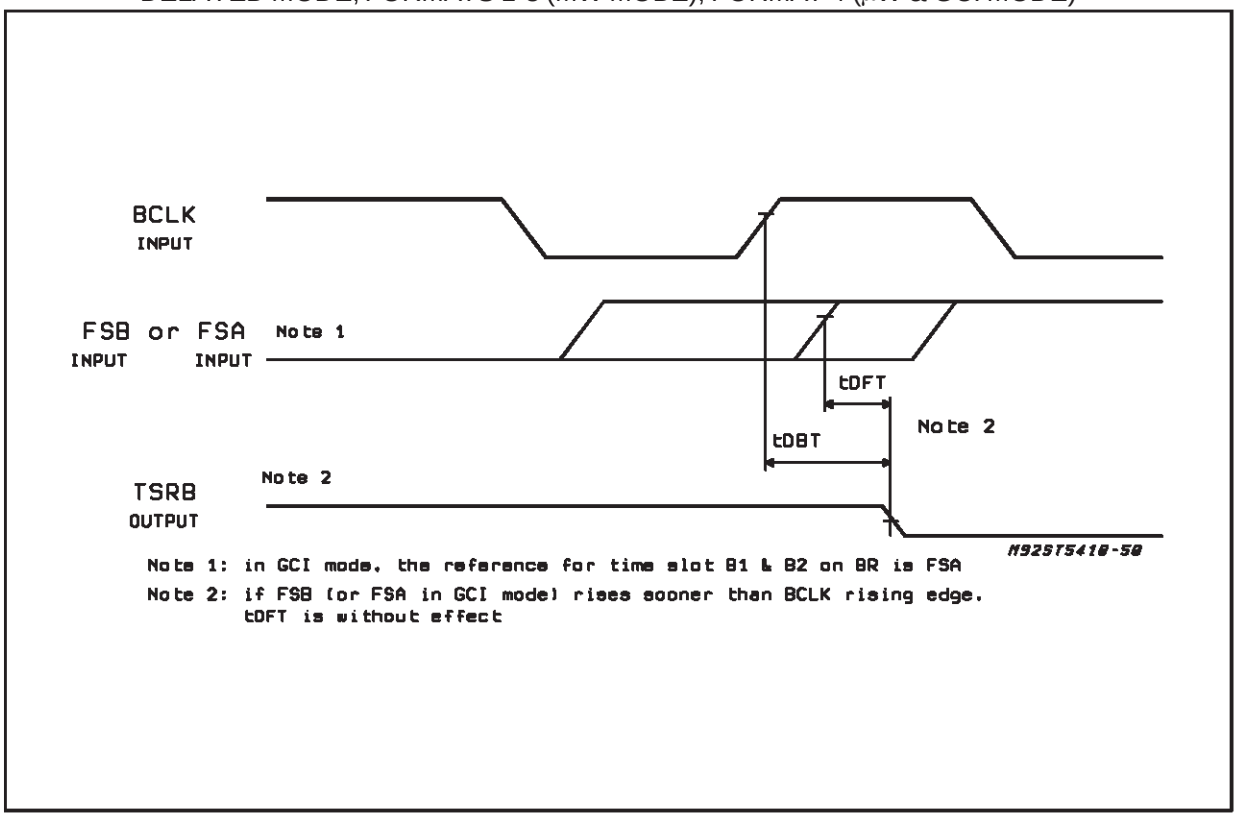


Figure 26: DCLK, DX, DR IN CONTINUOUS MODE SLAVE & MASTER, DELAYED & NON DELAYED MODES ALL FORMATS IN µW MODE ONLY

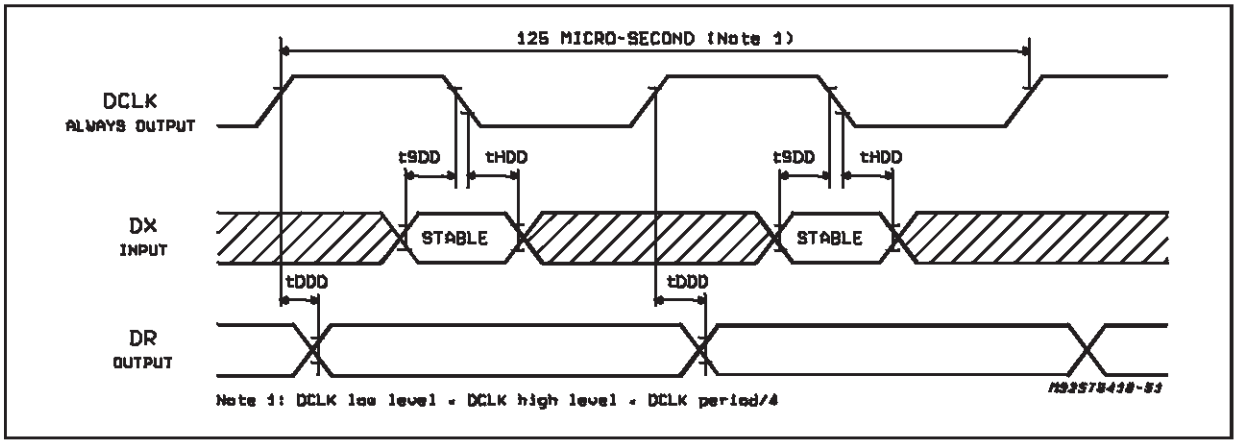


Figure 27: MCLK ALL MODES

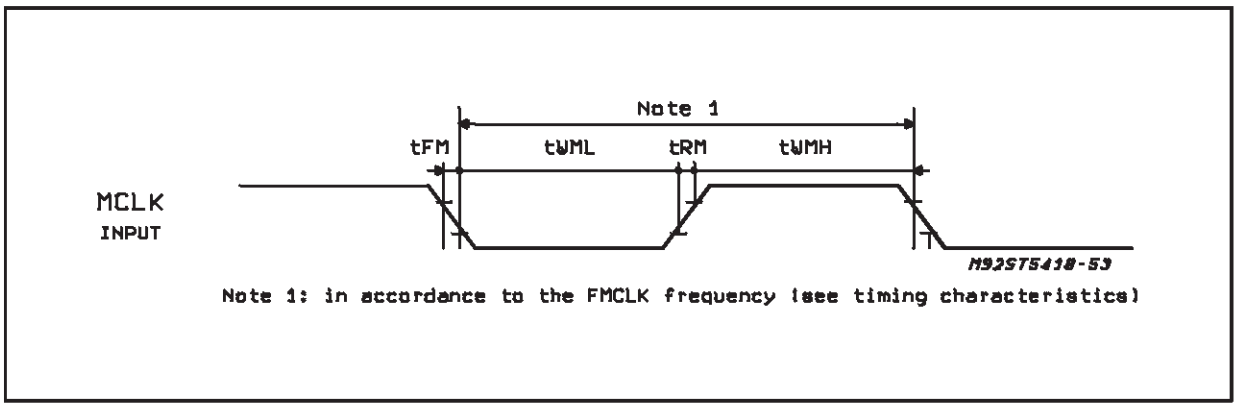


Figure 28: µW PORT Mode A

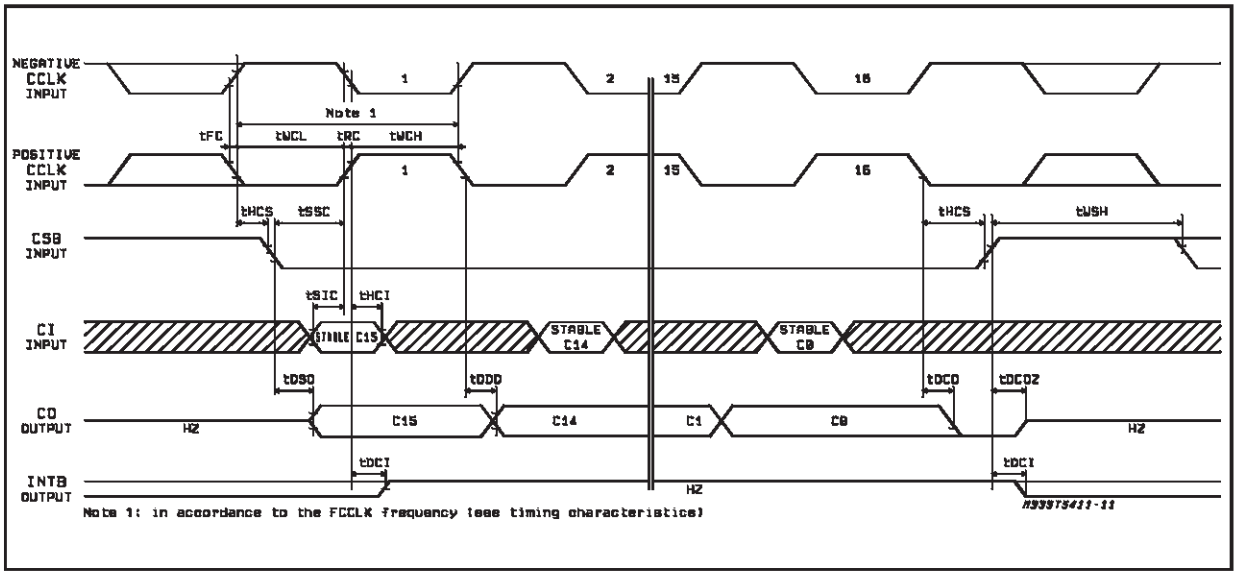
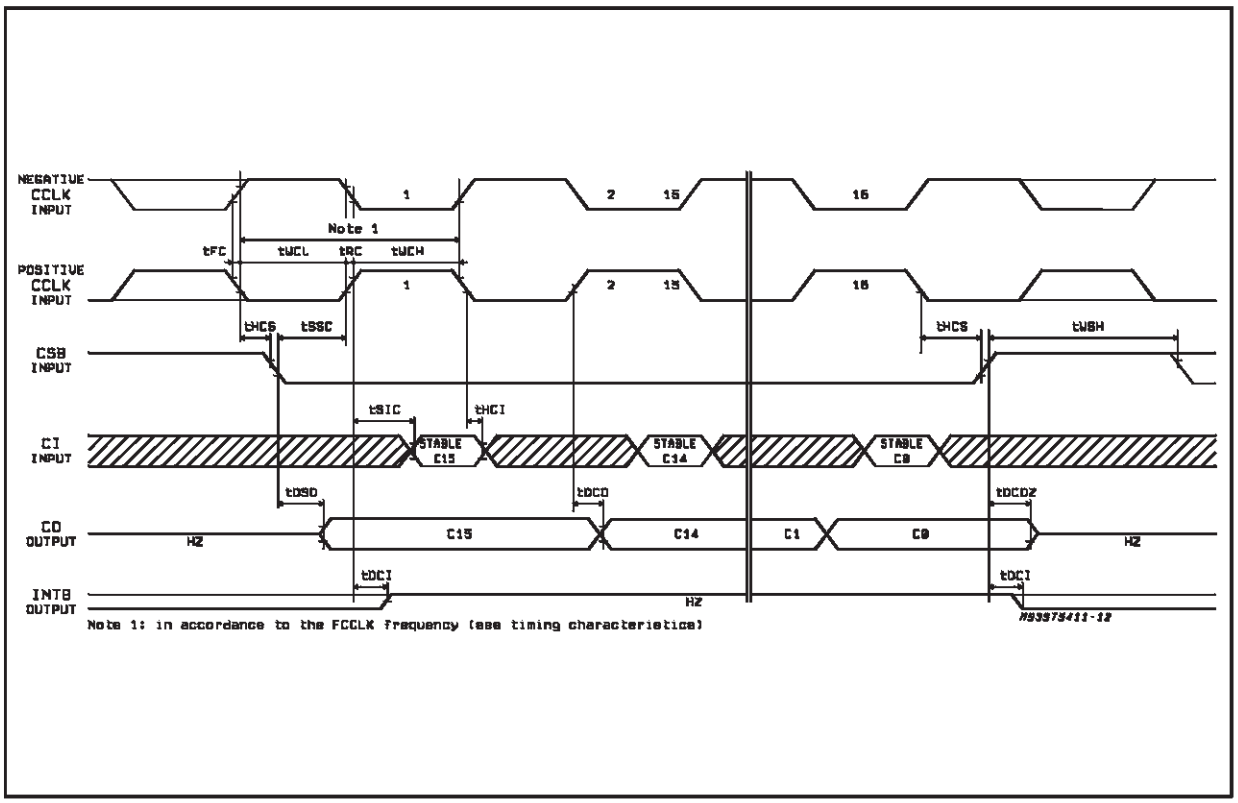
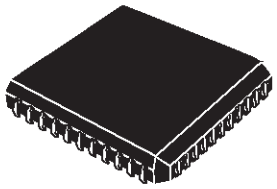


Figure 29: µW PORT Mode B

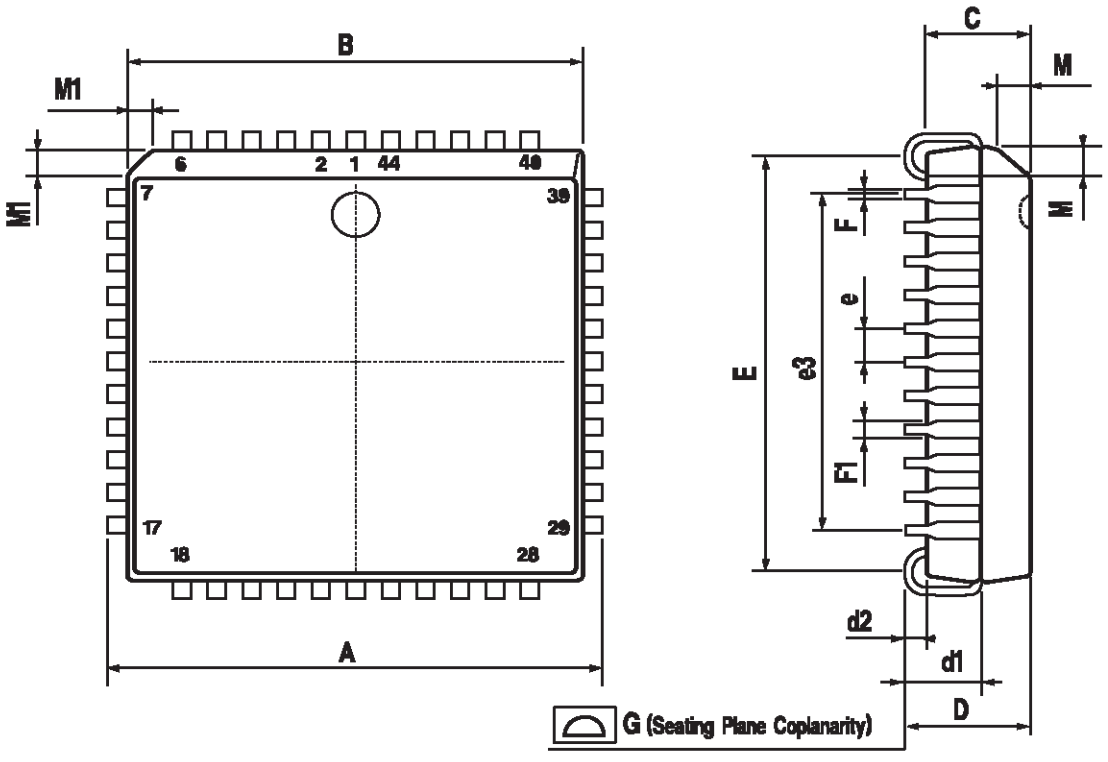


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	

OUTLINE AND MECHANICAL DATA

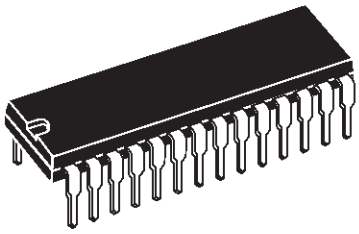


PLCC44

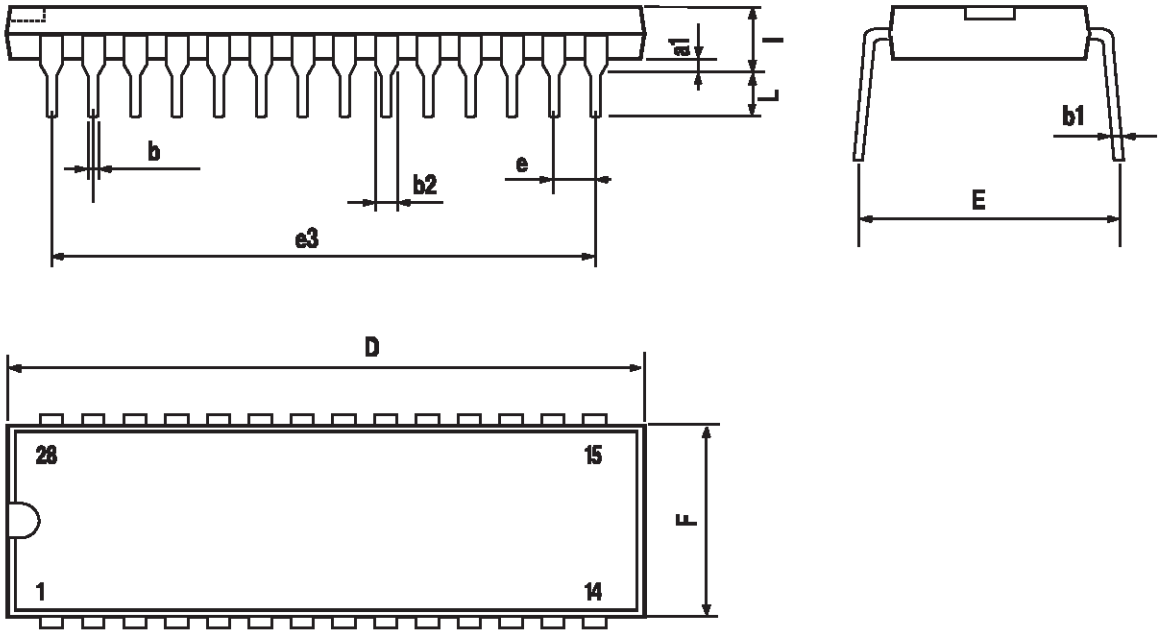


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.34			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

OUTLINE AND MECHANICAL DATA



DIP28



ESD - The SGS-THOMSON Internal Quality Standards set a target of 2 KV that each pin of the device should withstand in a series of tests based on the Human Body Model (MIL-STD 883 Method 3015): with C = 100pF; R = 1500Ω and performing 3 pulses for each pin versus V_{CC} and GND.

Device characterization showed that, in front of the SGS-THOMSON Internaly Quality Standards, all pins of STLC5412 withstand at least 2000V.

The above points are not expected to represent a pratical limit for the correct device utilization nor for its reliability in the field. Nonetheless they must be mentionned in connection with the applicability of the different SURE 6 requirements to STLC5412.