



## 256 Kbit (32Kb x 8) Low Voltage UV EPROM and OTP EPROM

- **LOW VOLTAGE READ OPERATION:**  
3V to 3.6V
- **FAST ACCESS TIME:** 90ns
- **LOW POWER CONSUMPTION:**
  - Active Current 10mA at 5MHz
  - Standby Current 10µA
- **PROGRAMMING VOLTAGE:** 12.75V ± 0.25V
- **PROGRAMMING TIME:** 100µs/byte (typical)
- **ELECTRONIC SIGNATURE**
  - Manufacturer Code: 20h
  - Device Code: 8Dh

### DESCRIPTION

The M27V256 is a low voltage 256 Kbit EPROM offered in the two ranges UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for microprocessor systems and is organized as 32,768 by 8 bits.

The M27V256 operates in the read mode with a supply voltage as low as 3V. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

The FDIP28W (window ceramic frit-seal package) has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

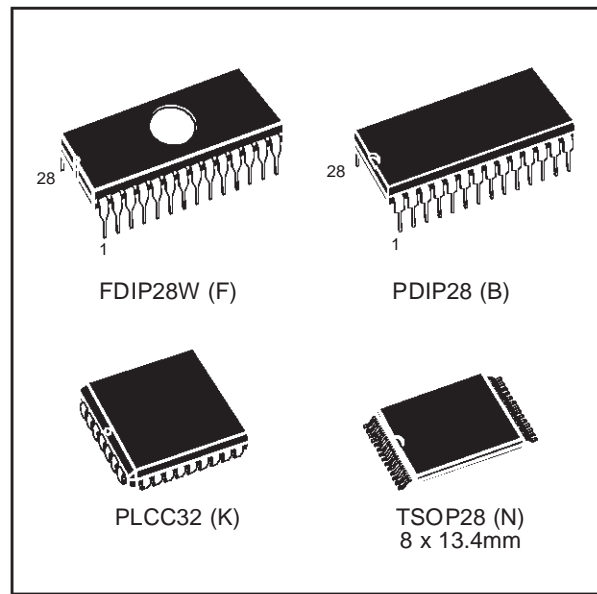


Figure 1. Logic Diagram

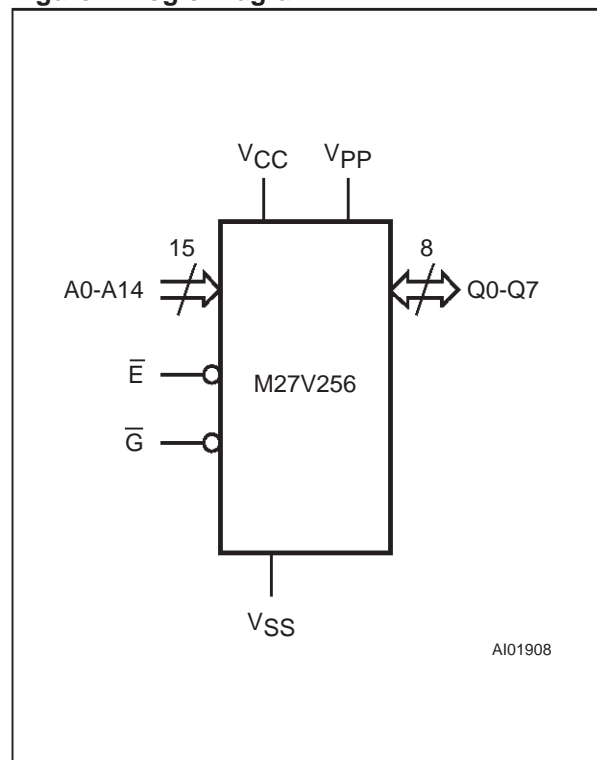


Table 1. Signal Names

A0-A14	Address Inputs
Q0-Q7	Data Outputs
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
V <sub>PP</sub>	Program Supply
V <sub>CC</sub>	Supply Voltage
V <sub>SS</sub>	Ground

## M27V256

Figure 2A. DIP Pin Connections

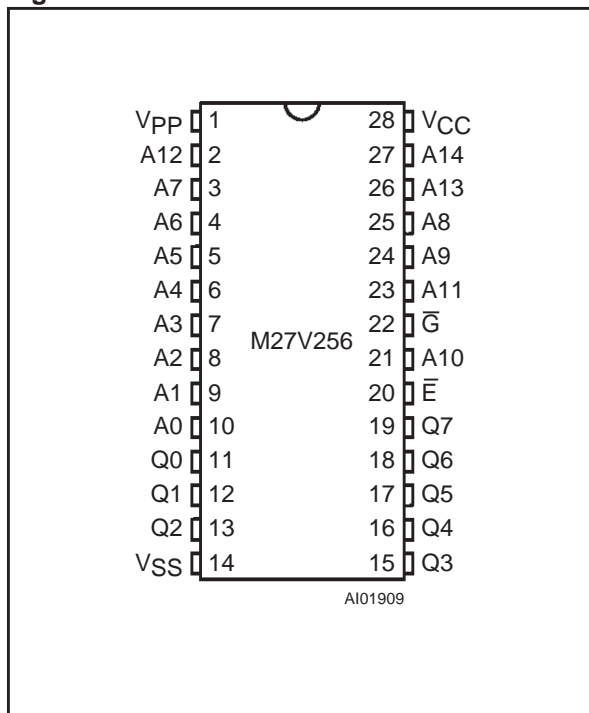
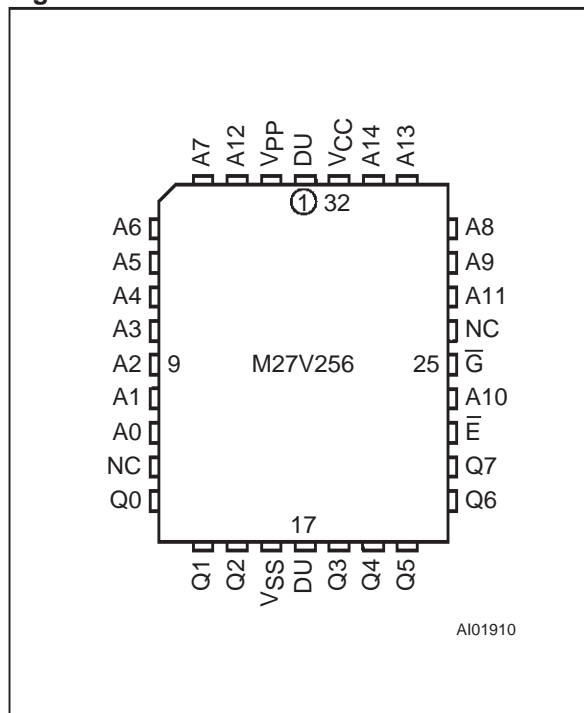
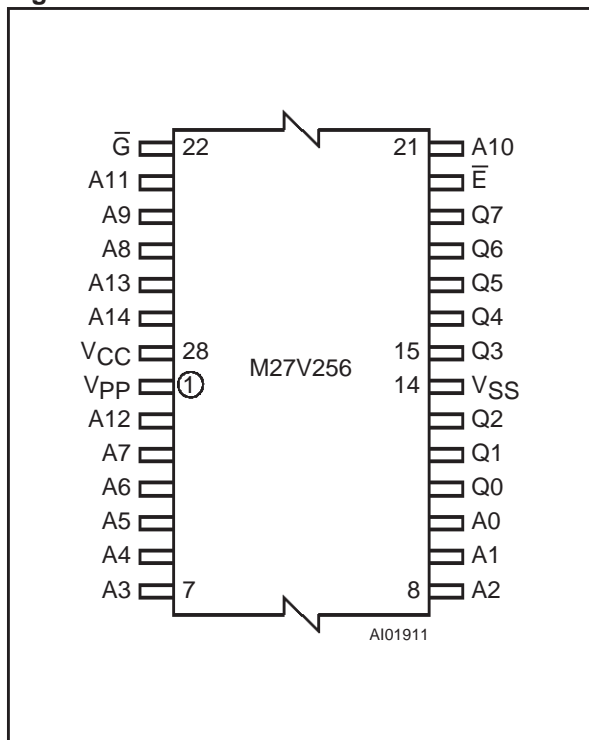


Figure 2B. LCC Pin Connections



**Warning:** NC = Not Connected, DU = Don't Use.

Figure 2C. TSOP Pin Connections



For applications where the content is programmed only one time and erasure is not required, the M27V256 is offered in PDIP28, PLCC32 and TSOP28 (8 x 13.4 mm) packages.

### DEVICE OPERATION

The modes of operation of the M27V256 are listed in the Operating Modes. A single power supply is required in the read mode. All inputs are TTL levels except for  $V_{PP}$  and 12V on A9 for Electronic Signature.

#### Read Mode

The M27V256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ( $\bar{E}$ ) is the power control and should be used for device selection. Output Enable ( $\bar{G}$ ) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time ( $t_{AVQV}$ ) is equal to the delay from  $\bar{E}$  to output ( $t_{ELQV}$ ). Data is available at the output after delay of  $t_{GLQV}$  from the falling edge of  $\bar{G}$ , assuming that  $\bar{E}$  has been low and the addresses have been stable for at least  $t_{AVQV} - t_{GLQV}$ .

**Table 2. Absolute Maximum Ratings (1)**

Symbol	Parameter	Value	Unit
T <sub>A</sub>	Ambient Operating Temperature (3)	-40 to 125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-50 to 125	°C
T <sub>STG</sub>	Storage Temperature	-65 to 150	°C
V <sub>IO</sub> (2)	Input or Output Voltage (except A9)	-2 to 7	V
V <sub>CC</sub>	Supply Voltage	-2 to 7	V
V <sub>A9</sub> (2)	A9 Voltage	-2 to 13.5	V
V <sub>PP</sub>	Program Supply Voltage	-2 to 14	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is -0.5V with possible undershoot to -2.0V for a period less than 20ns. Maximum DC voltage on Output is V<sub>CC</sub> +0.5V with possible overshoot to V<sub>CC</sub> +2V for a period less than 20ns.
3. Depends on range.

**Table 3. Operating Modes**

Mode	$\bar{E}$	$\bar{G}$	A9	V <sub>PP</sub>	Q0-Q7
Read	V <sub>IL</sub>	V <sub>IL</sub>	X	V <sub>CC</sub>	Data Out
Output Disable	V <sub>IL</sub>	V <sub>IH</sub>	X	V <sub>CC</sub>	Hi-Z
Program	V <sub>IL</sub> Pulse	V <sub>IH</sub>	X	V <sub>PP</sub>	Data In
Verify	V <sub>IH</sub>	V <sub>IL</sub>	X	V <sub>PP</sub>	Data Out
Program Inhibit	V <sub>IH</sub>	V <sub>IH</sub>	X	V <sub>PP</sub>	Hi-Z
Standby	V <sub>IH</sub>	X	X	V <sub>CC</sub>	Hi-Z
Electronic Signature	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>ID</sub>	V <sub>CC</sub>	Codes

Note: X = V<sub>IH</sub> or V<sub>IL</sub>, V<sub>ID</sub> = 12V ± 0.5V.

**Table 4. Electronic Signature**

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V <sub>IL</sub>	0	0	1	0	0	0	0	0	20h
Device Code	V <sub>IH</sub>	1	0	0	0	1	1	0	1	8Dh

### Standby Mode

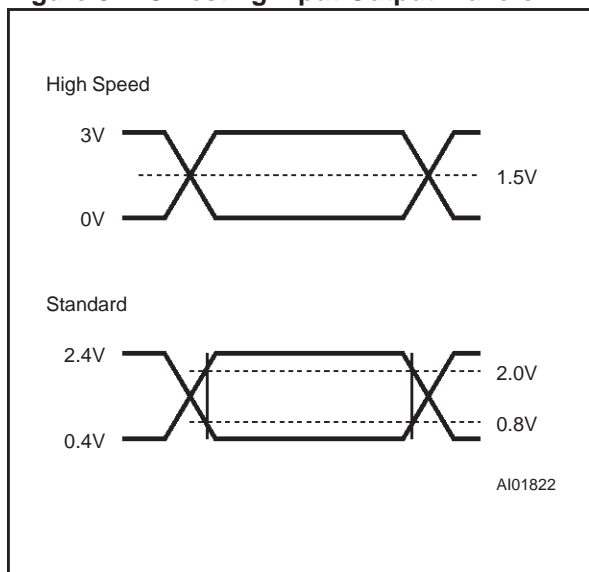
The M27V256 has a standby mode which reduces the supply current from 10mA to 10μA with low voltage operation V<sub>CC</sub> ≤ 3.6V, see Read Mode DC Characteristics table for details. The M27V256 is

placed in the standby mode by applying a CMOS high signal to the  $\bar{E}$  input. When in the standby mode, the outputs are in a high impedance state, independent of the  $\bar{G}$  input.

**Table 5. AC Measurement Conditions**

	High Speed	Standard
Input Rise and Fall Times	≤ 10ns	≤ 20ns
Input Pulse Voltages	0 to 3V	0.4V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

**Figure 3. AC Testing Input Output Waveform**



**Figure 4. AC Testing Load Circuit**



**Table 6. Capacitance <sup>(1)</sup>** (T<sub>A</sub> = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V		6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V		12	pF

Note: Sampled only, not 100% tested.

**Two Line Output Control**

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

- a. the lowest possible memory power dissipation,
- b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines,  $\bar{E}$  should be decoded and used as the primary device selecting function, while  $\bar{G}$  should be made a common connection to all devices in the array and connected to the READ line from the

system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

**System Considerations**

The power switching characteristics of Advance CMOS EPROMs require careful decoupling of the devices. The supply current, I<sub>CC</sub>, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of  $\bar{E}$ . The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

**Table 7. Read Mode DC Characteristics (1)**

(TA = 0 to 70°C or -40 to 85°C; VCC = 3.3V ± 10%; VPP = VCC)

Symbol	Parameter	Test Condition	Min	Max	Unit
ILI	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±10	μA
ILO	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±10	μA
ICC	Supply Current	$\bar{E} = V_{IL}, \bar{G} = V_{IL}, I_{OUT} = 0mA,$ $f = 5MHz, V_{CC} \leq 3.6V$		10	mA
ICC1	Supply Current (Standby) TTL	$\bar{E} = V_{IH}$		1	mA
ICC2	Supply Current (Standby) CMOS	$\bar{E} > V_{CC} - 0.2V, V_{CC} \leq 3.6V$		10	μA
I <sub>PP</sub>	Program Current	$V_{PP} = V_{CC}$		10	μA
V <sub>IL</sub>	Input Low Voltage		-0.3	0.8	V
V <sub>IH</sub> (2)	Input High Voltage		2	V <sub>CC</sub> + 1	V
V <sub>OL</sub>	Output Low Voltage	$I_{OL} = 2.1mA$		0.4	V
V <sub>OH</sub>	Output High Voltage TTL	$I_{OH} = -400\mu A$	2.4		V
	Output High Voltage CMOS	$I_{OH} = -100\mu A$	V <sub>CC</sub> - 0.7V		V

Note: 1. VCC must be applied simultaneously with or before VPP and removed simultaneously or after VPP.

2. Maximum DC voltage on Output is VCC + 0.5V.

**Table 8A. Read Mode AC Characteristics (1)**

(TA = 0 to 70 °C or -40 to 85°; VCC = 3.3V ± 10%; VPP = VCC)

Symbol	Alt	Parameter	Test Condition	M27V256				Unit
				-90 (3)		-100		
				Min	Max	Min	Max	
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address Valid to Output Valid	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$		90		100	ns
t <sub>ELQV</sub>	t <sub>CE</sub>	Chip Enable Low to Output Valid	$\bar{G} = V_{IL}$		90		100	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable Low to Output Valid	$\bar{E} = V_{IL}$		40		45	ns
t <sub>EHQZ</sub> (2)	t <sub>DF</sub>	Chip Enable High to Output Hi-Z	$\bar{G} = V_{IL}$	0	25	0	30	ns
t <sub>GHQZ</sub> (2)	t <sub>DF</sub>	Output Enable High to Output Hi-Z	$\bar{E} = V_{IL}$	0	25	0	30	ns
t <sub>AXQX</sub>	t <sub>OH</sub>	Address Transition to Output Transition	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$	0		0		ns

Note: 1. VCC must be applied simultaneously with or before VPP and removed simultaneously or after VPP.

2. Sampled only, not 100% tested.

3. Speed obtained with High Speed AC measurement conditions.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1μF ceramic capacitor be used on every device between VCC and VSS. This should be a high frequency capacitor of low inherent inductance and should be

placed as close to the device as possible. In addition, a 4.7μF bulk electrolytic capacitor should be used between VCC and VSS for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

**Table 8B. Read Mode AC Characteristics (1)**

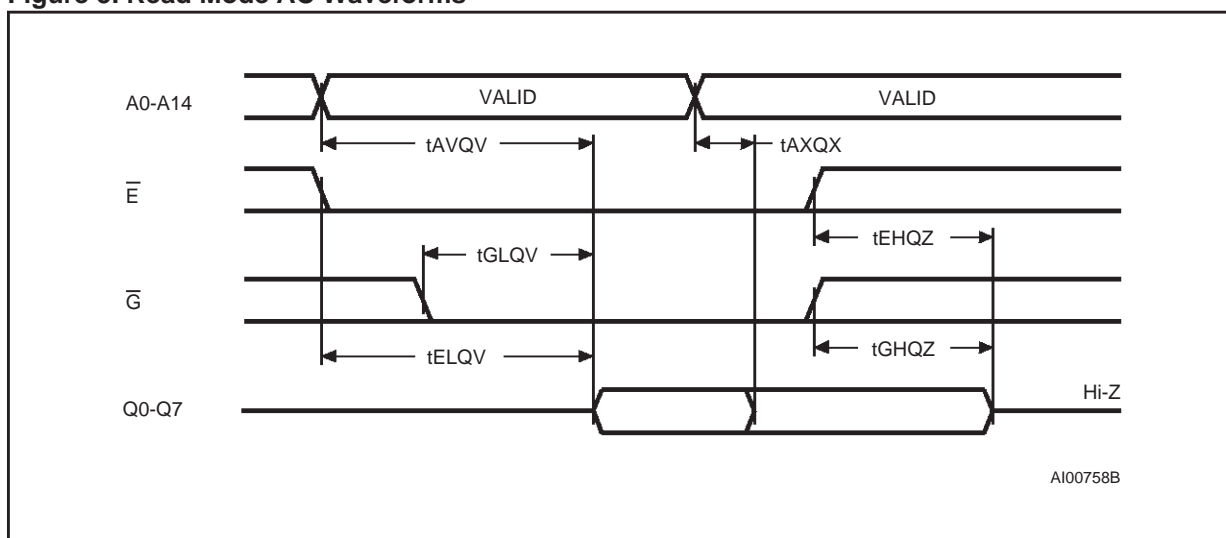
( $T_A = 0$  to  $70^\circ\text{C}$  or  $-40$  to  $85^\circ\text{C}$ ;  $V_{CC} = 3.3\text{V} \pm 10\%$ ;  $V_{PP} = V_{CC}$ )

Symbol	Alt	Parameter	Test Condition	M27V256						Unit
				-120		-150		-200		
				Min	Max	Min	Max	Min	Max	
$t_{AVQV}$	$t_{ACC}$	Address Valid to Output Valid	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$		120		150		200	ns
$t_{ELQV}$	$t_{CE}$	Chip Enable Low to Output Valid	$\bar{G} = V_{IL}$		120		150		200	ns
$t_{GLQV}$	$t_{OE}$	Output Enable Low to Output Valid	$\bar{E} = V_{IL}$		45		50		60	ns
$t_{EHQZ}^{(2)}$	$t_{DF}$	Chip Enable High to Output Hi-Z	$\bar{G} = V_{IL}$	0	35	0	40	0	50	ns
$t_{GHQZ}^{(2)}$	$t_{DF}$	Output Enable High to Output Hi-Z	$\bar{E} = V_{IL}$	0	35	0	40	0	50	ns
$t_{AXQX}$	$t_{OH}$	Address Transition to Output Transition	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$	0		0		0		ns

Note: 1.  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

2. Sampled only, not 100% tested.

**Figure 5. Read Mode AC Waveforms**



**Programming**

The M27V256 has been designed to be fully compatible with the M27C256B and has the same electronic signature. As a result the M27V256 can be programmed as the M27C256B on the same programming equipments applying 12.75V on  $V_{PP}$  and 6.25V on  $V_{CC}$  by the use of the same PRESTO II algorithm. When delivered (and after each erasure for UV EPROM), all bits of the M27V256 are in the '1' state. Data is introduced by selectively programming '0's into the desired bit locations.

Although only '0's will be programmed, both '1's and '0's can be present in the data word. The only way to change a '0' to a '1' is by die exposition to ultraviolet light (UV EPROM). The M27V256 is in the programming mode when  $V_{PP}$  input is at 12.75V,  $\bar{G}$  is at  $V_{IH}$  and  $\bar{E}$  is pulsed to  $V_{IL}$ . The data to be programmed is applied to 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.  $V_{CC}$  is specified to be  $6.25\text{V} \pm 0.25\text{V}$ .

**Table 9. Programming Mode AC Characteristics (1)**  
 ( $T_A = 25\text{ }^\circ\text{C}$ ;  $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$ ;  $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$ )

Symbol	Parameter	Test Condition	Min	Max	Unit
$I_{LI}$	Input Leakage Current	$V_{IL} \leq V_{IN} \leq V_{IH}$		$\pm 10$	$\mu\text{A}$
$I_{CC}$	Supply Current			50	mA
$I_{PP}$	Program Current	$\bar{E} = V_{IL}$		50	mA
$V_{IL}$	Input Low Voltage		-0.3	0.8	V
$V_{IH}$	Input High Voltage		2	$V_{CC} + 0.5$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1\text{mA}$		0.4	V
$V_{OH}$	Output High Voltage TTL	$I_{OH} = -1\text{mA}$	3.6		V
$V_{ID}$	A9 Voltage		11.5	12.5	V

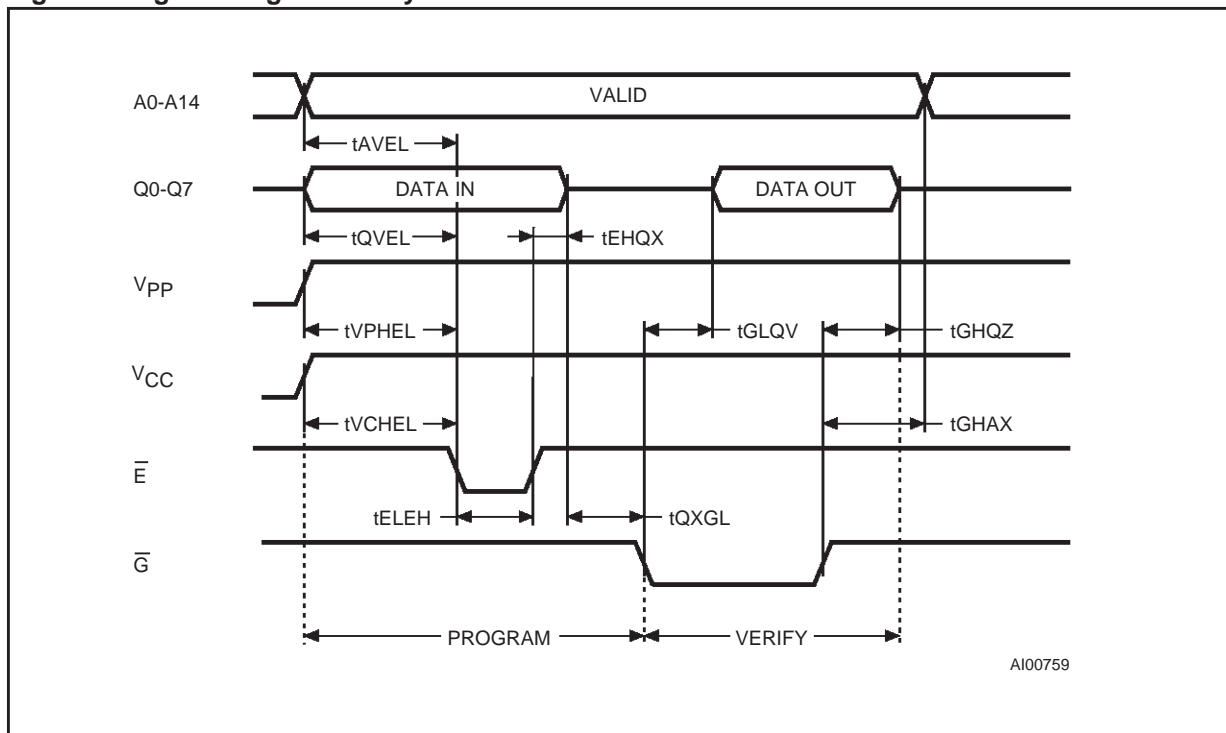
Note:  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

**Table 10. Programming Mode AC Characteristics (1)**  
 ( $T_A = 25\text{ }^\circ\text{C}$ ;  $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$ ;  $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$ )

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
$t_{AVEL}$	$t_{AS}$	Address Valid to Chip Enable Low		2		$\mu\text{s}$
$t_{QVEL}$	$t_{DS}$	Input Valid to Chip Enable Low		2		$\mu\text{s}$
$t_{VPHEL}$	$t_{VPS}$	$V_{PP}$ High to Chip Enable Low		2		$\mu\text{s}$
$t_{VCHL}$	$t_{VCS}$	$V_{CC}$ High to Chip Enable Low		2		$\mu\text{s}$
$t_{ELEH}$	$t_{PW}$	Chip Enable Program Pulse Width		95	105	$\mu\text{s}$
$t_{EHQX}$	$t_{DH}$	Chip Enable High to Input Transition		2		$\mu\text{s}$
$t_{QXGL}$	$t_{OES}$	Input Transition to Output Enable Low		2		$\mu\text{s}$
$t_{GLQV}$	$t_{OE}$	Output Enable Low to Output Valid			100	ns
$t_{GHQZ}$	$t_{DFP}$	Output Enable High to Output Hi-Z		0	130	ns
$t_{GHAX}$	$t_{AH}$	Output Enable High to Address Transition		0		ns

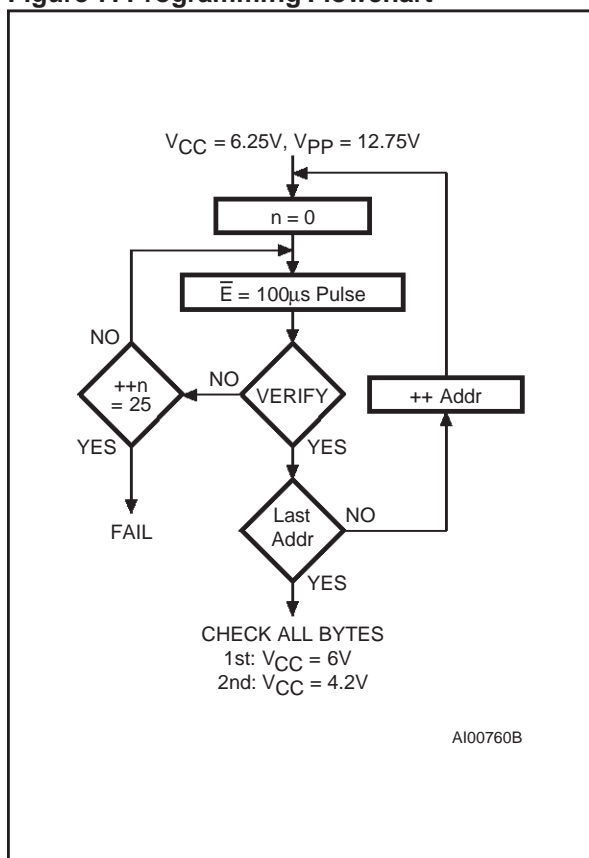
Note:  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

Figure 6. rogramming and Verify Modes AC Waveforms



AI00759

Figure 7. Programming Flowchart



AI00760B

**PRESTO II Programming Algorithm**

PRESTO II Programming Algorithm allows to program the whole array with a guaranteed margin, in a typical time of 3.5 seconds. Programming with PRESTO II involves the application of a sequence of 100µs program pulses to each byte until a correct verify occurs (see Figure 7). During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE at V<sub>CC</sub> much higher than 3.6V provides necessary margin to each programmed cell.

**Program Inhibit**

Programming of multiple M27V256s in parallel with different data is also easily accomplished. Except for  $\bar{E}$ , all like inputs including  $\bar{G}$  of the parallel M27V256 may be common. A TTL low level pulse applied to a M27V256's  $\bar{E}$  input, with V<sub>PP</sub> at 12.75 V, will program that M27V256. A high level  $\bar{E}$  input inhibits the other M27V256s from being programmed.

**Program Verify**

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with  $\bar{G}$  at V<sub>IL</sub>,  $\bar{E}$  at V<sub>IH</sub>, V<sub>PP</sub> at 12.75V and V<sub>CC</sub> at 6.25V.





### On-Board Programming

The M27V256 can be directly programmed in the application circuit. See the relevant Application Note AN620.

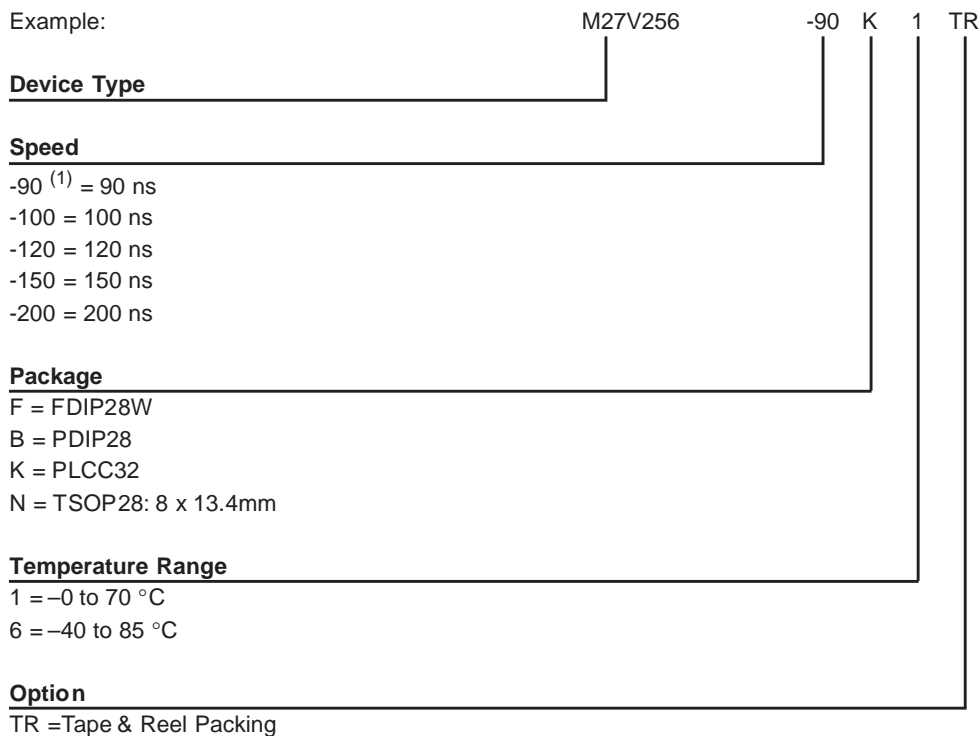
### Electronic Signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the  $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$  ambient temperature range that is required when programming the M27V256. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27V256, with  $V_{CC} = V_{PP} = 5\text{V}$ . Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from  $V_{IL}$  to  $V_{IH}$ . All other address lines must be held at  $V_{IL}$  during Electronic Signature mode. Byte 0 ( $A0=V_{IL}$ ) represents the manufacturer code and byte 1 ( $A0=V_{IH}$ ) the device identifier code. For the STMicroelectronics M27V256, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7. Note that the M27V256 and M27C256B have the same identifier bytes.

### ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27V256 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27V256 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27V256 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27V256 window to prevent unintentional erasure. The recommended erasure procedure for the M27V256 is exposure to short wave ultraviolet light which has wavelength 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of  $15\text{ W-sec/cm}^2$ . The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with  $12000\text{ }\mu\text{W/cm}^2$  power rating. The M27V256 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

**Table 11. Ordering Information Scheme**



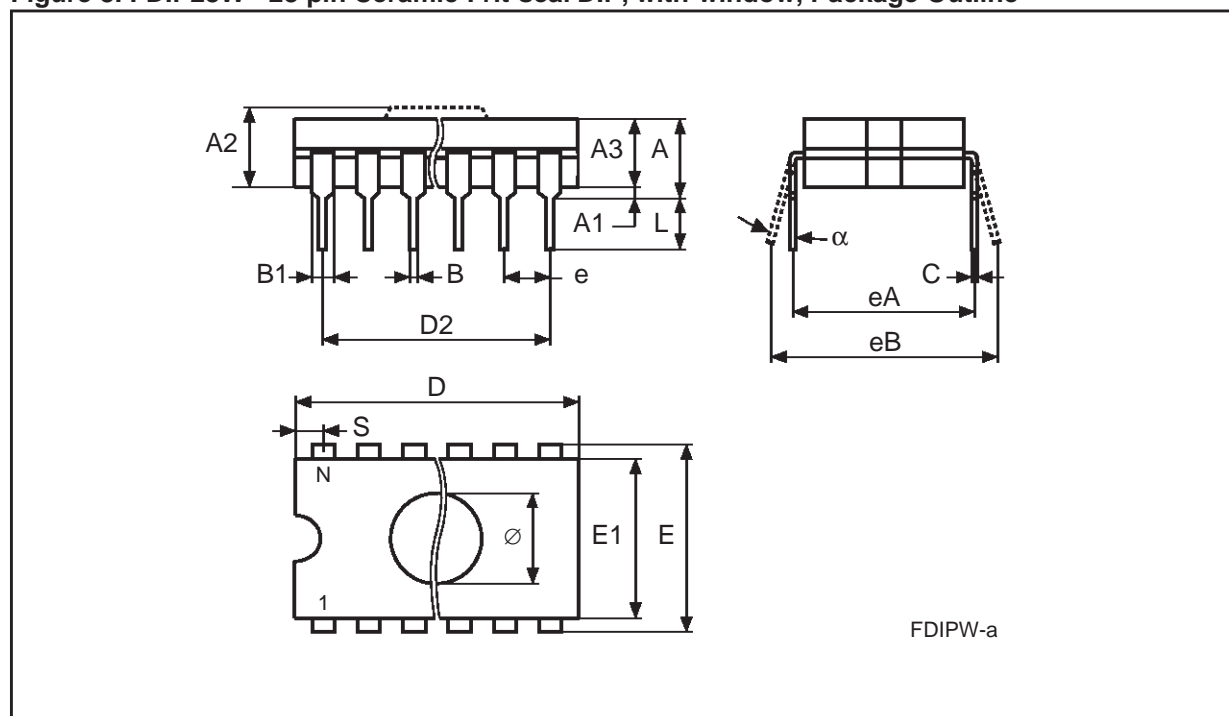
Note: 1. High Speed, see AC Characteristics section for further information.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 12. FDIP28W - 28 pin Ceramic Frit-seal DIP, with window, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.72			0.225
A1		0.51	1.40		0.020	0.055
A2		3.91	4.57		0.154	0.180
A3		3.89	4.50		0.153	0.177
B		0.41	0.56		0.016	0.022
B1	1.45	–	–	0.057	–	–
C		0.23	0.30		0.009	0.012
D		36.50	37.34		1.437	1.470
D2	33.02	–	–	1.300	–	–
E	15.24	–	–	0.600	–	–
E1		13.06	13.36		0.514	0.526
e	2.54	–	–	0.100	–	–
eA	14.99	–	–	0.590	–	–
eB		16.18	18.03		0.637	0.710
L		3.18			0.125	
S		1.52	2.49		0.060	0.098
∅	7.11	–	–	0.280	–	–
α		4°	11°		4°	11°
N		28			28	

Figure 8. FDIP28W - 28 pin Ceramic Frit-seal DIP, with window, Package Outline

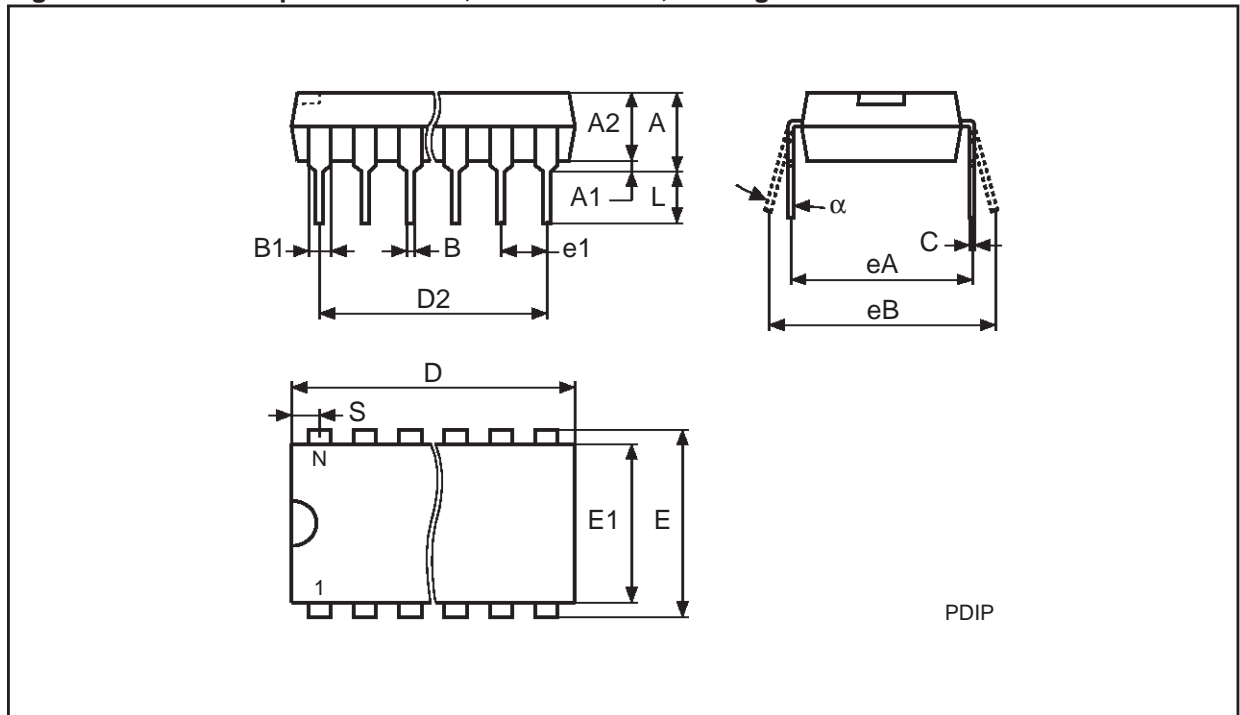


Drawing is not to scale.

Table 13. PDIP28 - 28 pin Plastic DIP, 600 mils width, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		–	5.08		–	0.200
A1		0.38	–		0.015	–
A2		3.56	4.06		0.140	0.160
B		0.38	0.51		0.015	0.020
B1	1.52	–	–	0.060	–	–
C		0.20	0.30		0.008	0.012
D		36.83	37.34		1.450	1.470
D2	33.02	–	–	1.300	–	–
E	15.24	–	–	0.600	–	–
E1		13.59	13.84		0.535	0.545
e1	2.54	–	–	0.100	–	–
eA	14.99	–	–	0.590	–	–
eB		15.24	17.78		0.600	0.700
L		3.18	3.43		0.125	0.135
S		1.78	2.08		0.070	0.082
$\alpha$		0°	10°		0°	10°
N		28			28	

Figure 9. PDIP28 - 28 pin Plastic DIP, 600 mils width, Package Outline

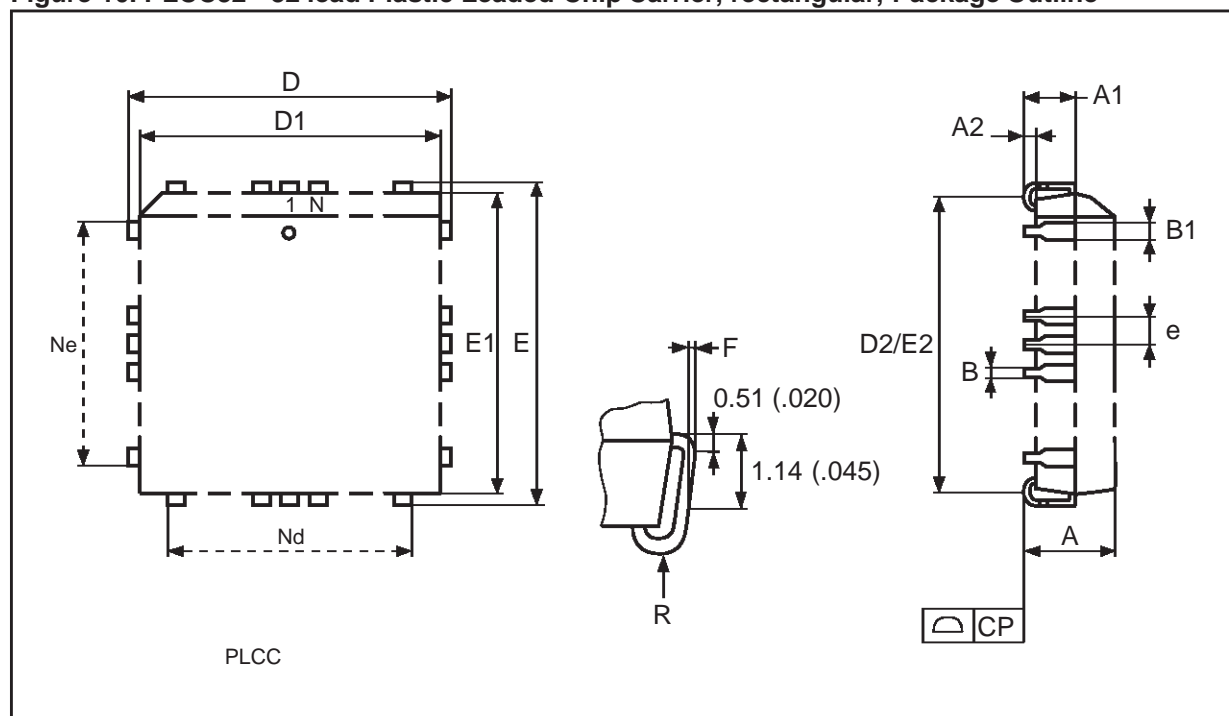


Drawing is not to scale.

Table 14. PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
A2		–	0.38		–	0.015
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
F		0.00	0.25		0.000	0.010
R	0.89	–	–	0.035	–	–
N		32			32	
Nd		7			7	
Ne		9			9	
CP			0.10			0.004

Figure 10. PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular, Package Outline

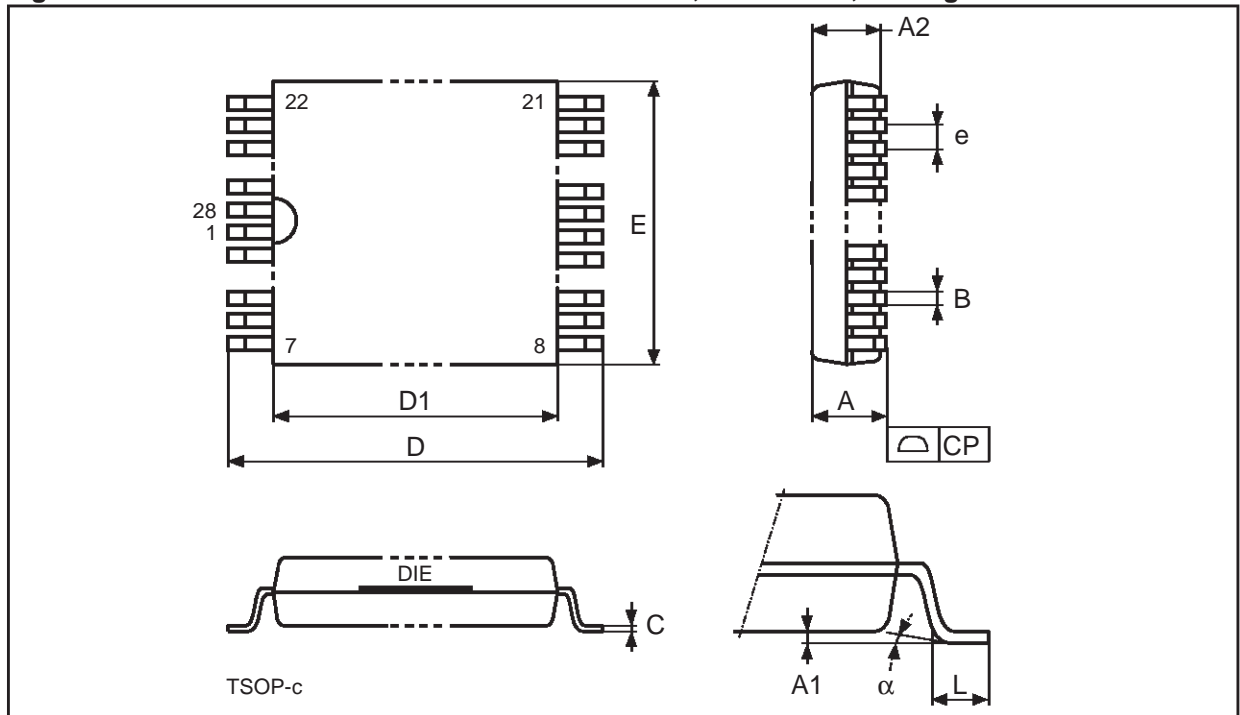


Drawing is not to scale.

Table 15. TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.00	1.25		0.039	0.049
A1			0.20			0.008
A2		0.95	1.05		0.037	0.041
B			0.30			0.012
C		0.10	0.21		0.004	0.008
D		13.10	13.70		0.516	0.539
D1		11.70	11.90		0.461	0.469
E		7.90	8.25		0.311	0.325
e	0.55	-	-	0.022	-	-
L		0.30	0.70		0.012	0.028
$\alpha$		0°	5°		0°	5°
N	28			28		
CP			0.10			0.004

Figure 11. TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm, Package Outline



Drawing is not to scale

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