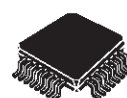


5 BIT DYNAMIC DAC CONTROLLER FOR MOBILE CPU

PRELIMINARY DATA

- DYNAMIC DAC DETECTION ON CHIP
- PROGRAMMABLE OUTPUT FROM 0.925V TO 2.0V WITH 0.05V AND 0.025V BINARY STEPS
- ULTRA HIGH EFFICIENCY
- SEPARATE 5V BIAS SUPPLY AVAILABLE FOR HIGH EFFICIENCY PERFORMANCE
- EXCELLENT OUTPUT ACCURACY $\pm 1\%$ OVER LINE, LOAD AND TEMPERATURE VARIATIONS
- HIGH PRECISION INTERNAL REFERENCE DIGITALLY TRIMMED
- OPERATING SUPPLY VOLTAGE FROM 4.75V TO 25V
- VERY FAST LOAD TRANSIENT
- REMOTE SENSING INPUTS
- INTERNAL LINEAR REGULATOR 2.5V /150mA, $\pm 2\%$ PRECISION
- POWER MANAGEMENT
 - PROGRAMMABLE POWER-UP TIME
 - POWER GOOD OUTPUT, SKIP MODE
 - OUTPUT OVERVOLTAGE PROTECTION
 - OUTPUT UNDERVOLTAGE LOCKOUT
- OPERATING FREQUENCY UP TO 1MHz
- MEETS INTEL MOBILE PENTIUM® III



TQFP32
(7mm x 7mm)

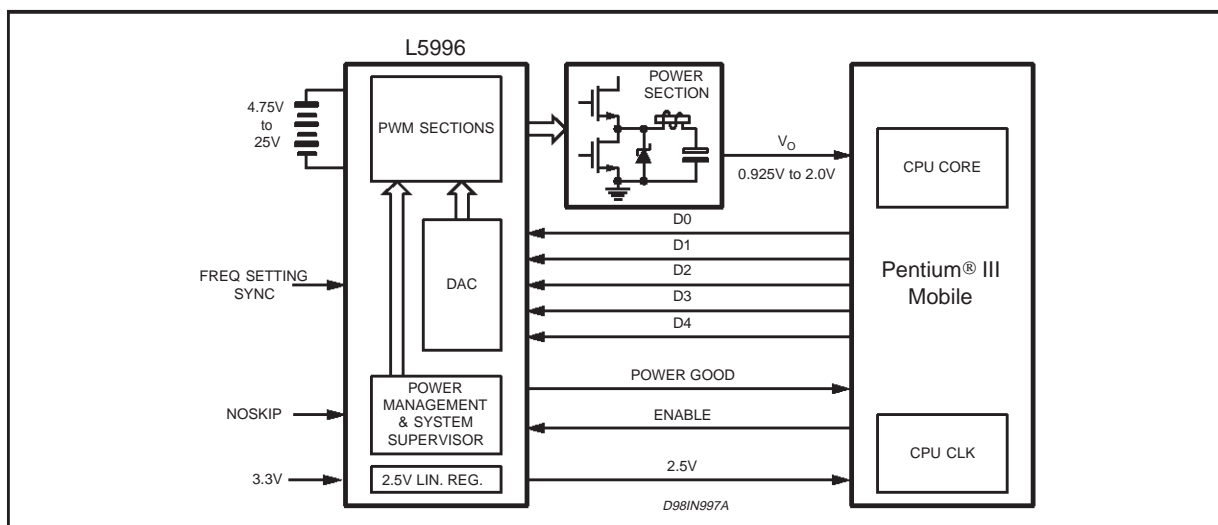
Application

- ADVANCED MICROPROCESSOR SUPPLIES
- POWER SUPPLY FOR PENTIUM® III INTEL MOBILE

DESCRIPTION

The L5996 is a power supply controller that offers a complete power management for notebook CPUs of the next generation especially for mobile Pentium III. A high precise 5 bit digital to analog converter (DAC) allows to adjust the output voltage from 0.925V to 2.0V. Dynamic DAC code changes are detected on chip in order to switch the output voltage between 1.3V and 1.45V in less than 100 μ s. The high precision internal refer-

TYPICAL APPLICATION CIRCUIT



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{Th\ j-amb}$	Thermal Resistance Junction to Ambient	60	°C/W

ELECTRICAL CHARACTERISTICS ($V_{IN} = 12V$; $T_i = 25^\circ C$, OSC = GND, unless otherwise specified)● = specifications referred to T_J from 0 to $70^\circ C$.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS						
V_{IN}	Input Supply Voltage	●	4.75		25	V
I_{OP}	Operating Quiescent Current	RGATE = HGATE = OPEN ENABLE = REG5	●	0.9	1.1	mA
I_{SB}	Stand-By Current	ENABLE = GND $V_{IN} = 12V$ $V_{IN} = 25V$	●	80 100	150 180	μA μA
INTERNAL REGULATOR (VREG5)						
V_{REG5}	Output Voltage	$V_{IN} = 7.5V$ to $25V$ $I_{LOAD} = 0$ to $5mA$, $C_{REG5} = 4.7\mu F$		4.9	5.0	5.1 V
I_{REG5}	Total Current Capability	$C_{REG5} = 4.7\mu F$ $V_{IN} = 5.5V$ $V_{IN} \geq 6V$		25	60	mA mA
	Switch-Over Threshold Voltage			4.3	4.5	4.7 V
	Current Capability (internal switch on)	$V_{5SW} = 4.5$ to $5.5V$ $V_{REG5} \geq 4.4V$		25		mA
2.5V REFERENCE VOLTAGE						
$V_{O2.5}$	Regulated Voltage	$V_{IN\ 2.5} = 3.3V$ $C_{VO\ 2.5} = 47\mu F$ $I_{O\ 2.5} = 10mA$	●	2.45	2.5	2.55 V
	Regulation over Line and Load	$6V < V_{IN} < 25V$ $V_{IN\ 2.5} = 3.3V$ $I_{O\ 2.5} = 0-150mA$	●	2.425	2.5	2.575 V
$I_{VO\ 2.5\ MAX}$	Current Limit	$V_{IN\ 2.5} = 3.3V$			500	mA
PROGRAMMABLE REFERENCE VOLTAGE AND VBG						
V_{PROG}	Accuracy	V_{ID0} , V_{ID1} , V_{ID2} , V_{ID3} , V_{ID4} see Table 1.	●	-0.5%	V_{PROG}	+0.5% V
V_{FB}	Output Voltage Accuracy	Line and Load Regulation included, V_{ID0} , V_{ID1} , V_{ID2} , V_{ID3} , V_{ID4} , see Table 1.	●	-1%	V_{PROG}	+1% V
V_{BG}	Band Gap reference	$C_{VBG} = 220nF$	●	1.240	1.246	1.252 V
POWER MANAGEMENT						
	Enable Voltage	HIGH LEVEL		2.4		V
	Disable Voltage	LOW LEVEL			0.8	V
	Power Good Saturation Voltage	$I_{sink} = 400\mu A$			0.4	V
	NOSKIP Mode (Active high)	High Level Low Level		2.4	0.8	V V
	Output UVLO Threshold	OVP = GND		60	70	80 %
	Output UVLO Lockout Time	Depending on C_{SS} value			775	ms/ μF

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
PROTECTION FUNCTIONS							
V _{8-V7}	Over-Current Threshold Voltage	V _{SSTART} = 3.1V	●	48	60	72	mV
	Pulse Skipping Mode Threshold Voltage	NOSKIP = HIGH		7	11	15	mV
	Zero Crossing Threshold			-4		+4	mV
	Under-Voltage Threshold			V _{prog} -13%	V _{prog} -10%	V _{prog} -7%	V
	Upper Over-Voltage Threshold			V _{prog} +7%	V _{prog} +10%	V _{prog} +13%	V
	Lower Over-Voltage Threshold				V _{prog} -4.5%		V
	Over-Voltage Propagation Time					1.5	μs
	Under-Voltage Propagation Time					1.5	μs
SOFT START							
	Soft start source current			3.2	4	4.8	μA
	Soft start clamp voltage				3.1		V
OSCILLATOR AND SYNC							
f _{osc}	Fixed frequency	OSC = 0V; FREQ = REG5	●	225	250	275	KHz
		OSC = REG5 FREQ = REG5	●	180	200	220	KHz
f _{SINK MIN}	Minimum Synchronizable external frequency	FREQ = REG5 OSC = EXTERNAL SIGNAL				120	KHz
	Sync pulse width	Rising edge mode		200			ns
	Sync pulse amplitude			3		5.5	V
fosc	Operating switching frequency	Rext connected between FREQ and GND, OSC connect to REG5 or GND Rext = 680kΩ Rext = 40kΩ	●			100 1	kHz MHz
HIGH AND LOW SIDE GATE DRIVERS							
I _{OH5}	Output high source peak current	HSTRAP = RSTRAP = REG5			550		mA
R _{H5}	Output high sink impedance	I _{test} = 100mA, HSTRAP = RSTRAP = REG5			3.5		Ω
I _{OH12}	Output high source peak current	HSTRAP = RSTRAP = 12V			2		A
R _{H12}	Output high sink impedance	I _{test} = 100mA, HSTRAP - RSTRAP = 12V			2		Ω
I _{OL5}	Output low peak current	HSTRAP = RSTRAP = 5V			500		mA
R _{L5}	Output low impedance	I _{test} = 100mA, HSTRAP = RSTRAP = 5V			3		Ω
I _{OL12}	Output low peak current	HSTRAP = RSTRAP = 12V			2		A
R _{L12}	Output low Impedance	I _{test} = 100mA, HSTRAP = RSTRAP = 12V			2		Ω
T _{CC}	Dead Time	GATE low to high		60			ns

FUNCTIONAL PIN DESCRIPTION

ENABLE(pin1): Enable input. A high level ($>2.4V$) enables the device, a low level ($<0.8V$) shuts it down. As ENABLE drops below $0.8V$, the drivers are turned off and all internal functions are disabled except REG5. In this condition the stand by current is less than $80\mu A$ at $V_{IN} = 12V$.

VIN(pin2): Device supply voltage. Input voltage range at this pin is $4.75V$ to $25V$ and the operating current requirement at $12V$ is $650\mu A$.

REG5(pin3): $5V$ Regulator supply. Used also to supply the bootstrap capacitor. A minimum $2.2\mu F$ ceramic capacitor connected to PWRGND is required.

V5SW(pin4): $5V$ supply line. Connecting to $5V$ bus ($4.75V$ to $5.5V$) the device is no longer powered by VIN but by this pin and the internal linear regulator is disconnected increasing the efficiency.

DISPROT (pin5) Disable Protection Functions. A high level ($3.3V$ CMOS LOGIC) on this pin disables the undervoltage and the overvoltage protection. Tie this pin to Vss for normal operation.

SSTART(pin6): Soft Start. The soft-start time is programmed by an external capacitor connected between this pin and SGND. The internal current generator forces $4\mu A$ through the capacitor implementing the soft start function.

HRSNS(pin7): Error summing current sense non inverting input.

LRSNS(pin8): Error summing current sense inverting input.

VFB(pin9): Regulator voltage feedback input. Connect close to the CPU input supply pin realise an accurate voltage regulation. VFB internally is connected to the window comparator that is used to increase the performance during the load transient.

COMP(pin10): Regulator stability compensation pin. The compensation is realised internally and normally it is not necessary to connect any external components to this pin.

VPROG(pin11): Reference voltage test pin. This pin provides the DAC output and should be decoupled to ground using a $0.22\mu F$ ceramic capacitor. No load has to be connected.

SNSGND(pin12): Remote ground sense. This pin is internally connected to the low power circuitry and for a precise output voltage regulation can be connected to the output capacitor negative terminal.

VIN2.5(pin13): $2.5V$ linear supply voltage. Is available on-chip a linear regulator useful for the $2.5V$ bus. A max input voltage of $3.3V$ is recommended at I_{omax} ($150mA$).

Vo2.5(pin14): $2.5V$ linear regulator output. The linear regulator is realised with an internal NPN transistor with $\pm 2\%$ output accuracy. A minimum of $47\mu F$ capacitor connected versus PWRGND is required.

VBG(pin15): Band-gap reference voltage. A min $220nF$ ceramic capacitor is required to assure the band gap stability and noise immunity.

VSS(pin16): Signal ground. This pin could be connected to the PWRGND pin.

FREQ(pin17): Connecting an external resistor versus ground is possible to select the switching frequency between $100kHz$ and $1MHz$. Using an $R_{ext}=680k$ the fsw is $100kHz$, using an $R_{ext} = 40k$ the fsw is $1MHz$. In this condition is recommended to connect the OSC pin to REG5 or to VSS.

OSC(pin18): Connecting to REG5 is able to set the switching frequency at $200kHz$, connecting to VSS is able to set the switching frequency at $250kHz$. An external pulsed signal, with an amplitude higher than $2.4V$, could synchronise the device. In all these conditions pin FREQ has to be connected to REG5.

OVP/CURLIM(pin19): Over voltage protection and reduced current limit window. If the output voltage reaches the 10% above the programmed voltage (VPROG) this pin is driven low the high side driver is turned off and the low, side driver is turned on. All the internal blocks are active. The device uses OVP function to discharge the output during HIGH_TO_LOW core voltage transition. The pin is driven low also during LOW_TO_HIGH core voltage transition. The pin will stay low as

long as the current limit value is reduced with respect to the normal operating value. This is done to limit voltage overshoots during core voltage changes. Making this signal externally available simplifies system debugging.

VID0-4(pin20-24): Voltage Identification code input. These open collector compatible inputs are used to program the output voltage as specified in Table 1. Every pin has an internal pull up. If all four pins are high or floating, the output voltage and the 2.5V regulator are suspended and the POWERGOOD is low.

NOSKIP(pin25): Pulse skipping mode control. A high level (>2.4V) disables pulse skipping in low load condition, a low level (>0.8V) enables it.

HSRC(pin26): High side N-Channel switch source connection. This pin provides the return path for the high side driver.

HGATE(pin27): Gate driver output, high side N-Channel switch. The driver internal impedance is about 4Ω at VIN=12V.

HSTRAP(pin28): Bootstrap capacitor pin. This pin

provide to supply the high side driver sinking the current by the bootstrap capacitor.

RSTRAP(pin29): Synchronous rectifier gate driver supply voltage. This pin could be connected to REG5 to reduce the switching losses due to the external Mosfets gate capacitance. This is useful to maintain an high efficiency at light load.

RGATE(pin30): Gate driver output, low side N-Channel switch. The driver internal impedance is about 3Ω at VIN=12V.

PWRGND(pin31): Power ground. This pin has to be connected closely to the low side mosfet source in order to reduce the noise injected into the IC.

POWER GOOD(pin32): Open drain power good output. This pin is pulled low if the output voltage is not within $\pm 10\%$ and the 2.5V output is lower than 2.175V (-13%). The pin is pulled low also if REG5, VPROG and VBG have not reached the expected values. This test could be useful in an assembling fault condition.

Table 1. VID [4:0] AND corresponding +VCC_CPU_CORE ranges

VID[4:0]	+VCC_CPU_CORE	VID[4:0]	+VCC_CPU_CORE
00000	2.00V	10000	1.275V
00001	1.95V	10001	1.250V
00010	1.90V	10010	1.225V
00011	1.85V	10011	1.200V
00100	1.80V	10100	1.175V
00101	1.75V	10101	1.150V
00110	1.70V	10110	1.125V
00111	1.65V	10111	1.100V
01000	1.60V	11000	1.075V
01001	1.55V	11001	1.050V
01010	1.50V	11010	1.025V
01011	1.45V	11011	1.000V
01100	1.40V	11100	0.975V
01101	1.35V	11101	0.950V
01110	1.30V	11110	0.925V
01111	No CPU	11111	No CPU

Figure 1. Application Circuit

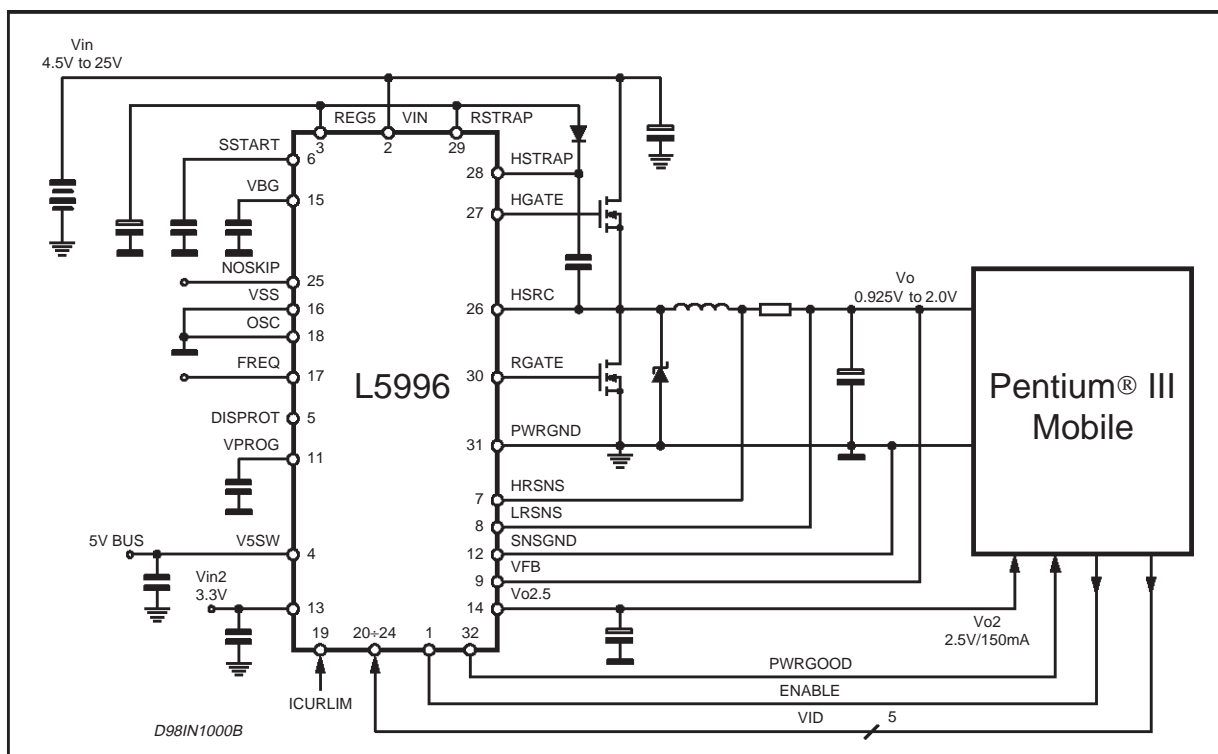
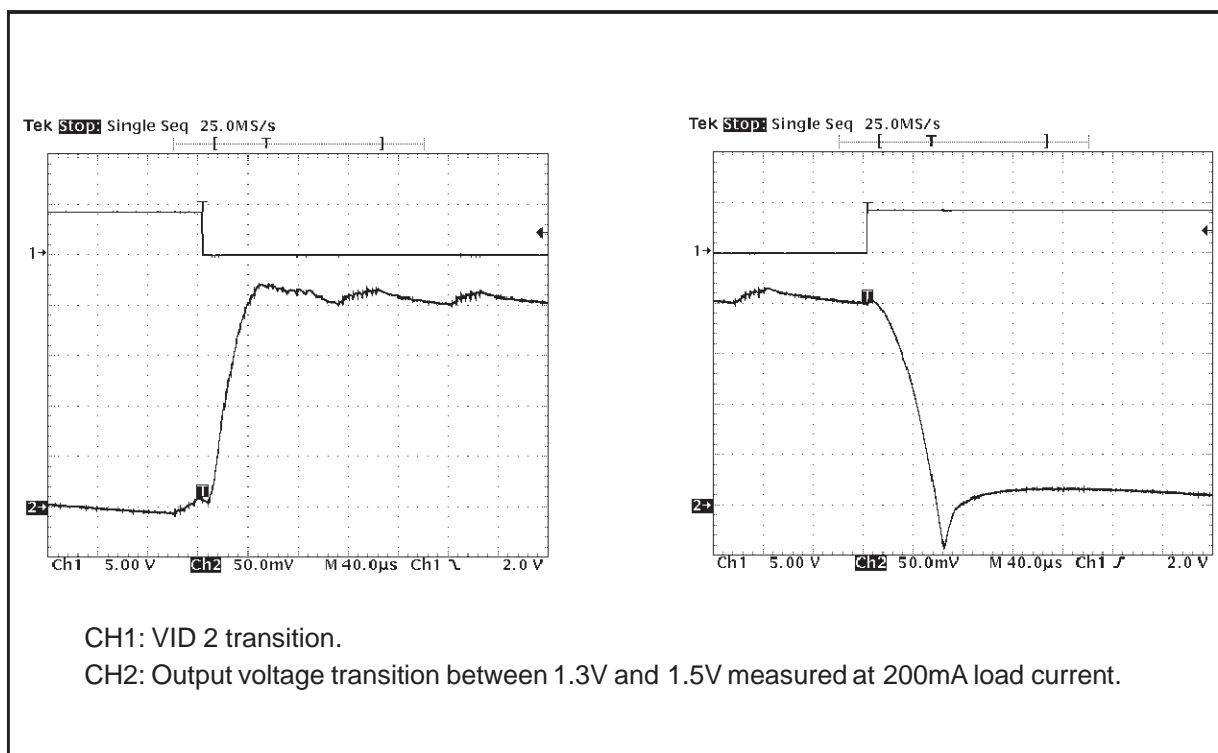
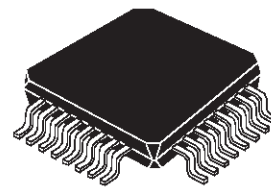


Figure 2. Output voltage transition between 1.3V and 1.5V measured at 200mA load current.

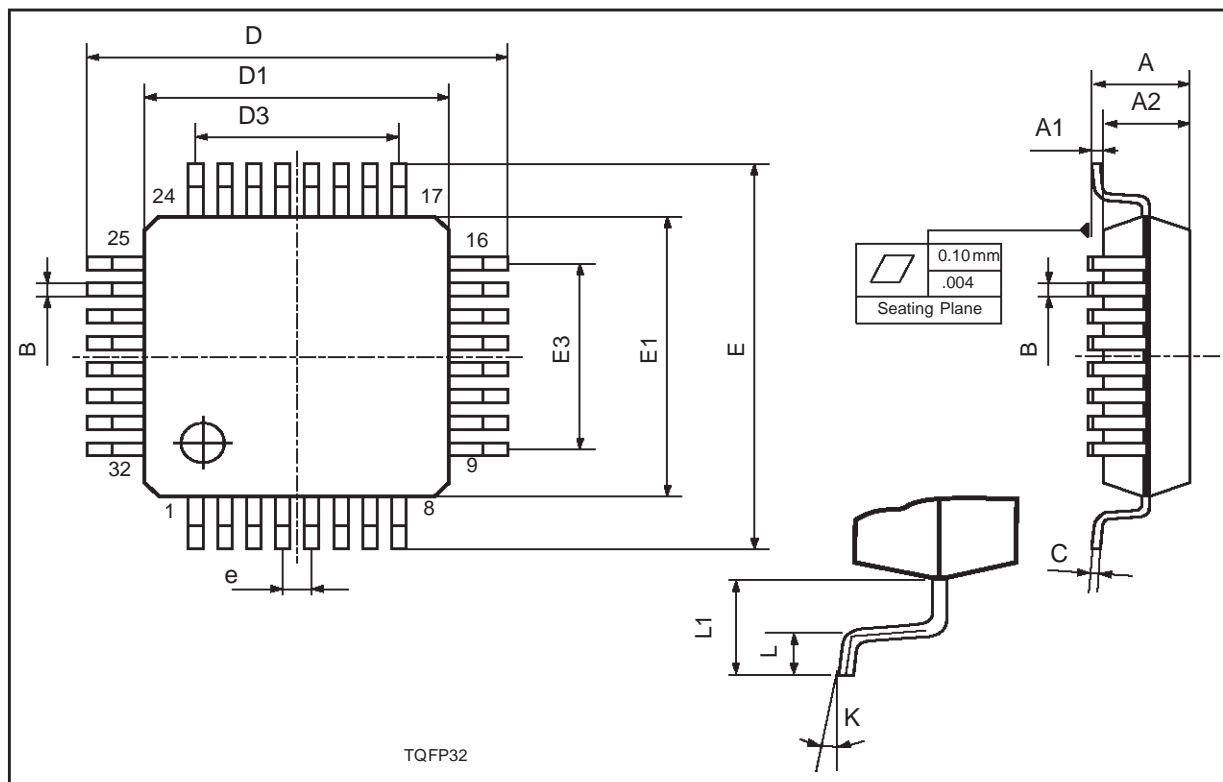


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.60			0.220	
e		0.80			0.031	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.60			0.220	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP32



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