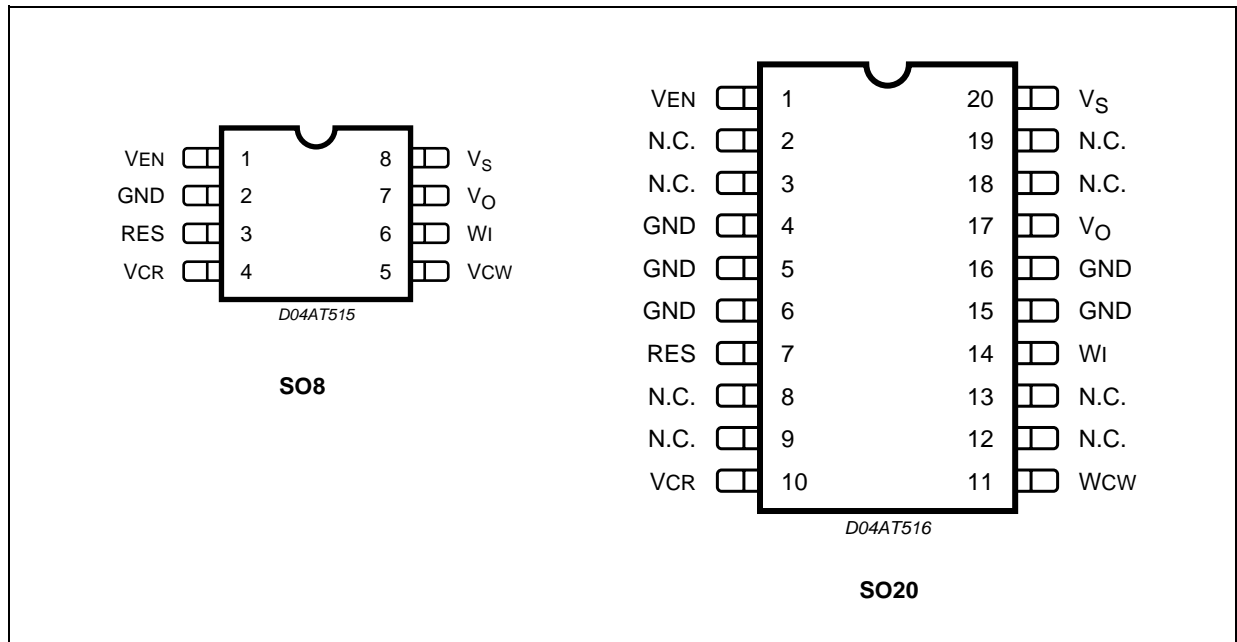


PIN DESCRIPTION

N. (SO8)	N. (SO20)	NAME	FUNCTION
1	1	WEn	Watchdog enable input. If high it activates the watchdog operation.
2	4	gnd	Ground reference
	5,6,15,16	gnd	Ground Connected these pins to a heat spreader ground
3	7	Res	Reset output. It is pulled down when output voltage goes below Vo_th or frequency at Wi is too low.
4	10	Vcr	Reset timing adjust. A capacitor between Vcr pin and gnd, sets the reset delay time (trd)
5	11	Vcw	Watchdog timer adjust A capacitor between Vcw pin and gnd, sets the time response of the watchdog monitor.
6	14	Wi	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated.
7	17	Vo	Voltage regulator output Block to ground with a capacitor >100nF (needed for regulator stability)
8	20	Vs	Supply voltage Block to ground directly at IC pin with a ceramic capacitor
	2,3,8,9,12,13,18,19	N. C.	not connected

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{Vsdc}	DC supply voltage	-0.3 to 40	V
I_{Vsdc}	Input current	internally limited	
V_{Vo}	DC output voltage	-0.3 to 6	V
I_{Vo}	DC output current	internally limited	
V_{Wi}	Watchdog input voltage	-0.3 to $V_{Vo} + 0.3$	V
V_{od}	Open drain output voltage (RES)	-0.3 to $V_{Vo} + 0.3$	V
I_{od}	Open drain output current (RES)	internally limited	
V_{cr}	Reset delay voltage	-0.3 to $V_{Vo} + 0.3$	V
V_{cw}	Watchdog delay voltage	-0.3 to $V_{Vo} + 0.3$	V
V_{WE_n}	Watchdog enable input	-0.3 to 40	V
T_j	Junction temperature	-40 to 150	°C
V_{ESD}	ESD voltage level (HBM-MIL STD 883C)	±2	kV

Note:

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

THERMAL DATA

Symbol	Parameter	SO8	SO12+4+4	Unit
$R_{th-j\ amb}$	Thermal Resistance Junction to ambient	130 to 180	50(*)	°C/W

(*) with 6 sq. cm on board heat sink

ELECTRICAL CHARACTERISTICS ($V_s = 5.6V$ to $31V$, $T_j = -40^\circ C$ to $+150^\circ C$ unless otherwise specified)

Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
GENERAL							
V_o	V_{o_ref}	Output voltage	$V_s=5.6$ to $31V$ $I_o=1$ to $150mA$	4.85	5.00	5.15	V
V_o	I_{short_13}	Short circuit current (1)	$V_s=13.5V$	160	210	250	mA
V_o	I_{lim}	Output current limitation (1)	$V_s=13.5V$	170	250	290	mA
V_s, V_o	V_{line}	Line regulation voltage	$V_s=5.6$ to $31V$ $I_o=1$ to $150mA$			25	mV
V_o	V_{load}	Load regulation voltage	$I_o=1$ to $150mA$			25	mV
V_s, V_o	V_{dp}	Drop voltage	$I_o=150mA$		180	400	mV
V_s, V_o	SVR	Ripple rejection	$f_r = 100$ Hz	55			dB
V_s, V_o	I_{qs_1}	Current consumption with watchdog not active $I_{qs_1} = I_{Vs} - I_o$	$V_s=13.5V, I_o<1mA,$ WE_n low		69	115	μA

Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Vs, Vo	I _{qs_10}	Current consumption with watchdog not active $I_{qs_10} = I_{Vs} - I_o$	Vs=13.5V, Io=10mA, WEn low		127	300	μA
Vs, Vo	I _{qs_50}	Current consumption with watchdog not active $I_{qs_50} = I_{Vs} - I_o$	Vs=13.5V, Io=50mA, WEn low		498	900	μA
Vs, Vo	I _{qs_150}	Current consumption with watchdog not active $I_{qs_150} = I_{Vs} - I_o$	Vs=13.5V, Io=150mA, WEn low		1.40	2	mA
Vs, Vo	I _{qn_1}	Current consumption with watchdog active $I_{qn_1} = I_{Vs} - I_o$	Vs=13.5V, Io<1mA, WEn high		110	170	μA
Vs, Vo	I _{qn_10}	Current consumption with watchdog active $I_{qn_10} = I_{Vs} - I_o$	Vs=13.5V, Io=10mA, WEn high		168	350	μA
Vs, Vo	I _{qn_50}	Current consumption with watchdog active $I_{qn_50} = I_{Vs} - I_o$	Vs=13.5V, Io=50mA, WEn high		538	1000	μA
Vs, Vo	I _{qn_150}	Current consumption with watchdog active $I_{qn_150} = I_{Vs} - I_o$	Vs=13.5V, Io=150mA, WEn high		1.45	2.00	mA
	T _w	Thermal protection temperature		150		190	°C
	T _{w_hy}	Thermal protection temperature hysteresis			10		°C

Note: 1. see fig1 (behavior of output current versus regulated voltage Vo)

RESET

Pin	Symbol	Parameter	Test condition	min	typ	max	Unit
Res	V _{res_l}	Reset output low voltage	R _{ext} = 5kΩ to Vo, Vo > 1V			0.4	V
Res	I _{Res_lkg}	Reset output high leakage current	V _{Res} = 5V			1	μA
Res	R _{Res}	Internal Pull up resistance	versus Vo	10	20	40	kΩ
Res	V _{o_th}	Reset threshold voltage	Vs = 5.6 to 31V Io = 1 to 150mA	6%	8%	10%	below V _{o_ref}
Vcr	V _{rhth}	Reset timing low threshold	Vs = 13.5V	10%	13%	16%	V _{o_ref}
Vcr	V _{rlth}	Reset timing high threshold	Vs = 13.5V	44%	47%	50%	V _{o_ref}
Vcr	I _{cr}	Charge current	Vs = 13.5V	8	15	30	μA
Vcr	I _{dr}	Discharge current	Vs = 13.5V	8	15	30	μA
Res	t _{rr_2}	Reset reaction time (2)	Vo = V _{o_th} - 100mV	100	250	700	μs
Res	t _{rd}	Reset delay time	Vs = 13.5V, C _{tr} = 1nF	65	115	165	ms

2. When Vo becomes lower than 4V, the reset reaction time decreases down to 2 s assuring a faster reset condition in this particular case.

WATCHDOG

Pin	Symbol	Parameter	Test condition	min	typ	max	Unit
Wi	Vih	Input high voltage	Vs=13.5V	3.5			V
Wi	Vil	Input low voltage	Vs=13.5V			1.5	V
Wi	Vih	Input hysteresis	Vs=13.5V		500		mV
Wi	Rwi	Pull down resistor	Vs=13.5V	30	100	250	kΩ
Vcw	Vwhth	Low threshold	Vs=13.5V	10%	13%	16%	V _{o_ref}
Vcw	Vwlth	High threshold	Vs=13.5V	44%	47%	50%	V _{o_ref}
Vcw	Icwc	Charge current	Vs=13.5V, Vcw=0.1V	5	10	20	μA
Vcw	Icwd	Discharge current	Vs=13.5V, Vcw=2.5V	1.25	2.5	5	μA
Vcw	Twop	Watchdog period	Vs=13.5V, Ctw=47nF	20	40	80	ms
Res	twol	Watchdog output low time	Vs=13.5V, Ctw=47nF	4	8	16	ms

WEn

Pin	Symbol	Parameter	Test condition	min	typ	max	Unit
WEn	VWEn_low	WEn input low voltage				1	V
WEn	VWEn_high	WEn input high voltage		3			V
WEn	VWEn_hyst	WEn input hysteresis		600	920	1300	mV
WEn	RWEn	Pull down current	Vs=13.5V	1	2.5	5	μA

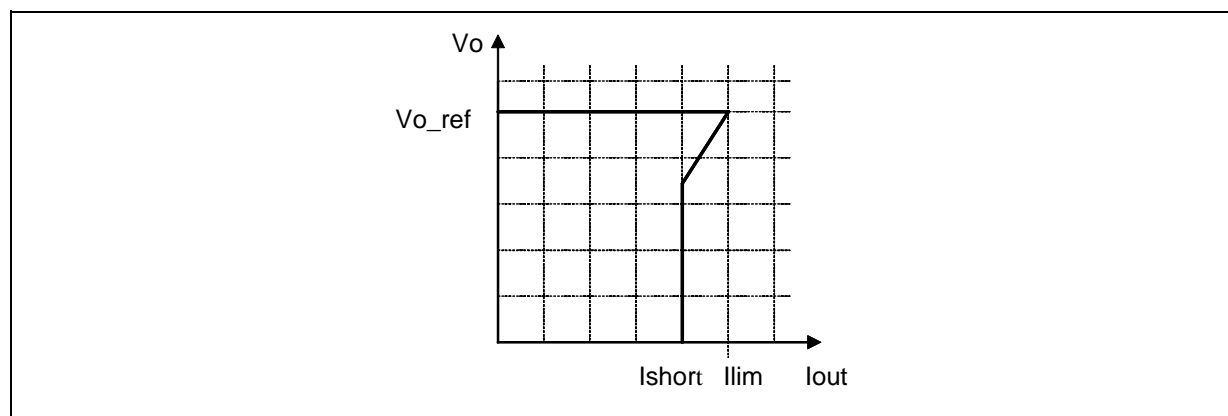
VOLTAGE REGULATOR

The voltage regulator uses a p-channel MOS transistor as a regulating element. With this structure a very low dropout voltage at current up to 150mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated.

The voltage Regulator is always active and not depending on the state of WEn input pin.

A short circuit protection to GND is provided.

Figure 1. Behavior of output current versus regulated voltage Vo



The reset circuit monitors the output voltage V_o . If the output voltage stays lower than V_{o_th} for filter time t_{rr} , then Res goes low. If the output voltage V_o becomes lower than 2.0V (typ) than Res goes immediately low. The reset low signal is guaranteed for an output voltage V_o greater than 1V.

When the output voltage goes back higher than V_{o_th} then Res goes high with a delay t_{rd} . This delay is obtained by 512 period of an oscillator. The oscillator period is given by:

$$T_{osc} = \frac{(V_{rhth} - V_{rlth}) \cdot C_{tr}}{I_{cr}} + \frac{(V_{rhth} - V_{rlth}) \cdot C_{tr}}{I_d}$$

t_{rd} is given by

$$t_{rd} = 512 \times T_{osc}$$

where:

$I_{cr} = 15\mu A$ is an internally generated charge current,

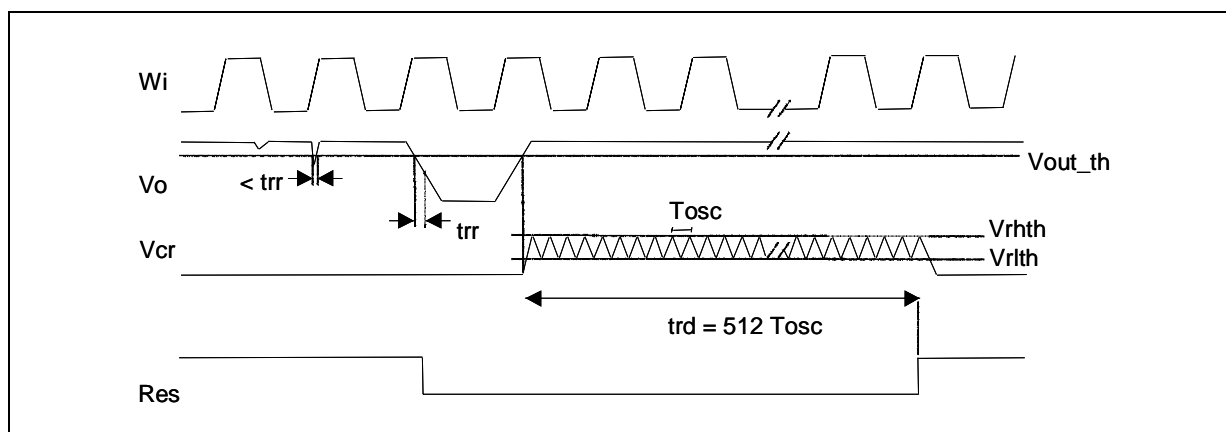
$I_{dr} = 15\mu A$ is an internally generated discharge current,

$V_{rhth} = 2.35V$ and $V_{rlth} = 0.65V$ are two typ thresholds,

C_{tr} is an external capacitance.

The Reset is always active and not depending on the state of WEn input pin.

Figure 2. Reset Time Diagram



Watchdog

The watchdog input Wi monitors a connected microcontroller. If pulses are missing, the Reset output Res is set to low. The pulse sequence time can be set within a wide range with the external capacitor C_{tw} . The watchdog circuit discharges the capacitor C_{tw} with the constant current I_{cwd} . If the lower threshold V_{wlth} is reached, a watchdog reset is generated.

To prevent this reset the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold V_{wlth} . In order to calculate the minimum time t_{dis} during which the microcontroller must output the positive edge the following equation can be used

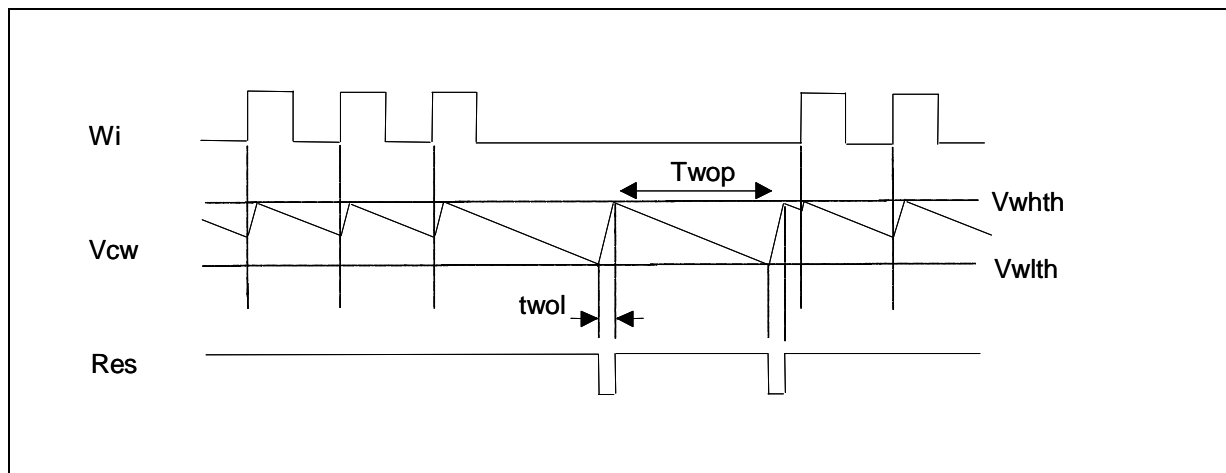
$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{cwd} \times t_{dis}$$

Every Wi positive edge switches the current source from discharging to charging, the same happens when the lower threshold is reached. When the voltage reaches the upper threshold V_{whth} the current switches from charging to discharging. The result is a saw tooth waveform at the watchdog timer capacitor C_{tw} .

The Watchdog operation is active only if WEn input pin is set to logic state high.



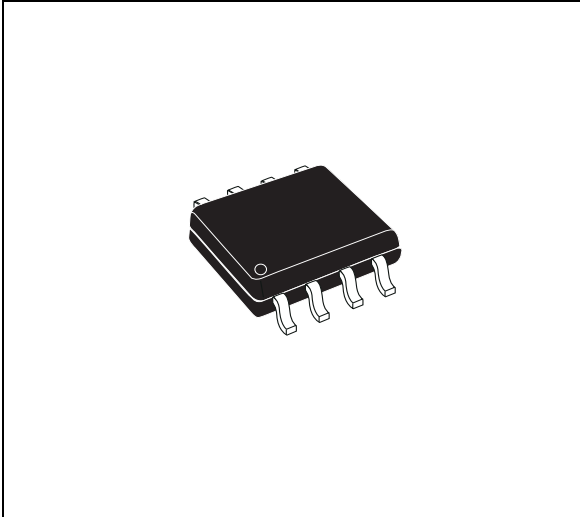
Figure 3. Watchdog time diagram



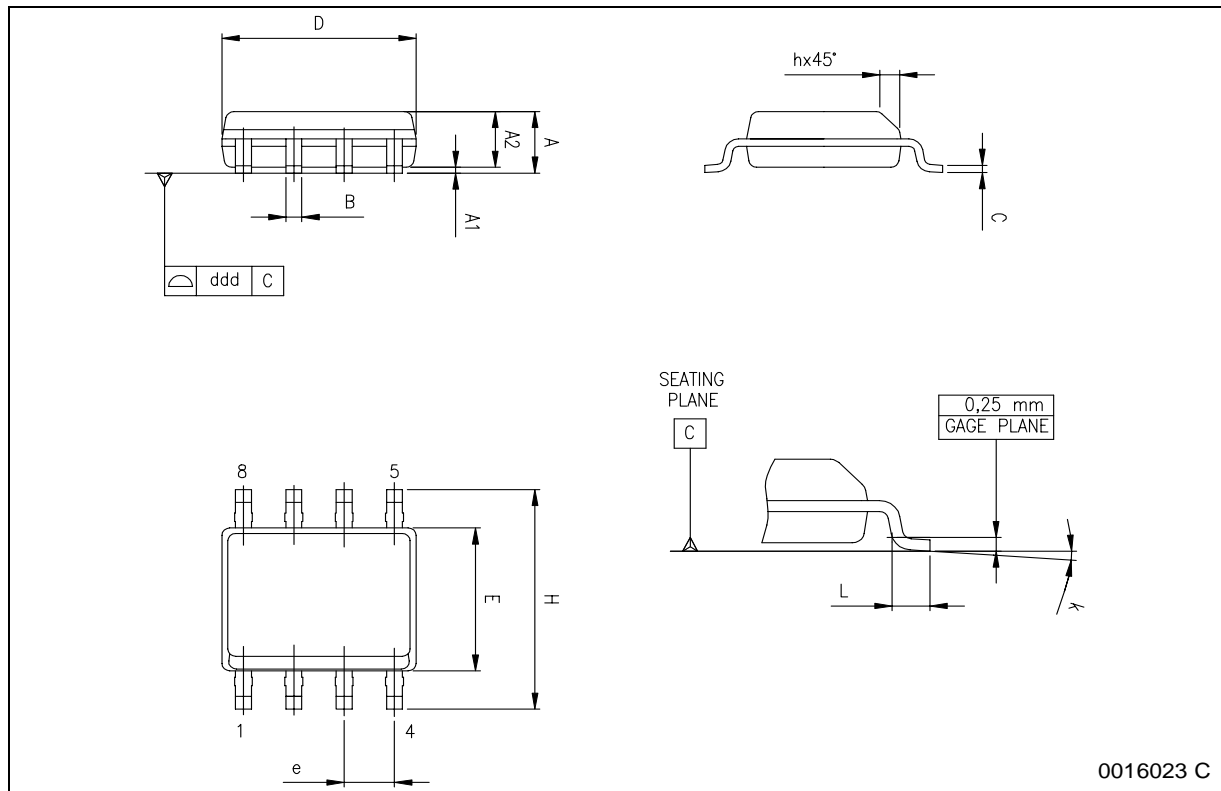
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

Note: (1) Dimensions D does not include mold flash, protrusions or gate burrs.
Mold flash, protrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

OUTLINE AND MECHANICAL DATA



SO-8



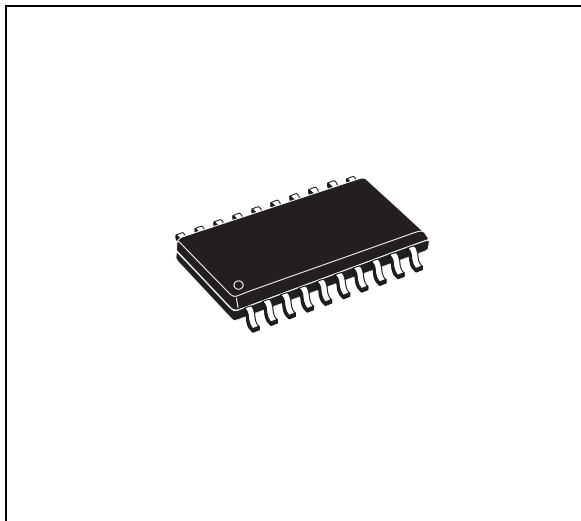
0016023 C



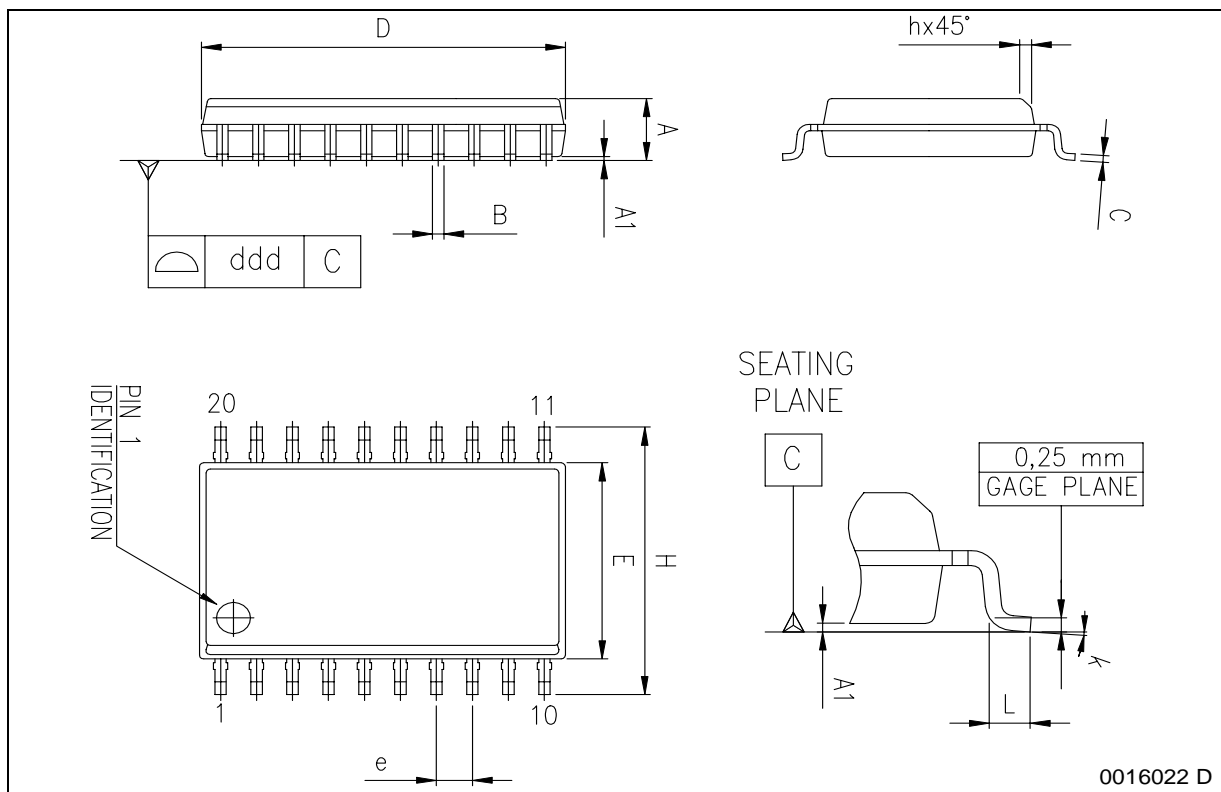
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO20



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