CX-6-SM CRYSTAL

800 kHz to 1.35 MHz

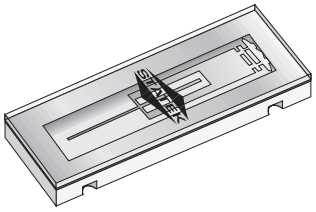
Ultra-Low Profile (1mm)
Miniature Surface Mount Quartz Crystal

DESCRIPTION

The CX-6-SM quartz crystals are leadless devices designed for surface mounting on printed circuit boards or hybrid substrates. They are hermetically sealed in a rugged, miniature ceramic package. They are manufactured using the STATEK-developed photolithographic process, and are designed utilizing the experience acquired by producing millions of crystals for industrial, commercial, military and medical applications. Maximum process temperature should not exceed 260°C.

FEATURES

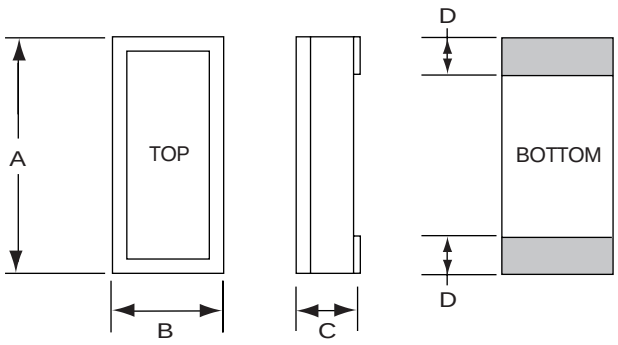
- Ultra-low profile (1mm)
- Extensional mode
- Ideal for use with microprocessors
- Designed for low power applications
- Low aging
- Full military testing available
- Ideal for battery operated applications
- Designed and manufactured in the USA



actual size

side view

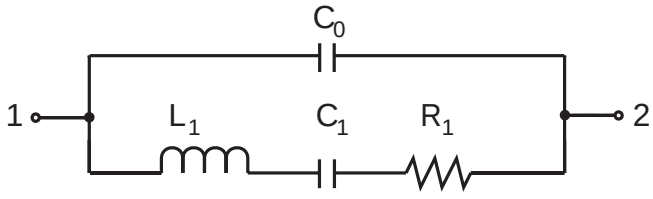
PACKAGE DIMENSIONS



	TYP.		MAX.	
DIM	INCHES	mm	INCHES	mm
A	.265	6.73	.280	7.11
B	.103	2.62	.114	2.90
C	-	-	see below	
D	.050	1.27	.060	1.52

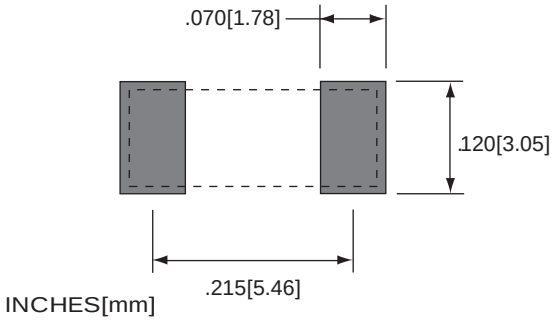
DIM "C"	GLASS LID		CERAMIC LID	
MAX	INCHES	mm	INCHES	mm
SM1	.039	0.99	.053	1.35
SM2	.041	1.04	.055	1.40
SM3	.044	1.12	.058	1.47

EQUIVALENT CIRCUIT



R_1 Motional Resistance L_1 Motional Inductance
C_1 Motional Capacitance C_0 Shunt Capacitance

SUGGESTED LAND PATTERN



INCHES[mm]

10133 - Rev A

SPECIFICATIONS

Specifications are typical at 25°C unless otherwise noted.
Specifications are subject to change without notice.

Frequency Range	800 kHz - 1.35 MHz
Functional Mode	Extensional
Calibration Tolerance*	A ± 0.05% (± 500ppm)
	B ± 0.1%
	C ± 1.0%
Load Capacitance	7 pF
Motional Resistance (R_1)	5 kΩ MAX
Motional Capacitance (C_1)	1.2fF
Quality Factor (Q)	150 k
Shunt Capacitance (C_0)	1.0 pF
Drive Level	3 μW MAX.
Turning Point (T_O)**	35°C
Temperature Coefficient (k)	-0.035 ppm/°C²
Note: Frequency (f) deviation from frequency (f_O) @ turning point temperature (T_O);	$\frac{f-f_O}{f_O} = k(T-T_O)^2$
Aging, first year	5ppm MAX.
Shock	1000g peak, 0.3 msec.,1/2 sine
Vibration, survival	10g rms, 20-1,000 Hz random
Operating Temperature	-10°C to +70°C Commercial
	-40°C to +85°C Industrial
	-55°C to +125°C Military
Storage Temperature	-55°C to +125°C
Max Process Temperature	260°C for 20 sec.

* Tighter frequency calibration available.
** Other turning point available.

PACKAGING

CX-6-SM - Tray Pack (Standard)

-16mm tape, 7" or 13" reels (Optional)
Per EIA 481 (see data sheet 10109)

TERMINATIONS

Designation	Termination
SM1	Gold Plated
SM2	Nickel, Solder Plated
SM3	Nickel, Solder Plated and Solder Dipped

HOW TO ORDER CX-6-SM CRYSTALS

CX-6 ____ -SM1 1.0 MHz (A / I)

- CX-6: "S" if special or custom design. Blank if Std.
- ____: Blank = Glass Lid; C=Ceramic Lid
- -SM1: SM1, SM2, SM3
- 1.0 MHz: Frequency
- (A): Calibration Tolerance* @ 25°C (A), (B), (C)
- / I): Temp. Range: C = Commercial, I = Industrial, M = Military, S = Specify

*Other calibration fill in ppm.

TYPICAL APPLICATION FOR A PIERCE OSCILLATOR

The low profile CX miniature surface mount crystal is ideal for small, high density, battery operated portable products. The CX crystal designed in a Pierce oscillator (single inverter) circuit provides very low current consumption and high stability. A conventional CMOS Pierce oscillator circuit is shown below. The crystal is effectively inductive and in a PI-network circuit with C_D and C_G provides the additional phase shift necessary to sustain oscillation. The oscillation frequency (f_O) is 15 to 150 ppm above the crystal's series resonant frequency (f_S).

Drive Level

R_A is used to limit the crystal's drive level by forming a voltage divider between R_A and C_D. R_A also stabilizes the oscillator against changes in the amplifiers output resistance (R_0). R_A should be increased for higher voltage operation.

Load Capacitance

The CX crystal calibration tolerance is influenced by the effective circuit capacitances, specified as the load capacitance (C_L). C_L is approximately equal to:

$$C_L = \frac{C_D \times C_G}{C_D + C_G} + C_S \qquad (1)$$

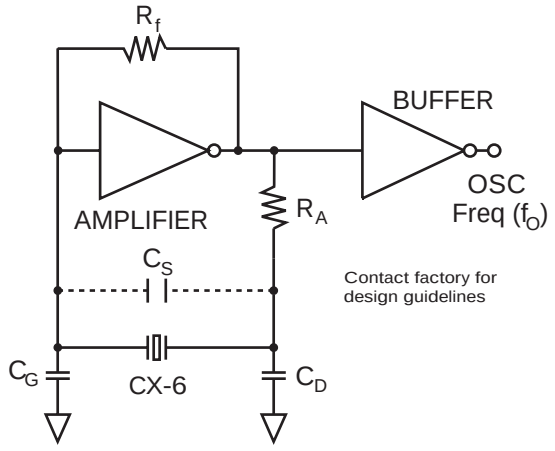
NOTE: C_D and C_G include stray layout to ground and C_S is the stray shunt capacitance between the crystal terminal. In practice, the effective value of C_L will be less than that calculated from C_D, C_G and C_S values because of the effect of the amplifier output resistance. C_S should be minimized.

The oscillation frequency (f_O) is approximately equal to:

$$f_O = f_S \left[1 + \frac{C_1}{2(C_0 + C_L)}\right] \qquad (2)$$

Where f_S = Series resonant frequency of the crystal
C_1 = Motional Capacitance
C_0 = Shunt Capacitance

CONVENTIONAL CMOS PIERCE OSCILLATOR CIRCUIT



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