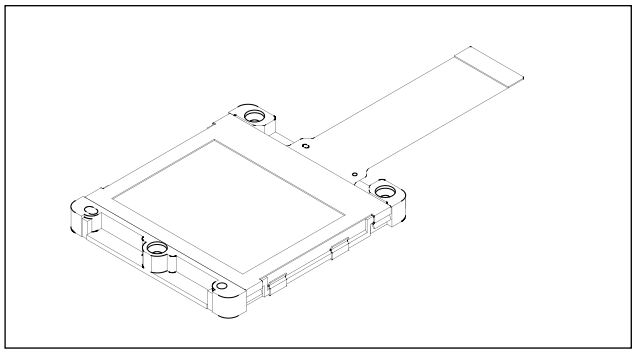
SONY

LCX028BLT

4.6cm (1.8-inch) Black-and-White LCD Panel



Description

The LCX028BLT is a 4.6cm diagonal active matrix TFT-LCD panel addressed by polycrystalline silicon super thin film transistors with a built-in peripheral driving circuit. Use of three LCX028BLT panels provides a full-color representation. The striped arrangement suitable for data projectors is capable of displaying fine text and vertical lines.

The adoption of an advanced on-chip black matrix realizes a high luminance screen. And cross talk free circuit and ghost free circuit contribute to high picture quality.

This panel has a polysilicon TFT high-speed scanner and built-in function to display images up/down and/or right/left inverse. The built-in 5V interface circuit leads to lower voltage of timing and control signals.

The panel contains an active area variable circuit which supports 4:3 and 16:9 data signals by changing the active area according to the type of input signal.

Features

- Number of active dots: 1,310,720 (1.8-inch, 4.6cm in diagonal)
- 4:3 and 16:9 aspect-ratio switching function
  4:3 (1280 (H) × 960 (V))
  16:9 (1280 (H) × 720 (V))
- High optical transmittance: 20% (typ.)
- Built-in cross talk free circuit and ghost free circuit
- High contrast ratio with normally white mode: 300 (typ.)
- Built-in H and V drivers (built-in input level conversion circuit, 5V driving possible)
- Up/down and/or right/left inverse display function
- Antidust glass package
- Microlens used

Element Structure

- Dots: 1280 (H) × 1024 (V) = 1,310,720
- Built-in peripheral driver using polycrystalline silicon super thin film transistors

Applications

- Liquid crystal data projectors
- Liquid crystal multimedia projectors
- Liquid crystal rear-projector TVs, etc.

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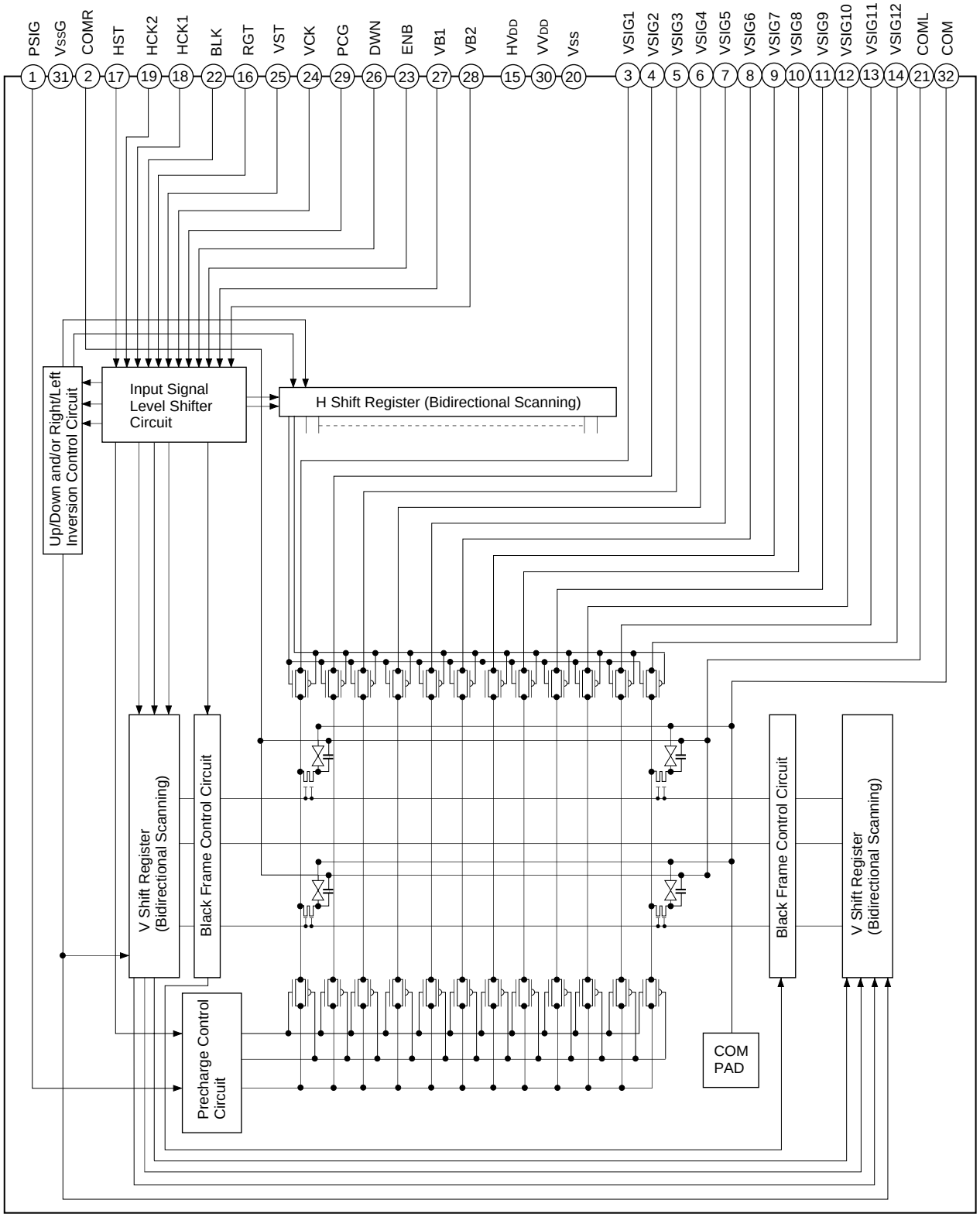
Block Diagram



Absolute Maximum Ratings (V_{SS} = 0V)

• H driver supply voltage	HV_{DD}	–1.0 to +20	V
• V driver supply voltage	VV_{DD}	–1.0 to +20	V
• Common pad voltage	COM, COML, COMR	–1.0 to +17	V
• H shift register input pin voltage	HST, HCK1, HCK2, RGT	–1.0 to +17	V
• V shift register input pin voltage	VST, VCK, PCG, BLK, ENB, DWN VB1, VB2	–1.0 to +17	V
• Video signal input pin voltage	SIG1 to 12, PSIG	–1.0 to +15	V
• Operating temperature*	Topr	–10 to +70	°C
• Storage temperature	Tstg	–30 to +85	°C

* Panel temperature inside the antidust glass

Operating Conditions (V_{SS} = 0V)

• Supply voltage

HV_{DD}	15.5 ± 0.5V
VV_{DD}	15.5 ± 0.5V

• Input pulse voltage (Vp-p of all input pins except video signal and uniformity improvement signal input pins)

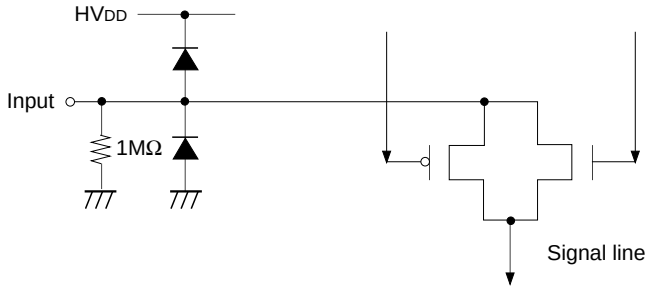
Pin Description

Pin No.	Symbol	Description
1	PSIG	Uniformity improvement signal
2	COMR	Voltage for right CS (storage capacity) electrode line
3	VSIG1	Video signal 1 to panel
4	VSIG2	Video signal 2 to panel
5	VSIG3	Video signal 3 to panel
6	VSIG4	Video signal 4 to panel
7	VSIG5	Video signal 5 to panel
8	VSIG6	Video signal 6 to panel
9	VSIG7	Video signal 7 to panel
10	VSIG8	Video signal 8 to panel
11	VSIG9	Video signal 9 to panel
12	VSIG10	Video signal 10 to panel
13	VSIG11	Video signal 11 to panel
14	VSIG12	Video signal 12 to panel
15	HV_{DD}	Power supply for H driver
16	RGT	Drive direction pulse for H shift register (H: nomal, L: reverse)
17	HST	Start pulse for H shift register drive
18	HCK1	Clock pulse for H shift register drive 1
19	HCK2	Clock pulse for H shift register drive 2
20	V_{SS}	GND (H, V drivers)
21	COML	Voltage for left CS (storage capacity) electrode line
22	BLK	Black Frame display pulse
23	ENB	Enable pulse for gate selection
24	VCK	Clock pulse for V shift register drive
25	VST	Start pulse for V shift register drive
26	DWN	Drive direction pulse for V shift register (H: nomal, L: reverse)
27	VB1	Display area switching 1
28	VB2	Display area switching 2
29	PCG	Improvement pulse for uniformity
30	VV_{DD}	Power supply for V driver
31	$V_{SS}G$	GND for V gate
32	COM	Common voltage of panel

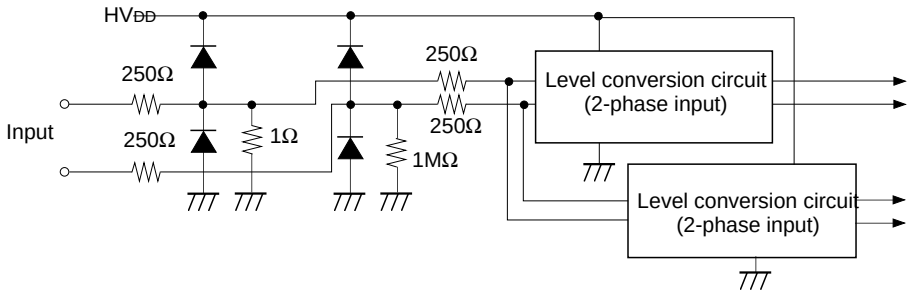
Input Equivalent Circuit

To prevent static charges, protective diodes are provided for each pin except the power supplies. In addition, protective resistors are added to all pins except the video signal inputs. All pins are connected to Vss with a high resistor of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (Resistance value: typ.)

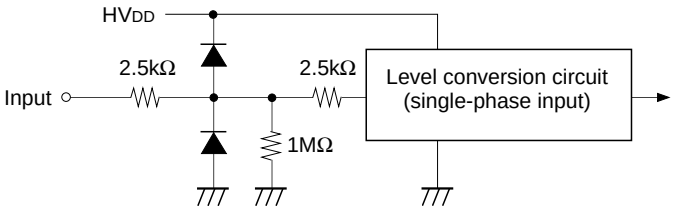
(1) VSIG1 to VSIG12, PSIG



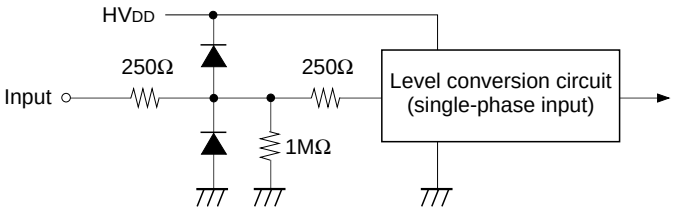
(2) HCK1,HCK2



(3) RGT

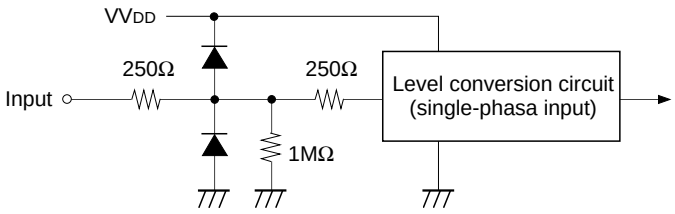


(4) HST

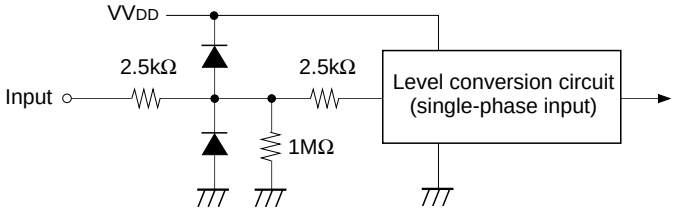


are all Vss

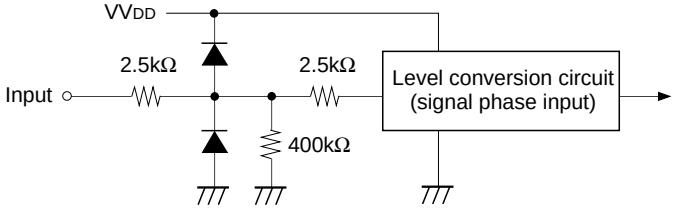
(5) PCG, VCK



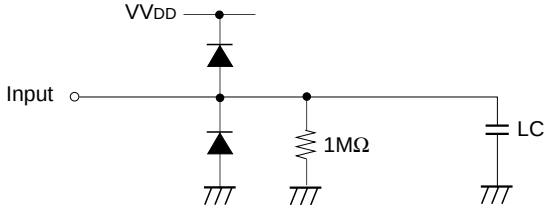
(6) VST,BLK,ENB,VB1,VB2



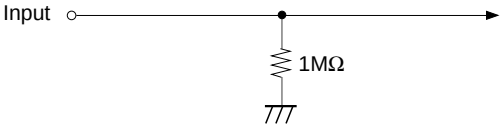
(7) DWN



(8) COM,COML,COMR



(9) HVDD, VSSG, VVDD



are all Vss

Input Signals

1. Input signal voltage conditions (V_{SS} = 0V)

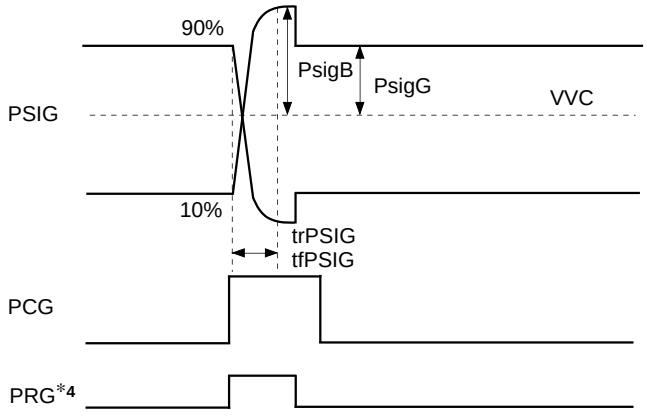
Item		Symbol	Min.	Typ.	Max.	Unit
H shift register input voltage HST, HCK1, HCK2, RGT	(Low)	VHIL	–0.5	0.0	0.4	V
	(High)	VHIH	4.5	5.0	5.5	V
V shift register input voltage VB1, VB2, BLK, VST, VCK, PCG, ENB, DWN	(Low)	VVIL	–0.5	0.0	0.4	V
	(High)	VVIH	4.5	5.0	5.5	V
Video signal center voltage		VVC	6.9	7.0	7.1	V
Video signal input range*1		Vsig	VVC – 4.5	7.0	VVC + 4.5	V
Common voltage of panel*2		Vcom	VVC – 0.6	VVC – 0.5	VVC – 0.4	V
Uniformity improvement signal input voltage (PSIG)*3		VpsigB	VVC ± 4.4	VVC ± 4.5	VVC ± 4.6	V
		VpsigG	VVC ± 1.7	VVC ± 1.8	VVC ± 1.9	

*1 Input video signal shall be symmetrical to VVC.

*2 The typical value of the common pad voltage may lower its suitable voltage according to the set construction to use. In this case, use the voltage of which has maximum contrast as typical value.
When the typical value is lowered, the maximum and minimum values may lower.

*3 Input a uniformity improvement signal PSIG in the same polarity with video signals VSIG1 to VSIG12 and which is symmetrical to VVC. PSIG wave form is 2 steps like below, in the upper chart, upper shows signal level of the 1st step, lower shows signal level of the 2nd step. Also, the rising and falling of PSIG are synchronized with the rising of PCG pulse, and the rise time trPSIG and fall time tfPSIG are suppressed within 400ns (as shown in a diagram below).

Input waveform of uniformity improvement signal PSIG



*4 PRG shows the time of the 1st step of PSIG signal, and it is not input to the panel.

Level Conversion Circuit

The LCX028BLT has a built-in level conversion circuit in the clock input unit on the panel. The input signal level increases to HV_{DD} or VV_{DD}. The V_{CC} of external ICs are applicable to 5 ± 0.5V.

2. Clock timing conditions (Ta = 25°C) (SXGA mode: fHckn = 4.5MHz, fVck = 32.0kHz, fv = 60Hz)

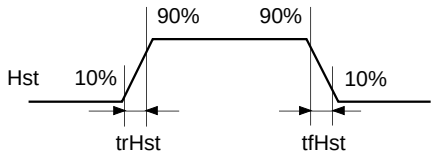
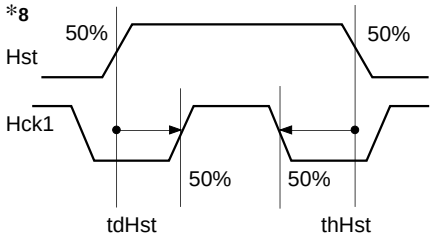
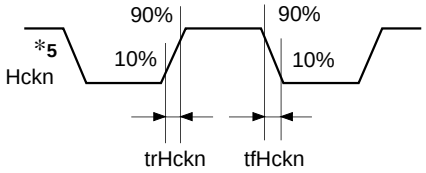
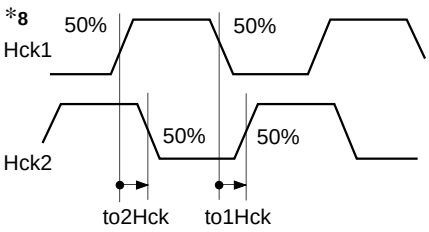
	Item	Symbol	Min.	Typ.	Max.	Unit
HST	Hst rise time	trHst	—	—	30	ns
	Hst fall time	tfHst	—	—	30	
	Hst data set-up time	tdHst	35	45	55	
	Hst data hold time	thHst	35	45	55	
HCK	Hckn rise time*5	trHckn	—	—	30	
	Hckn fall time*5	tfHckn	—	—	30	
	Hck1 fall to Hck2 rise time	to1Hck	–15	0	15	
	Hck1 rise to Hck2 fall time	to2Hck	–15	0	15	
VST	Vst rise time	trVst	—	—	100	
	Vst fall time	tfVst	—	—	100	
	Vst data set-up time	tdVst	2	6	10	µs
	Vst data hold time	thVst	2	6	10	
VCK	Vck rise time	trVck	—	—	100	ns
	Vck fall time	tfVck	—	—	100	
ENB	Enb rise time	trEnb	—	—	100	
	Enb fall time	tfEnb	—	—	100	
	Horizontal video period completed to Enb fall time	tdEnb	450*6	700	—	
	Enb rise to horizontal video period started	tuEnb	800	1100	—	
	Enb fall to Pcg rise time	toPcg	750	1000	—	
	Enb pulse width	twEnb	1800	—	—	
PCG	Pcg rise time	trPcg	—	—	30	
	Pcg fall time	tfPcg	—	—	30	
	Pcg rise to Vck rise/fall time	toVck	–100	0	100	
	Pcg fall to horizontal video period start time	toVideo	200	270	—	
	Pcg pulse width	twPcg	1600	1800	—	
PRG*4	PRG*4 rise to Pcg rise time	toPcgr	–10	0	10	
	PRG*4 fall to Pcg fall time	toPcgf	400	600	—	
	PRG*4 pulse width	twPRG*4	1100	1200	—	
BLK*5	Blk rise time	trBlk	—	—	100	
	Blk fall time	tfBlk	—	—	100	
	Blk rise to Enb fall time	toEnb	2	1	0	µs
	Blk fall to Pcg rise time	toPcg	–1	0	1	

*5 Hckn means Hck1 and Hck2.

*6 The minimum value of tdEnb is 450ns. When H-BLK has a long cycle and has some time to spare, take more time prior to other value.

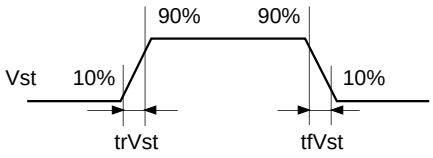
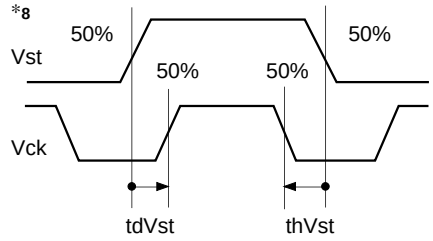
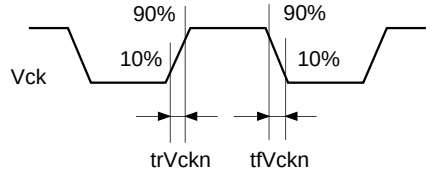
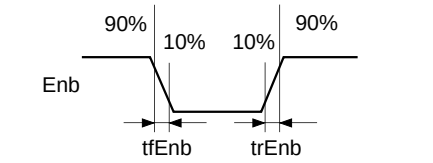
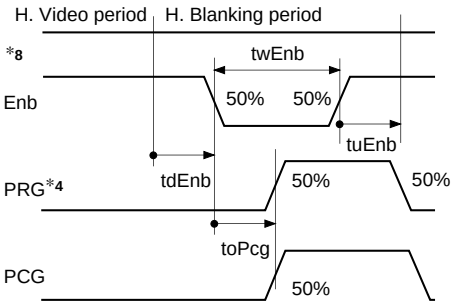
*7 Blk is the timing during 4:3 and 16:9 aspect-ratio mode, which keeps "H" level in other modes.

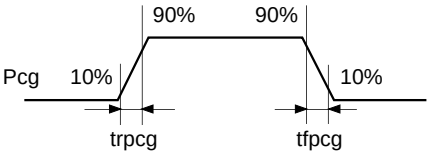
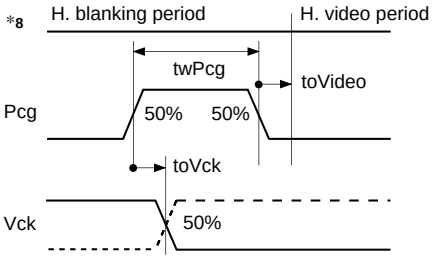
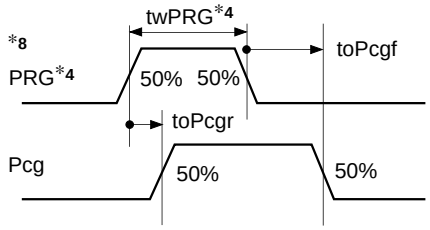
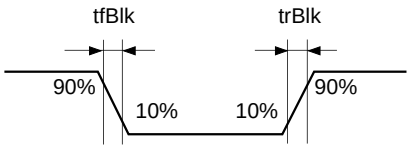
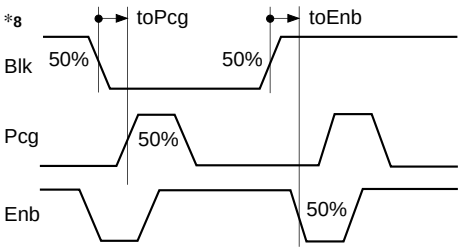
<Horizontal Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
HST	Hst rise time	trHst		• Hckn*5 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hst fall time	tfHst		
	Hst data set-up time	tdHst		• Hckn*5 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hst data hold time	thHst		
HCK	Hckn rise time*5	trHckn		• Hckn*5 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hckn fall time*5	tfHckn		
	Hck1 fall to Hck2 rise time	to1Hck		
	Hck1 rise to Hck2 fall time	to2Hck		

*8 Definitions: The right-pointing arrow (•→) means +.
The left-pointing arrow (←•) means –.
The black dot at an arrow (•) indicates the start of measurement.

<Vertical Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
VST	Vst rise time	trVst		
	Vst fall time	tfVst		
	Vst data set-up time	tdVst		
	Vst data hold time	thVst		
VCK	Vck rise time	trVck		
	Vck fall time	tfVck		
ENB	Enb rise time	trEnb		
	Enb fall time	tfEnb		
	Horizontal video period completed to Enb fall time	tdEnb		
	Enb rise to horizontal video period start time	tuEnb		
	Enb fall to Pcg rise time	toPcg		
	Enb pulse width	twEnb		

Item		Symbol	Waveform	Conditions
PCG*9	Pcg rise time	trPcg		
	Pcg fall time	tfPcg		
	Pcg rise to Vck rise/fall time	toVck		
	Pcg fall to horizontal video period start time	toVideo		
	Pcg pulse width	twPcg		
*9 PRG*4	PRG*4 rise to Pcg rise time	toPcgr		
	PRG*4 fall to Pcg fall time	toPcgf		
	PRG*4 pulse width	twPRG*4		
BLK	Blk rise time	trBlk		
	Blk fall time	tfBlk		
	Blk rise to Enb fall time	toEnb		
	Blk fall to Pcg rise time	toPcg		

*9 PCG input pin and PRG*4 should be "H" level during the horizontal 1H period, where the above BLK is low more than 10ns.

Electrical Characteristics (Ta = 25°C, HV_{DD} = 15.5V, VV_{DD} = 15.5V)

1. Horizontal drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Input pin capacitance	HCKn	CHckn	—	35	40	pF	
	HST	CHst	—	25	30	pF	
Input pin current	HCK1		–1000	–500	—	µA	HCK1 = GND
	HCK2		–1000	–500	—	µA	HCK2 = GND
	HST		–500	–190	—	µA	HST = GND
	RGT		–150	–40	—	µA	RGT = GND
Video signal input pin capacitance		Csig	—	200	250	pF	
Current consumption		IH	—	17.0	25.0	mA	HCKn: HCK1, HCK2 (4.5MHz)

2. Vertical drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Input pin capacitance	VCK	CVck	—	15	20	pF	
	VST	CVst	—	15	20	pF	
Input pin current	VCK,PCG		–500	–150	—	µA	VCK = GND, PCG = GND
VST, ENB, DWN, BLK, HB, VB			–150	–35	—	µA	VST, ENB, DWN,BLK, HB VB = GND
Current consumption		IV	—	4.0	6.0	mA	VCK: (32.0kHz)

3. Total power consumption of the panel

Item	Symbol	Min.	Typ.	Max.	Unit
Total power consumption of the panel	PWR	—	330	480	mW

4. Pin input resistance

Item	Symbol	Min.	Typ.	Max.	Unit
Pin – V_{SS} input resistance	Rpin	0.4	1	—	MΩ

5. Uniformity improvement signal

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance for uniformity improvement signal	CPSIGo	—	15	18	nF

6. COM pin capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
COM pin capacitance (COM, COML, COMR Total)	COM	—	25	30	nF

Electro-optical Characteristics (SXGA mode)

Item			Symbol	Measurement method	Min.	Typ.	Max.	Unit
Contrast ratio		25°C	CR	1	200	300	—	—
Optical transmittance		25°C	T	2	18	20	—	%
V-T characteristics	V_{90}	25°C	$RV_{90\text{-}25}$	3	0.9	1.3	1.6	V
			$GV_{90\text{-}25}$		1.0	1.4	1.7	
			$BV_{90\text{-}25}$		1.2	1.6	1.9	
		60°C	$RV_{90\text{-}60}$		0.9	1.3	1.6	
			$GV_{90\text{-}60}$		1.0	1.4	1.7	
			$BV_{90\text{-}60}$		1.1	1.5	1.8	
	V_{50}	25°C	$RV_{50\text{-}25}$		1.3	1.7	2.0	
			$GV_{50\text{-}25}$		1.4	1.8	2.1	
			$BV_{50\text{-}25}$		1.5	1.9	2.2	
		60°C	$RV_{50\text{-}60}$		1.2	1.6	1.9	
			$GV_{50\text{-}60}$		1.3	1.7	2.0	
			$BV_{50\text{-}60}$		1.4	1.8	2.1	
	V_{10}	25°C	$RV_{10\text{-}25}$		1.7	2.1	2.4	
			$GV_{10\text{-}25}$		1.8	2.2	2.5	
			$BV_{10\text{-}25}$		1.9	2.3	2.6	
		60°C	$RV_{10\text{-}60}$		1.7	2.1	2.4	
			$GV_{10\text{-}60}$		1.8	2.2	2.5	
			$BV_{10\text{-}60}$		1.8	2.2	2.5	
Response time	ON time	0°C	ton0	4	—	24.0	80.0	ms
		25°C	ton25		—	9.0	40.0	
	OFF time	0°C	toff0		—	99.0	200.0	
		25°C	toff25		—	27.0	70.0	
Flicker		60°C	F	5	—	–82.0	–40.0	dB
Image retention time		25°C	YT60	6	—	0	—	s
Cross talk		25°C	CTK	7	—	—	5	%

Reflection Preventive Processing

When a phase substrate which rotates the polarization axis is used to adjust to the polarization direction of a polarization screen or prism, use a phase substrate with reflection preventive processing on the surface. This prevents characteristic deterioration caused by luminous reflection.

<Electro-optical Characteristics Measurement>

Basic measurement conditions

(1) Driving voltage

HV_{DD} = 15.5V, VV_{DD} = 15.5V

VVC = 7.0V, Vcom = 6.5V

(2) Measurement temperature

25°C unless otherwise specified.

(3) Measurement point

One point in the center of the screen unless otherwise specified.

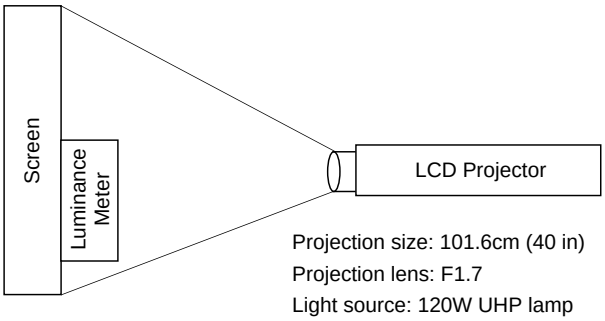
(4) Measurement systems

Two types of measurement systems are used as shown below.

(5) Video input signal voltage (Vsig)

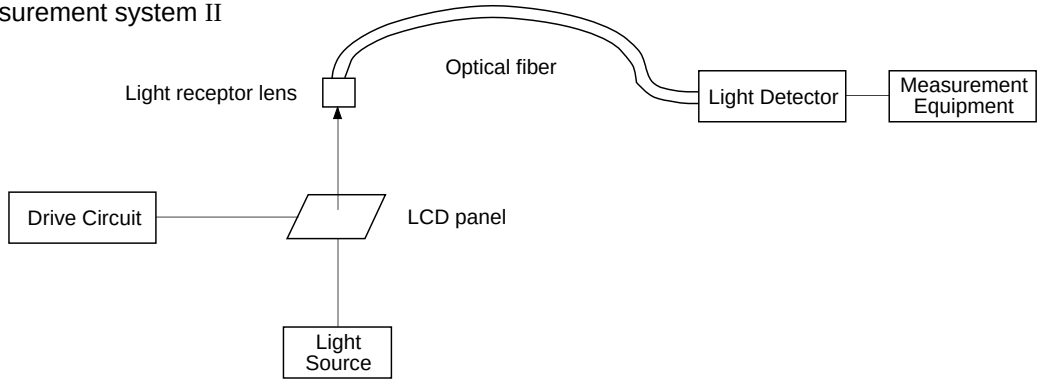
Vsig = 7.0 ± V_{AC} [V] (V_{AC} = signal amplitude)

• Measurement system I



Projection size: 101.6cm (40 in)
Projection lens: F1.7
Light source: 120W UHP lamp
Incidence illumination system: F#2.5
Polarzer: Side of incidence light-Polatechno's SHC-128U
Side of output light-Polatechno's SKN-18243

• Measurement system II



1. Contrast Ratio

Contrast Ratio (CR) is given by the following formula (1).

$$CR = \frac{L\ (White)}{L\ (Black)} \quad ... (1)$$

L (White): Surface luminance of the center of the screen at the input signal amplitude V_{AC} = 0.5V.

L (Black): Surface luminance of the center of the screen at V_{AC} = 4.5V.

Both luminosities are measured by System I.

2. Optical Transmittance

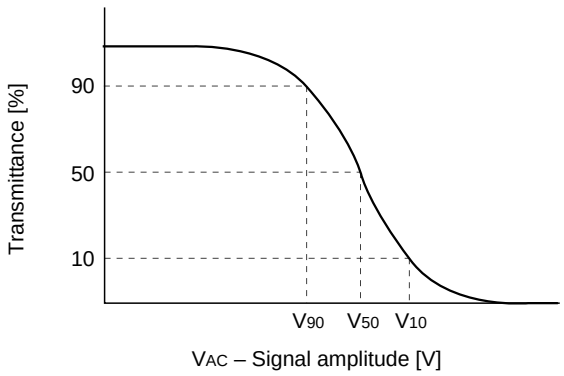
Optical Transmittance (T) is given by the following formula (2).

$$T = \frac{\text{White luminance}}{\text{Luminance of light source}} \times 100\ [\%] \ldots (2)$$

"White luminance" means the maximum luminance on the screen at the input signal amplitude V_{AC} = 0.5V on Measurement System I.

3. V-T Characteristics

V-T characteristics, or the relationship between signal amplitude and the transmittance of the panels, are measured by System II by inputting the same signal amplitude V_{AC} to each input pin. V_{90}, V_{50}, and V_{10} correspond to the voltages which define 90%, 50%, and 10% of transmittance respectively.



4. Response Time

Response time ton and toff are defined by formulas (5) and (6) respectively.

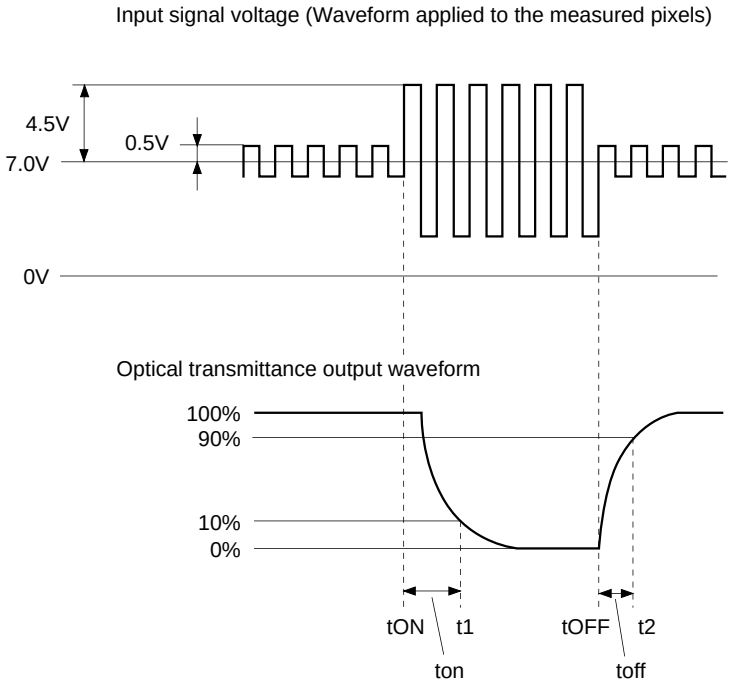
ton = t1 – tON ...(5)

toff = t2 – tOFF ...(6)

t1: time which gives 10% transmittance of the panel.

t2: time which gives 90% transmittance of the panel.

The relationships between t1, t2, tON and tOFF are shown in the right figure.



5. Flicker

Flicker (F) is given by formula (7). DC and AC (SXGA: 30Hz, rms) components of the panel output signal for gray raster* mode are measured by a DC voltmeter and a spectrum analyzer in System II.

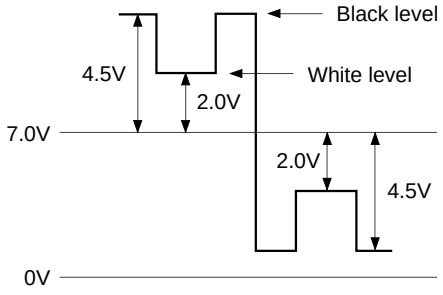
$$F\ [dB] = 20\log\left\{\frac{\text{AC component}}{\text{DC component}}\right\} \quad ...(7)$$

* Each input signal voltage for gray raster mode is given by Vsig = 7.0 ± V_{50} [V]
where: V_{50} is the signal amplitude which gives 50% of transmittance in V-T characteristics.

6. Image Retention Time

Apply the monoscope signal to the LCD panel for 60 minutes and then change this signal to the gray scale of Vsig = 7.0 ± V_{AC} (V_{AC}: 3 to 4V). Judging by sight at the V_{AC} that holds the maximum image retention, measure the time till the residual image becomes indistinct.

* Monoscope signal conditions:
Vsig = 7.0 ± 4.5 or ± 2.0 [V]
(shown in the right figure)
Vcom = 6.6V

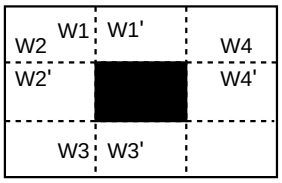


Vsig waveform

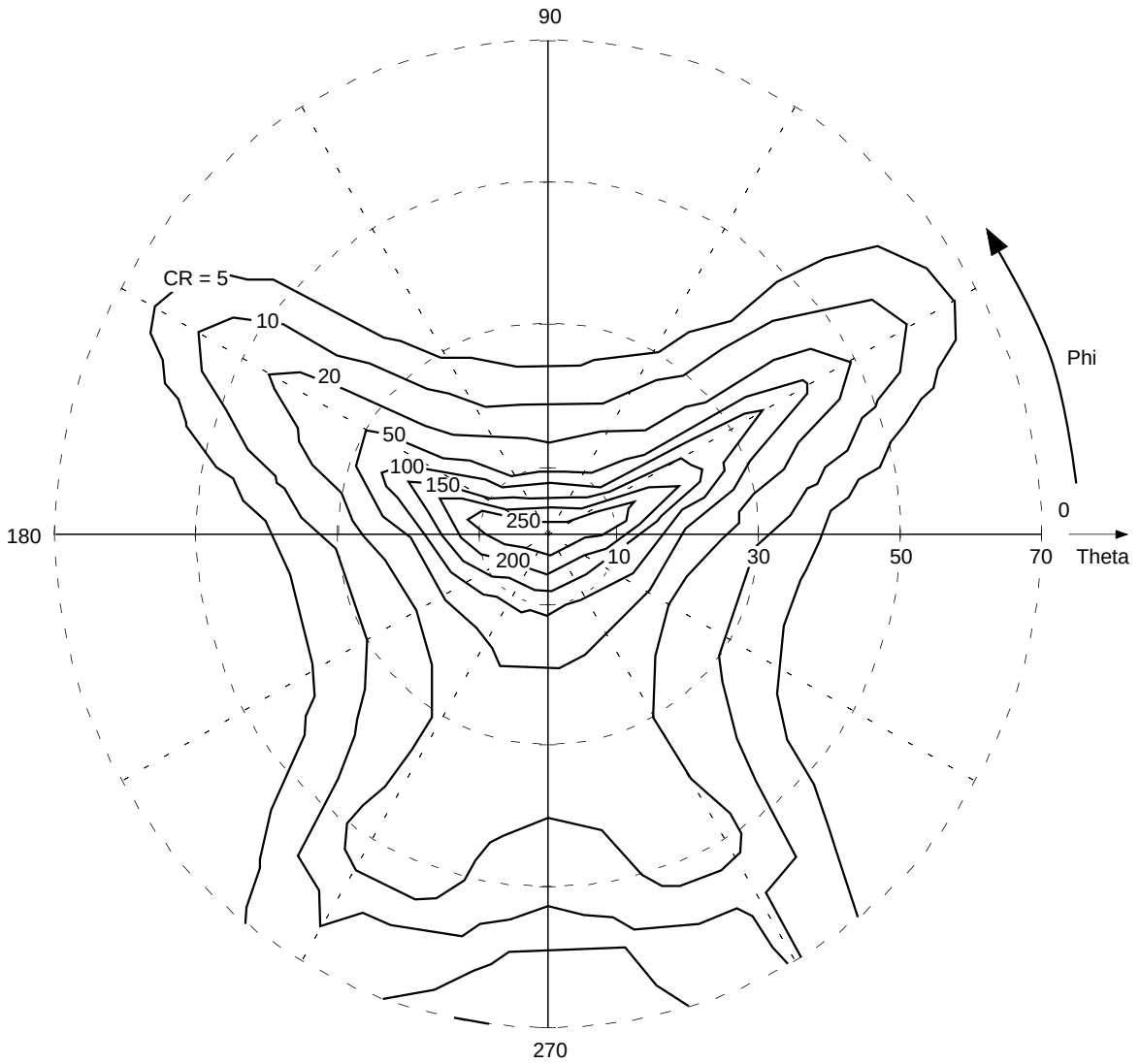
7. Cross Talk

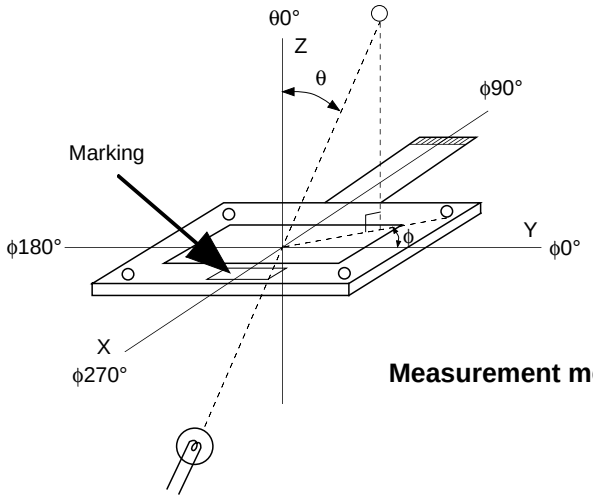
Cross talk is determined by the luminance differences between adjacent areas represented by Wi' and Wi (i = 1 to 4) around a black window (Vsig = 4.5 V/1V).

$$\text{Cross talk value CTK} = \left|\frac{Wi' - Wi}{Wi}\right| \times 100\ [\%]$$



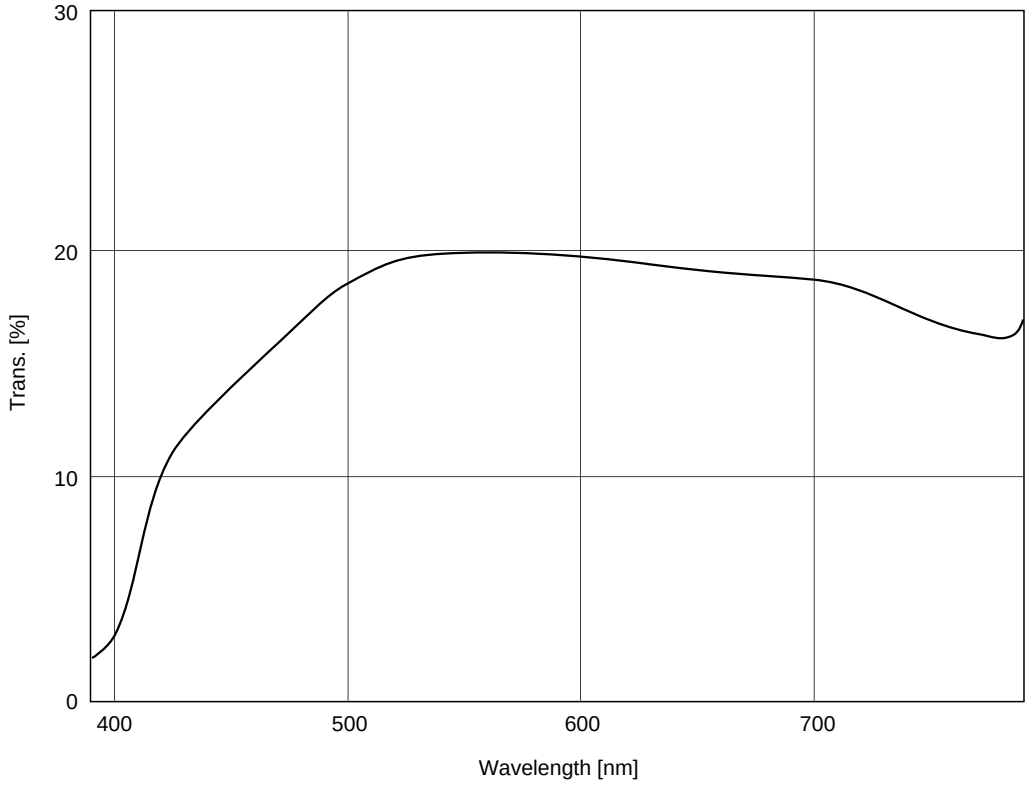
Viewing angle characteristics (without microlens)





Measurement method

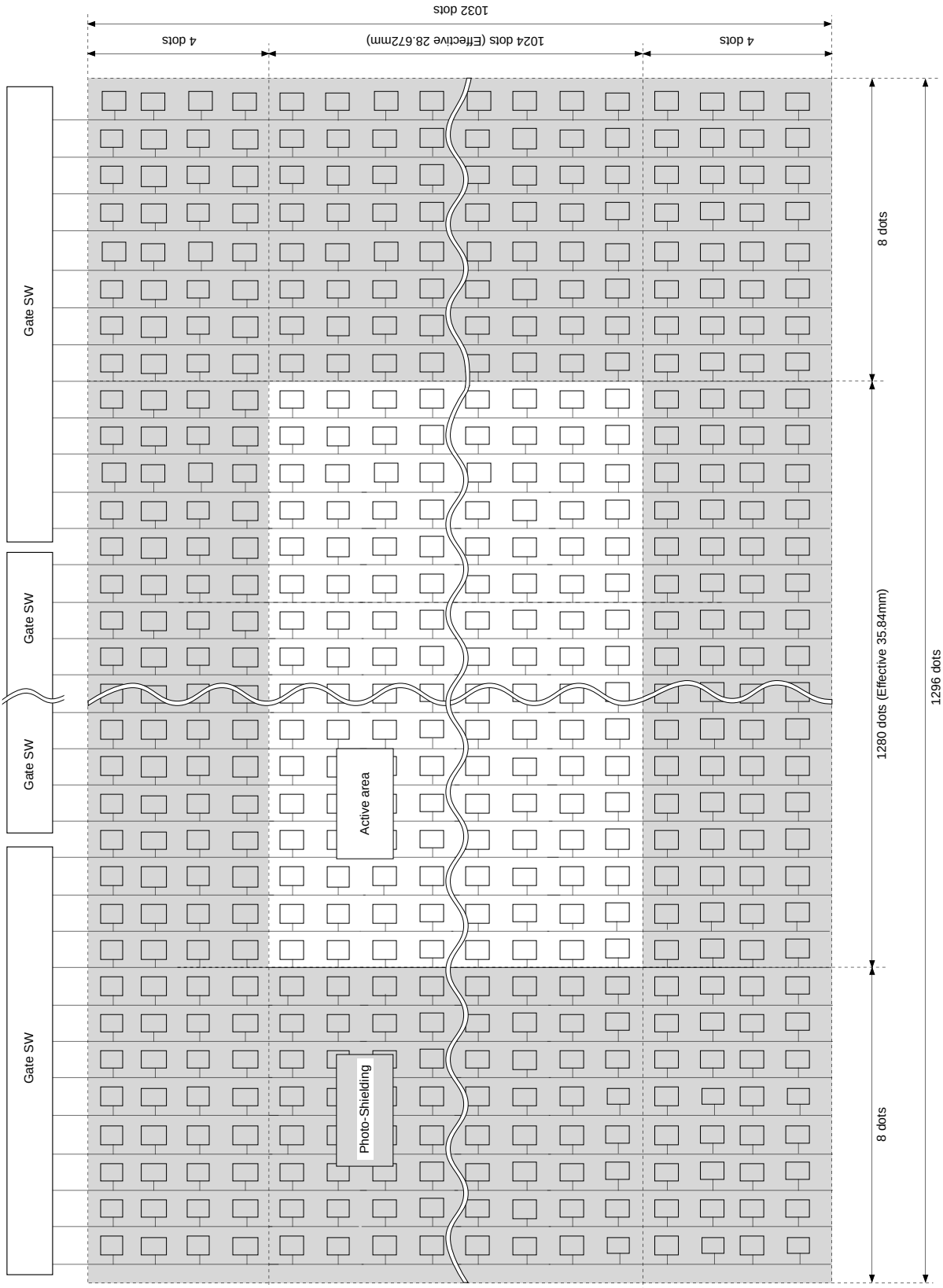
Optical transmittance of LCD panel (Typical Value)



Measurement method: Measurement system II

1. Dot Arrangement

The dots are arranged in a stripe. The shaded area is used for the dark border around the display.



2. LCD Panel Operations

[Description of basic operations]

- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to every 1024 gate lines sequentially in a single horizontal scanning period. (SXGA mode)

- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuits, applies selected pulses to every 1280 signal electrodes sequentially in a single horizontal scanning period. These pulses are used to supply the sampled video signal to the row signal lines.

- Vertical and horizontal shift registers address one pixel, and then Thin Film Transistors (TFTs; two TFTs) turn on to apply a video signal to the dot. The same procedures lead to the entire 1024 × 1280 dots to display a picture in a single vertical scanning period.

- The data and video signals shall be input with the 1H-inverted system.

[Description of operating mode]

This LCD panel can change the active area by displaying a black frame to support various computer or video signals. The active area is switched by VB1, VB2 and BLK. However, the center of the screen is not changed. The active area setting modes are shown below.

HB	VB	BLK	Screen aspect ratio
H	H	H	5:4 1280 × 1024
L	H	*1	4:3 1280 × 960
L	L	*1	16:9 1280 × 720

*1 Input BLK pulse (refer to drive waveform and vertical blanking period of black frame mode).

This LCD panel has the following functions to easily apply to various uses, as well as various broadcasting systems.

- Right/left inverse mode
- Up/down inverse mode

These modes are controlled by two signals (RGT and DWN). The right/left and/or up/down setting modes are shown below.

RGT	Mode
H	Right scan
L	Left scan

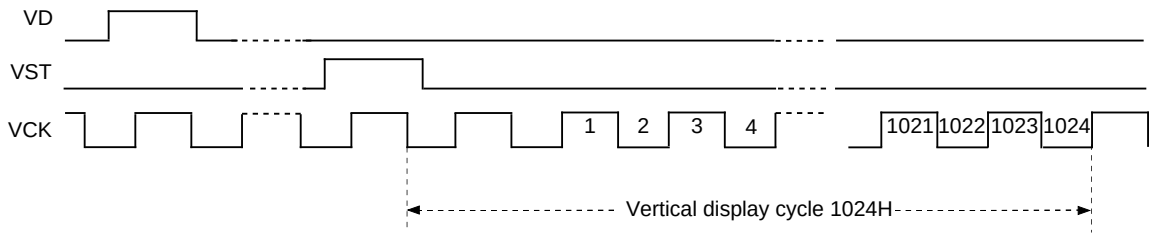
DWN	Mode
H	Down scan
L	Up scan

Right/left and/or up/down mean the direction when the Pin 1 marking is located at the right side with the pin block upside.

To locate the active area in the center of the panel in each mode, polarity of the start pulse and clock phase for both the H and V systems must be varied. The phase relationship between the start pulse and the clock for each mode is shown below.

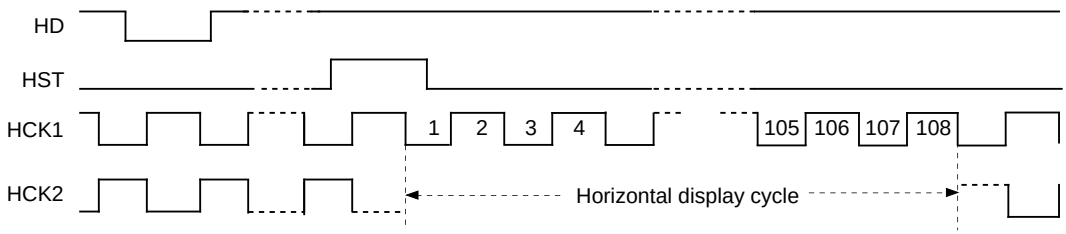
(1) Vertical direction display cycle (DWN = H, L)

(1.1) SXGA

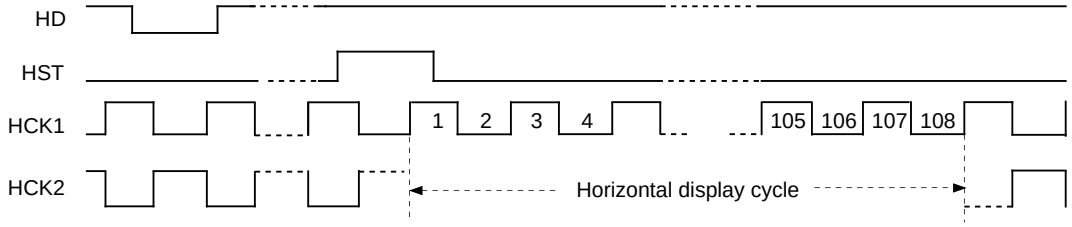


(2) Horizontal direction display cycle

(2.1.1) SXGA (RGT = H)

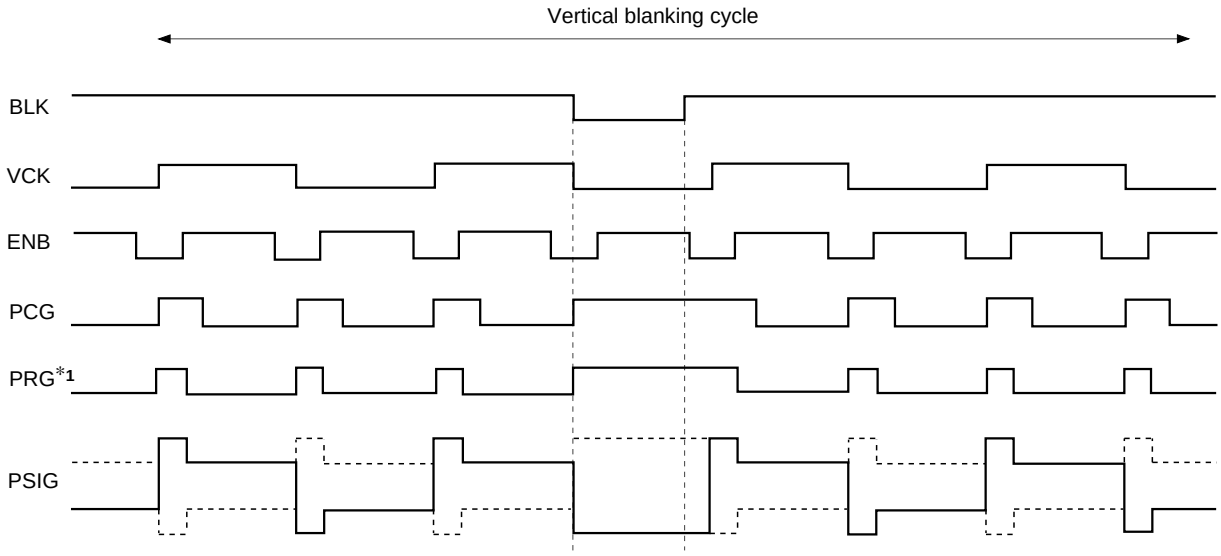


(2.1.2) SXGA (RGT = L)



(3) Vertical blanking cycle of black frame mode (4:3 and 16:9 display mode)

The input waveforms of PCG, PRG*1 and PSIG should be changed as shown below when BLK pulse is input.

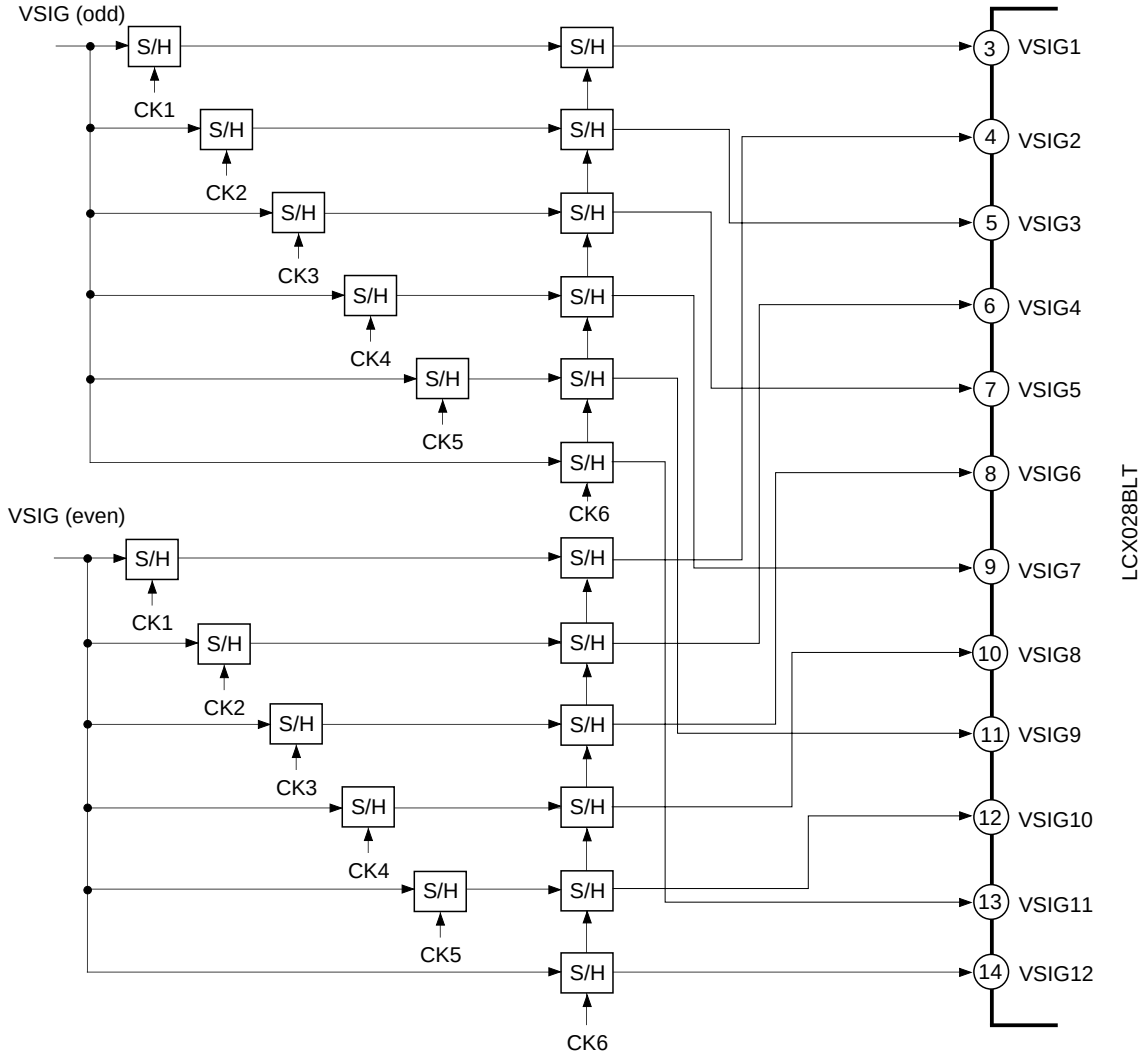


*1 PRG shows the period of PSIG black level, it is not input to the panel.

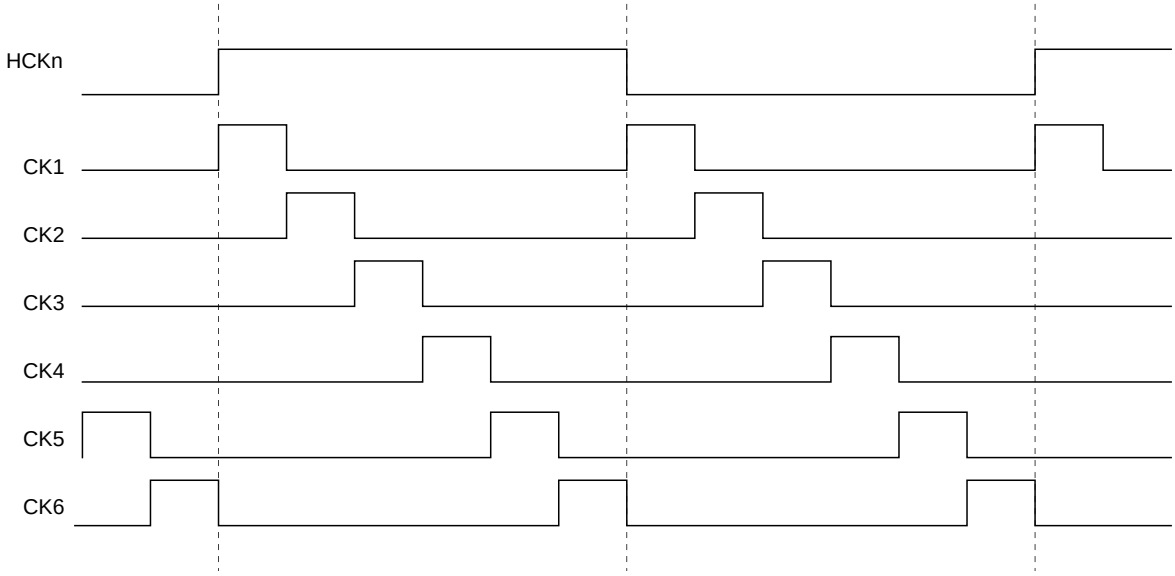
3. 12-dot Simultaneous Sampling

The horizontal shift register samples signals VSIG1 to VSIG12 simultaneously. This requires phase matching between signals VSIG1 to VSIG12 to prevent the horizontal resolution from deteriorating. Thus, phase matching between each signal is required using an external signal delaying circuit before applying the video signal to the LCD panel.

The block diagram of the delaying procedure using the sample-and-hold method is as follows. The following phase relationship diagram indicates the phase setting for right scan (RGT = High level). For left scan (RGT = Low level), the phase settings for signals VSIG1 to VSIG12 are exactly reversed.

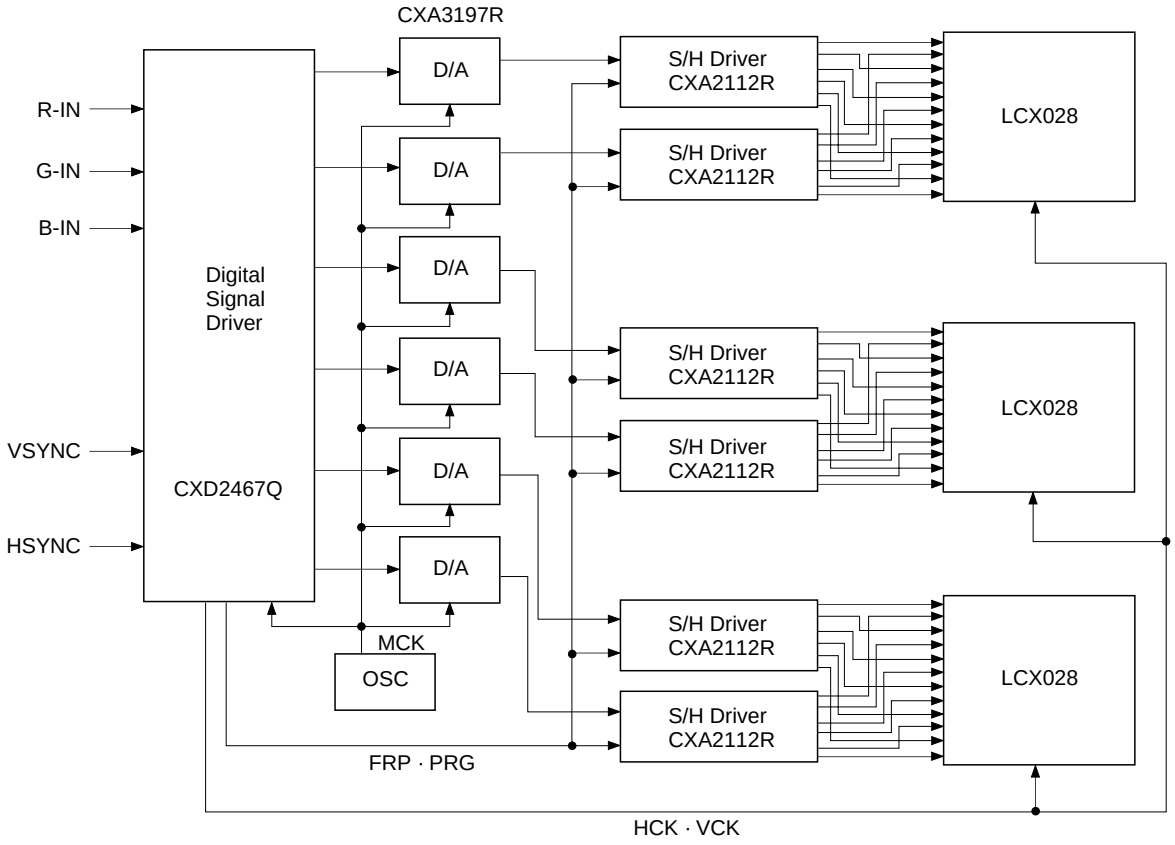


<Phase relationship of delaying sample-and-hold pulses> (right scan)



Display System Block Diagram

An example of display system is shown below.



Notes on Handling

(1) Static charge prevention

Be sure to take the following protective measures. TFT-LCD panels are easily damaged by static charges.

a) Use non-chargeable gloves, or simply use bare hands.
b) Use an earth-band when handling.
c) Do not touch any electrodes of a panel.
d) Wear non-chargeable clothes and conductive shoes.
e) Install conductive mats on the working floor and working table.
f) Keep panels away from any charged materials.
g) Use ionized air to discharge the panels.

(2) Protection from dust and dirt

a) Operate in a clean environment.
b) When delivered, the panel surface (glass panel) is covered by a protective sheet. Peel off the protective sheet carefully so as not to damage the glass panel.
c) Do not touch the glass panel surface. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave a stain on the surface.
d) Use ionized air to blow dust off the glass panel.

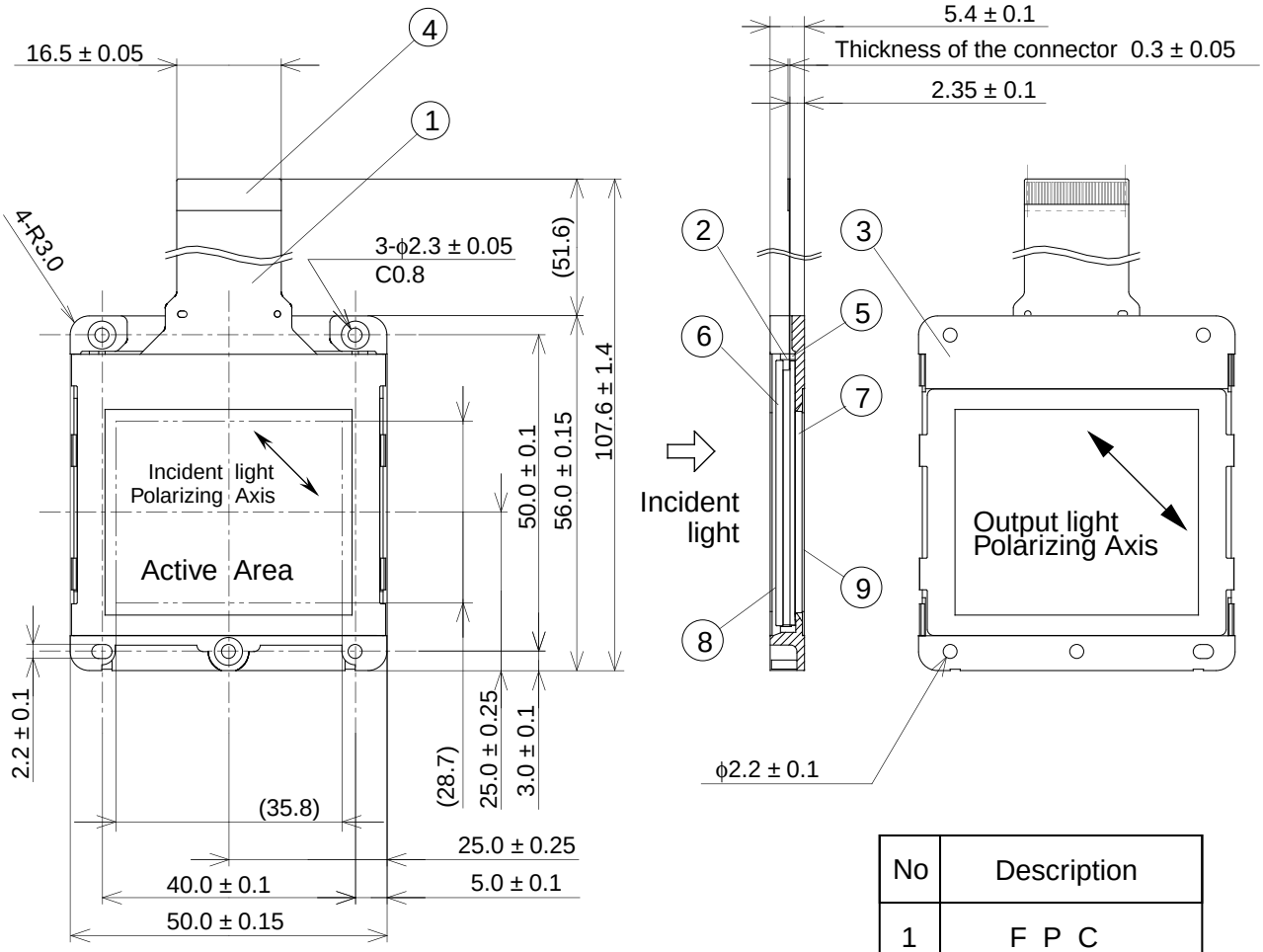
(3) Light resistance

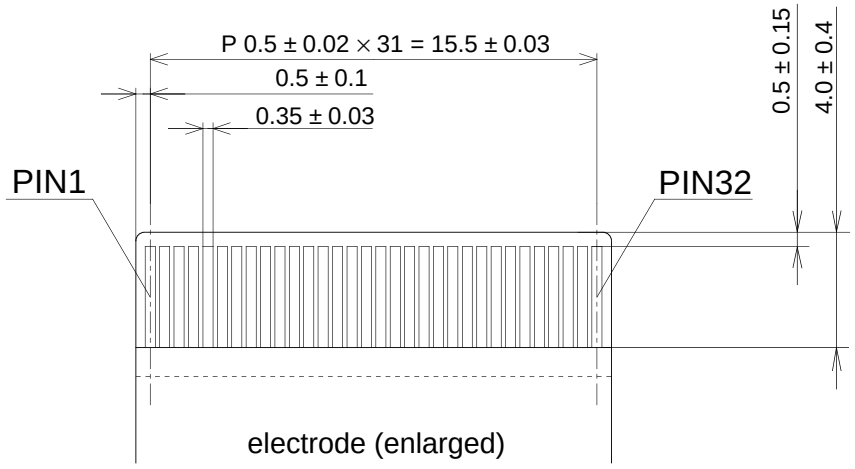
Orientation film and organic matter such as liquid crystal used inside of the LCD panel deteriorate by the light chemical reaction. As a result, its indication characteristic may irreversible change. The progress of its chemical reaction is influenced by short wavelength side's light (characteristics of UV cut filter) and temperature when quantitiy of light is constant. To control its progress, attach suitable UV cut filter between light source and LCD panel. (Sharp characteristic's filter of $\lambda > 425$nm is recommended.) Also, use suitable IR cut filter to lower the temperature of LCD panel and cool the panel carefully.

(4) Other handling precautions

a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
b) Do not drop the panel.
c) Do not twist or bend the panel or panel frame.
d) Keep the panel away from heat sources.
e) Do not dampen the panel with water or other solvents.
f) Avoid storing or using the panel at a high temperature or high humidity, which may result in panel damages.
g) Minimum radius of bending curvature for a flexible substrate must be 1mm.
h) Torque required to tighten screws on a panel must be 0.294N·m or less.
i) Do not pressure the portion other than mounting hole (cover).

Package Outline Unit: mm





No	Description
1	F P C
2	Molding material
3	Outside frame
4	Reinforcing board
5	Reinforcing material
6	Glass 1
7	Glass 2
8	Cover 1
9	Cover 2

The rotation angle of the active area relative to H and V is ± 1˚.

Mass 25g