SONY

CXG1150ER

Triple Low Noise Amplifier/Dual Mixer

Description

The CXG1150ER is a triple low noise amplifier/dual mixer MMIC, which has made through the Sony's GaAs J-FET process.

Features

- 3V single power supply operation
- 3-pin control by the on-chip logic circuit
- High gain: Gp = 16.5dB (LNA typ.)
  Gc = 10dB (MIX typ.)
- Low noise figure: NF = 1.1 to 1.9dB (LNA typ.)
  NF = 4.5dB (MIX typ.)
- Low LO input power operation: P_{LO} = –15dBm
- 24-pin VQFN small package

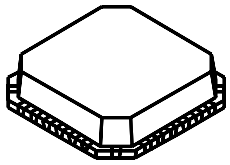
Applications

800MHz/1.5GHz Japan digital cellular phones (PDC)

Structure

GaAs J-FET MMIC

24 pin VQFN (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	4.5	V
• Input power	P_{IN}	+13	dBm
• Current consumption	I_{DD}	15	mA
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

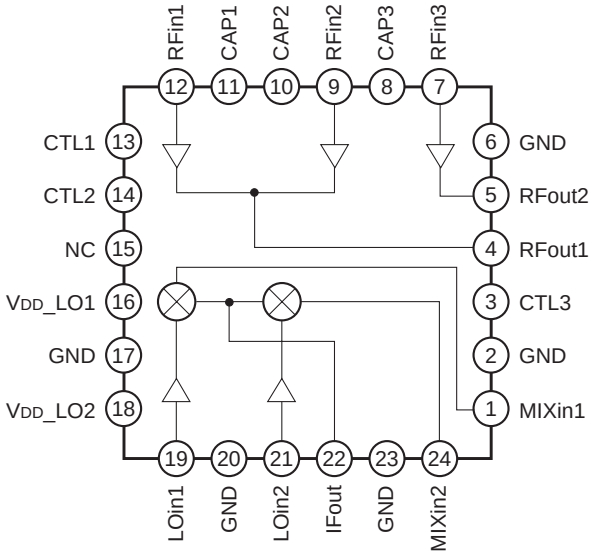
Recommended Operating Conditions

• Supply voltage	V_{DD}	2.7 to 3.3	V
• Control voltage	V_{CTL} (H)	2.4 to 3.3	V
	V_{CTL} (L)	0 to 0.5	V

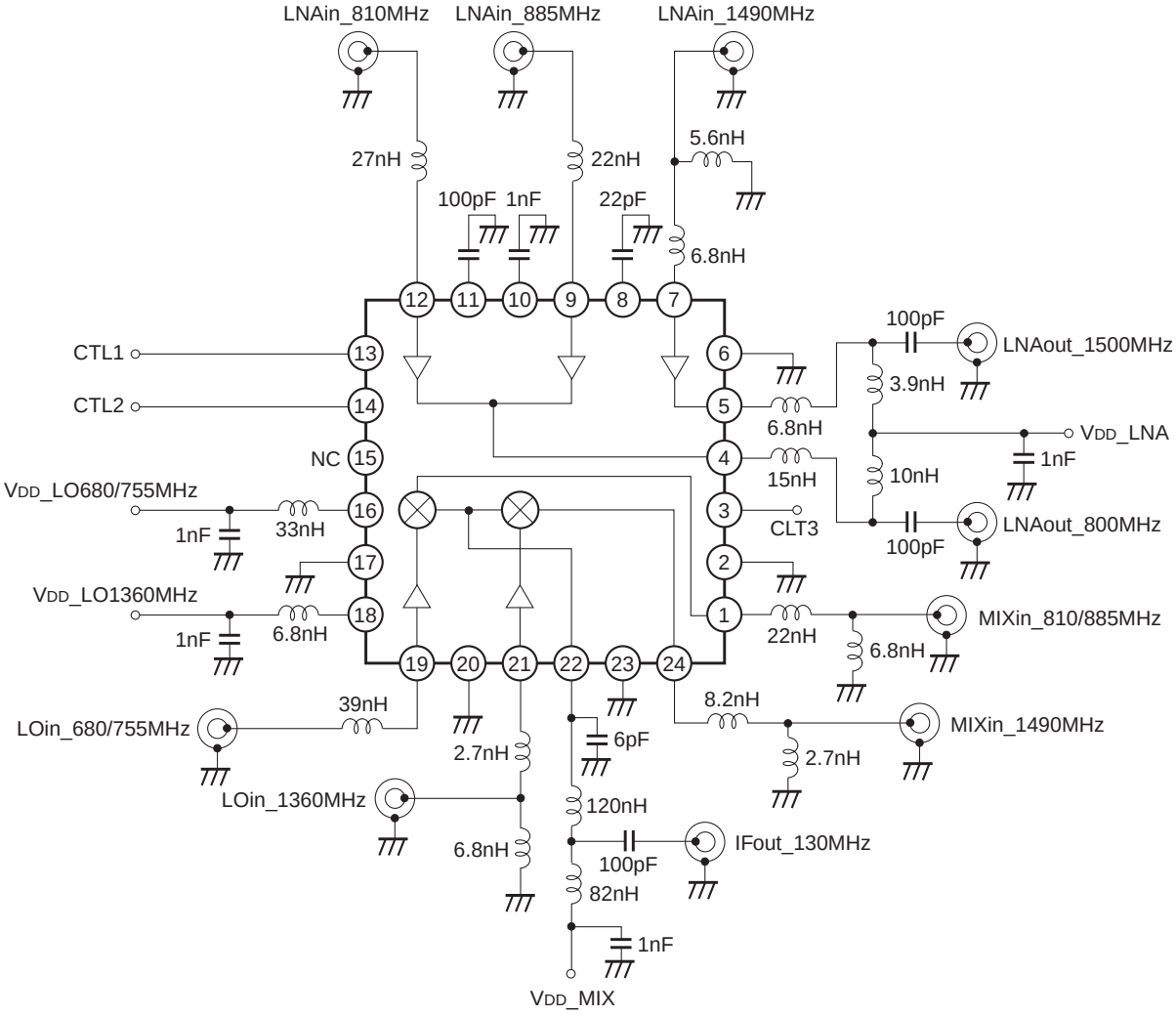
GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

E03114-PS

Block Diagram and Pin Configuration



Recommended Evaluation Circuit



Information for the evaluation circuit and components

The IF block is the evaluation circuit matching with 50Ω.
If the inductors with high Q value are not used in the IF block, gain might be dropped about 1dB.
In a recommended evaluation circuit board, the LK1608 series inductors made by "TAIYO YUDEN" are adopted, and in this board, the components of 1005 size are used except for the inductors in the above IF block.
When the matching of the IF block is changed to high impedance, operation might be unstable when the value of the capacitance (6pF) nearest from Pin 22 is drastically changed.

Operating Logic

$V_{CTL}1$	$V_{CTL}2$	$V_{CTL}3$	LNA1 (800MHz_D)	LNA2 (800MHz_T)	LNA3 (1.5GHz)	MIX1 (800MHz)	MIX2 (1.5GHz)
L	L	H	ON			ON	
L	L	L		ON		ON	
H	L	—		ON		ON	
—	H	—			ON		ON

(Blank is OFF)

Electrical Characteristics

The normalized values are those when the Sony's recommended evaluation board and components are used.

800MHz_TDMA Band Low Noise Amplifier (Pin 9 Input →Pin 4 Output)

Conditions: Unless otherwise specified, V_{DD} = 2.8V, V_{CTL} (H) = 2.8V, V_{CTL} (L) = 0V, $f_{RF}1$ = 810MHz, $f_{RF}2$ = 885MHz

(Ta = 25°C)

Item	Symbol	Path	Frequency	$V_{CTL}1$	$V_{CTL}2$	$V_{CTL}3$	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I_{DD}	—	—	L	L	L	—	2.9	4.0	mA	When no signal
			—	—	H	—	—	0	0.1		
Control current	I_{CTL}	—	—	L	L	L	—	0	5	µA	
			—	H	L	L	—	43	69		
			—	H	L	H	—	86	138		
Power gain	Gp	$RF_{IN}2$ →$RF_{OUT}1$	$f_{RF}1$	L	L	L	15.2	17	18.8	dB	When a small signal
				—	H	—	—	–22	–18		
			$f_{RF}2$	L	L	L	14.5	16	17.8		
				—	H	—	—	–21	–18		
Noise figure	NF	$RF_{IN}2$ →$RF_{OUT}1$	$f_{RF}1$	L	L	L	—	1.6	2.0	dB	
			$f_{RF}2$	L	L	L	—	1.5	1.9		
Input IP3	IIP3	$RF_{IN}2$ →$RF_{OUT}1$	$f_{RF}1$	L	L	L	–7	–4	—	dBm	*1
			$f_{RF}2$	L	L	L	–7	–3	—		
Isolation	I_{SO}	$RF_{OUT}1$ →$RF_{IN}2$	680MHz	L	L	L	25	30	—	dB	When a small signal
			755MHz	L	L	L	23	28	—		
Input reflection	VSWR	$RF_{IN}2$	$f_{RF}1$	L	L	L	—	2.4	3.2	—	*2
			$f_{RF}2$	L	L	L	—	1.8	2.2		
		$RF_{OUT}1$	$f_{RF}1$	L	L	L	—	1.7	2.2		
			$f_{RF}2$	L	L	L	—	1.8	2.2		

Besides the above logical condition, when $V_{CTL}1$ = H, $V_{CTL}2$ = L, $V_{CTL}3$ = L/H, the Path "$RF_{IN}2$ →$RF_{OUT}1$" turns on and the electrical characteristics at this time are same as the "ON" condition in the above table.

*1 Conversion from the IM3 suppression ratio for two-wave input: f_{RF}offset = 100kHz, P_{RF} = –30dBm.

*2 Input reflection is the value on the edge of IC and at the measurement power –30dBm.

800MHz_D Band Low Noise Amplifier (Pin 12 Input →Pin 4 Output)

Conditions: Unless otherwise specified, V_{DD} = 2.8V, V_{CTL} (H) = 2.8V, V_{CTL} (L) = 0V, $f_{RF}1$ = 810MHz, $f_{RF}4$ = 828MHz (Ta = 25°C)

Item	Symbol	Path	Frequency	$V_{CTL}1$	$V_{CTL}2$	$V_{CTL}3$	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I_{DD}	—	—	L	L	H	—	2	2.8	mA	When no signal
			—	—	H	—	—	0	0.1		
Control current	I_{CTL}	—	—	L	L	H	—	43	69	µA	
Power gain	Gp	$RF_{IN}1$ →$RF_{OUT}1$	$f_{RF}1$	L	L	H	15.2	17	18.8	dB	When a small signal
				—	H	—	—	–24	–20		
			$f_{RF}4$	L	L	H	14.5	16.3	18.1		
				—	H	—	—	–23	–20		
Noise figure	NF	$RF_{IN}1$ →$RF_{OUT}1$	$f_{RF}1$	L	L	H	—	1.6	2.0	dB	
			$f_{RF}4$	L	L	H	—	1.5	1.9		
Input IP3	IIP3	$RF_{IN}1$ →$RF_{OUT}1$	$f_{RF}1$	L	L	H	–10	–7	—	dBm	*1
			$f_{RF}4$	L	L	H	–10	–7	—		
Isolation	I_{SO}	$RF_{OUT}1$ →$RF_{IN}1$	680MHz	L	L	H	26	30	—	dB	When a small signal
			698MHz	L	L	H	25	29	—		
Gain difference from TDMA band	ΔGp	—	—	—	—	—	–0.7	0	+0.7	dB	Same frequency
Input reflection	VSWR	$RF_{IN}1$	$f_{RF}1$	L	L	H	—	2.4	3.2	—	*2
			$f_{RF}4$	L	L	H	—	2.1	2.6		
		$RF_{OUT}1$	$f_{RF}1$	L	L	H	—	2.0	2.4		
			$f_{RF}4$	L	L	H	—	1.9	2.3		

*1 Conversion from the IM3 suppression ratio for two-wave input: f_{RF}offset = 100kHz, P_{RF} = –30dBm.

*2 Input reflection is the value on the edge of IC and at the measurement power –30dBm.

1.5GHz Band Low Noise Amplifier

Conditions: Unless otherwise specified, V_{DD} = 2.8V, V_{CTL} (H) = 2.8V, V_{CTL} (L) = 0V, $f_{RF}3$ = 1490MHz

(Ta = 25°C)

Item	Symbol	Path	Frequency	$V_{CTL}1$	$V_{CTL}2$	$V_{CTL}3$	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I_{DD}	—	—	—	H	—	—	2.9	4.0	mA	When no signal
Control current	I_{CTL}	—	—	L	H	L	—	43	69	µA	
Power gain	Gp	$RF_{IN}3 \rightarrow RF_{OUT}2$	$f_{RF}3$	—	H	—	14.5	16	17.8	dB	When a small signal
Noise figure	NF	$RF_{IN}3 \rightarrow RF_{OUT}2$	$f_{RF}3$	—	H	—	—	1.5	1.9	dB	
Input IP3	IIP3	$RF_{IN}3 \rightarrow RF_{OUT}2$	$f_{RF}3$	—	H	—	–7	–4	—	dBm	*1
Isolation	I_{SO}	$RF_{OUT}2 \rightarrow RF_{IN}3$	1371MHz	—	H	—	17.5	20.5	—	dB	When a small signal
Input reflection	VSWR	$RF_{IN}2$	$f_{RF}3$	—	H	—	—	2.0	2.5	—	*2
		$RF_{OUT}1$	$f_{RF}3$	—	H	—	—	1.8	2.3		

*1 Conversion from the IM3 suppression ratio for two-wave input: f_{RF}offset = 100kHz, P_{RF} = –30dBm.

*2 Input reflection is the value on the edge of IC and at the measurement power –30dBm.

800MHz Band Mixer

Conditions: Unless otherwise specified, V_{DD} = 2.8V, V_{CTL} (H) = 2.8V, V_{CTL} (L) = 0V,
$f_{RF}1$ = 810MHz, $f_{RF}2$ = 885MHz, $f_{LO} = f_{RF} - 130$MHz, P_{LO} = –15dBm
(Ta = 25°C)

Item	Symbol	RF frequency	$V_{CTL}1$	$V_{CTL}2$	$V_{CTL}3$	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I_{DD_LO}	—	—	L	—	—	1.1	1.4	mA	When no signal
	I_{DD_MIX}		—	L	—	—	5.0	6.6		
Conversion gain	Gc	$f_{RF}1$	—	L	—	8.8	10	11.2	dB	When a small signal
		$f_{RF}2$	—	L	—	8.6	9.8	11.0		
Noise figure	NF	$f_{RF}1$	—	L	—	—	4	5.5	dB	
		$f_{RF}2$	—	L	—	—	5	6.5		
Input IP3	IIP3	$f_{RF}1$	—	L	—	1.0	+4.3	—	dBm	*3
		$f_{RF}2$	—	L	—	1.0	+4.3	—		
LO →RF leak	Plk	$f_{RF}1$	—	L	—	—	–26	–20	dBm	f_{LO} = 680MHz
		$f_{RF}2$	—	L	—	—	–22	–17		f_{LO} = 755MHz
RF input reflection	VSWR	$f_{RF}1$	—	L	—	—	2.4	3.2	—	*2
		$f_{RF}2$	—	L	—	—	2.7	3.6		
LO input reflection		680MHz	—	L	—	—	2.0	2.5		
		755MHz	—	L	—	—	1.9	2.4		

1.5GHz Band Mixer

Conditions: Unless otherwise specified, V_{DD} = 2.8V, V_{CTL} (H) = 2.8V, V_{CTL} (L) = 0V,
$f_{RF}3$ = 1490MHz, LO = 1360MHz/–15dBm (Ta = 25°C)

Item	Symbol	RF frequency	$V_{CTL}1$	$V_{CTL}2$	$V_{CTL}3$	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I_{DD_LO}	—	—	H	—	—	1.1	1.5	mA	When no signal
	I_{DD_MIX}		—	H	—	—	5.3	7.0		
Control current	I_{CTL}	$f_{RF}3$	L	H	L	—	43	69	µA	
Conversion gain	Gc	$f_{RF}3$	—	H	—	9.8	11	12.2	dB	When a small signal
Noise figure	NF	$f_{RF}3$	—	H	—	—	3.9	5.5	dB	
Input IP3	IIP3	$f_{RF}3$	—	H	—	–1.0	+1.8	—	dBm	*3
LO →RF leak	Plk	$f_{RF}3$	—	H	—	—	–21	–17	dBm	
RF input reflection	VSWR	$f_{RF}3$	—	H	—	—	1.6	2.1	—	*2
LO input reflection		1360MHz	—	H	—	—	2.9	3.9		

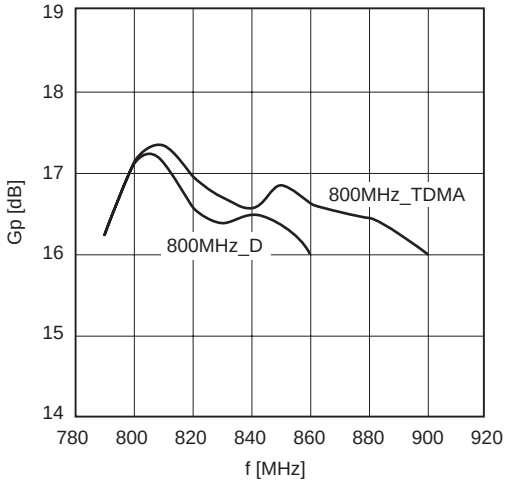
*3 Conversion from the IM3 suppression ratio for two-wave input: f_{RF}offset = 100kHz, P_{RF} = –25dBm

Example of Representative Characteristics

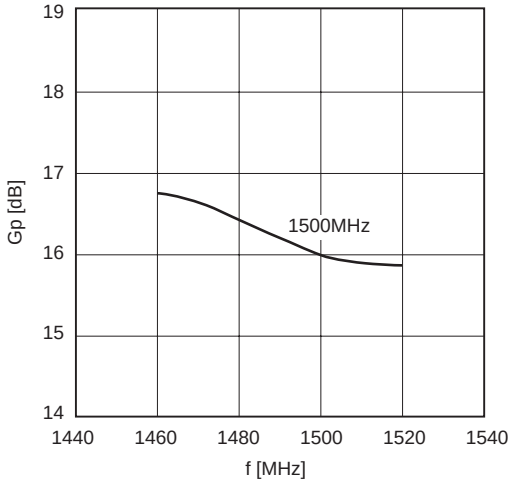
1. Frequency characteristics of main items in LNA block

Conditions: V_{DD} = 2.8V, 800MHz_D (Pin 12 input →Pin 4 output): $V_{CTL}1$ = 0V, $V_{CTL}2$ = 0V, $V_{CTL}3$ = 2.8V etc.
800MHz_TDMA (Pin 9 input →Pin 4 output): $V_{CTL}2$ = 0V, $V_{CTL}3$ = 0V,
1500MHz (Pin 7 input →Pin 5 output): $V_{CTL}2$ = 2.8V, $V_{CTL}3$ = 0V
Gp and NF are those when a small signal is input. The input IP3 is converted from the IM3 suppression ratio for two-wave input: f_{RF}offset = 100kHz, P_{RF} = –30dBm.

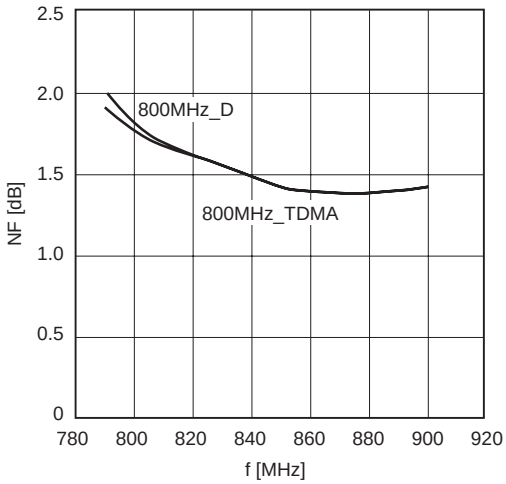
Power gain Gp



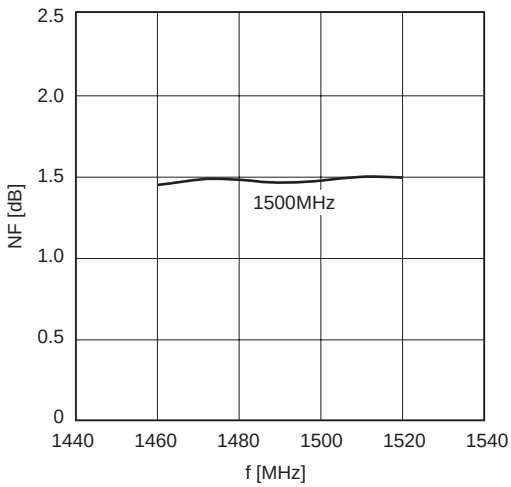
Power gain Gp



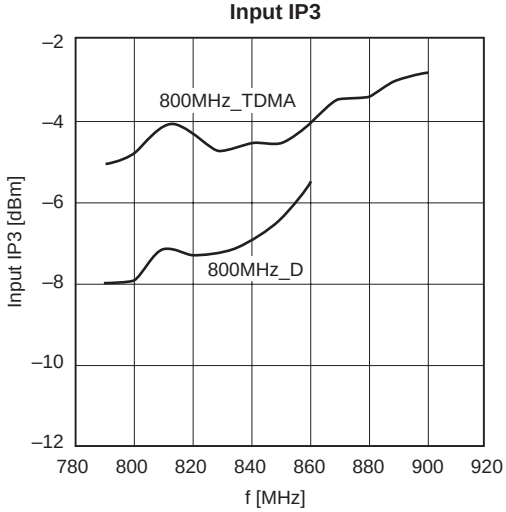
Noise figure NF



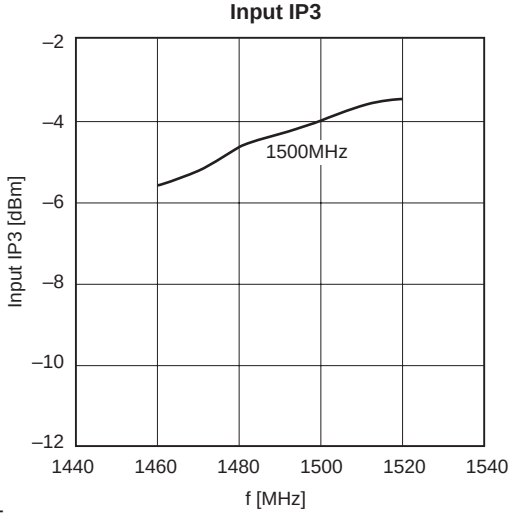
Noise figure NF



Input IP3



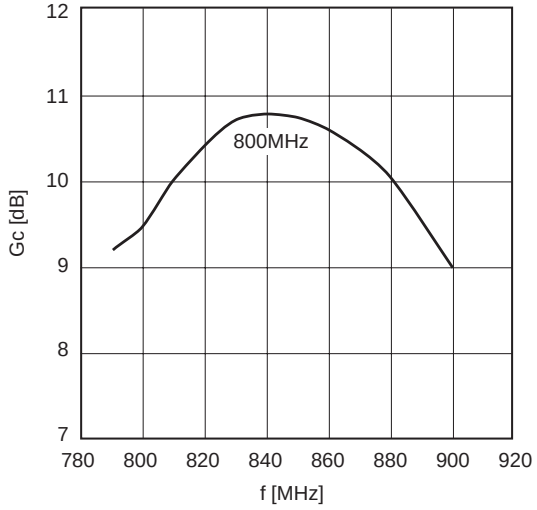
Input IP3



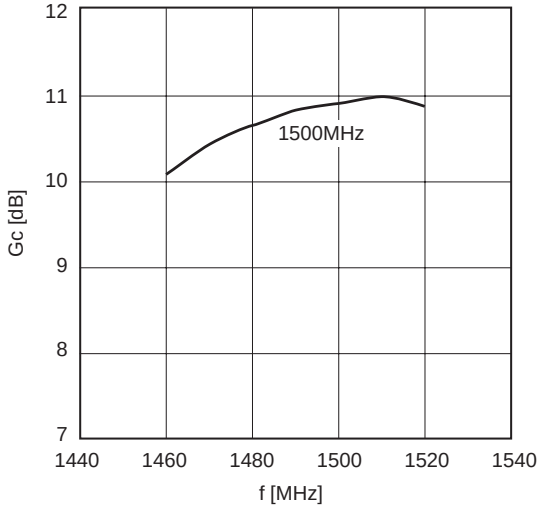
2. Frequency characteristics of main items in MIX block

Conditions: V_{DD} = 2.8V, $f_{LO} = f_{RF} - 130$MHz, P_{LO} = –15dBm, 800MHz: $V_{CTL}2$ = 0V, 1500MHz: V_{CTL2} = 2.8V
Gc and NF are those when a small signal is input. The input IP3 is concerted from the IM3 suppression ratio for two-wave input: f_{RF}offset = 100kHz, P_{RF} = –25dBm.

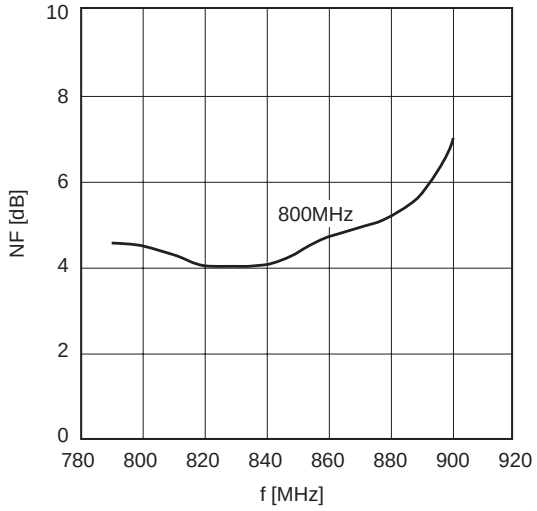
Conversion gain Gc



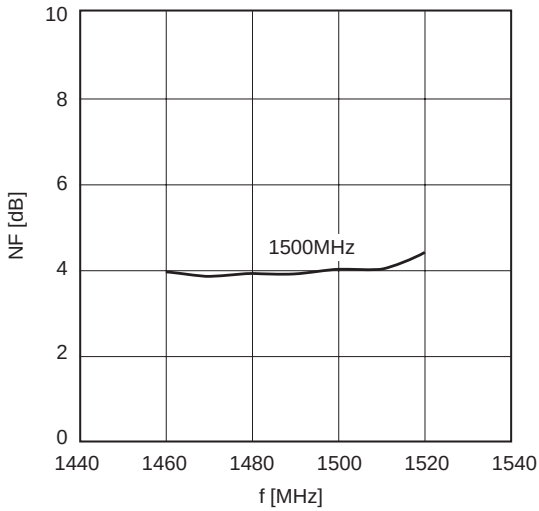
Conversion gain Gc



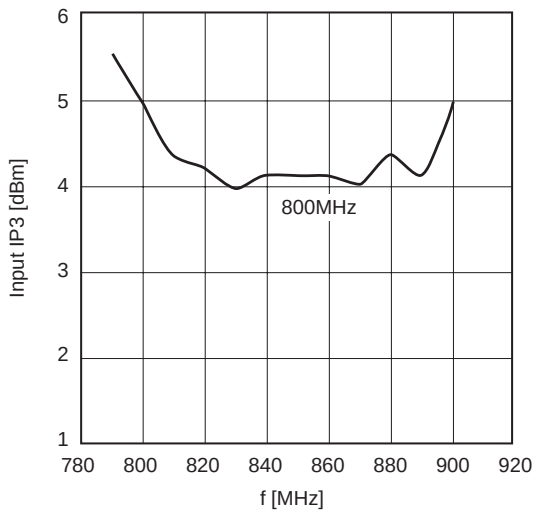
Noise figure NF



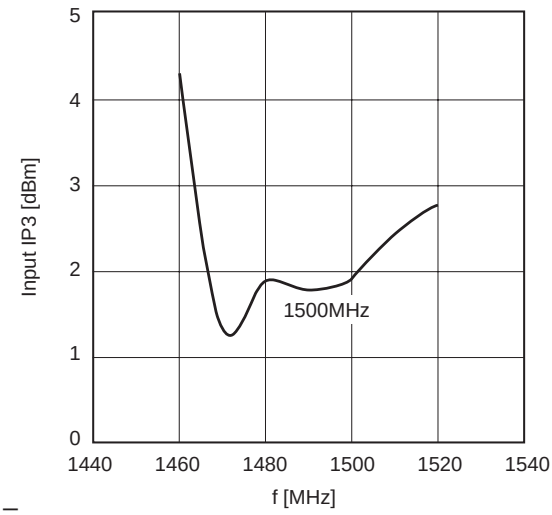
Noise figure NF



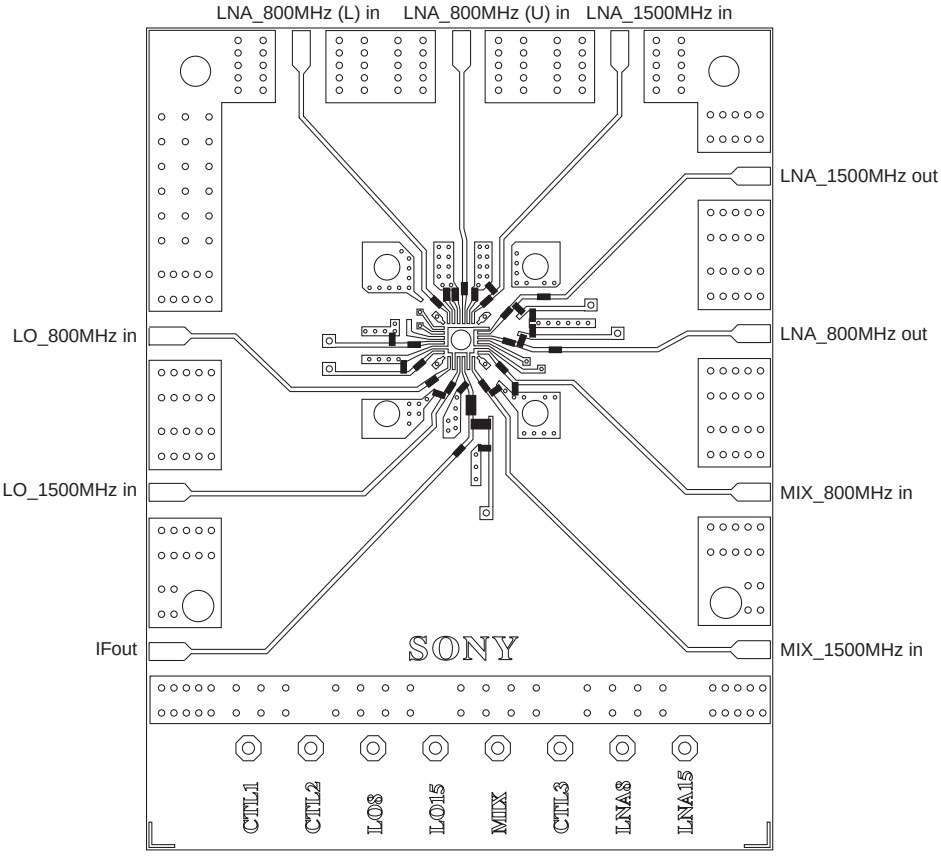
Input IP3



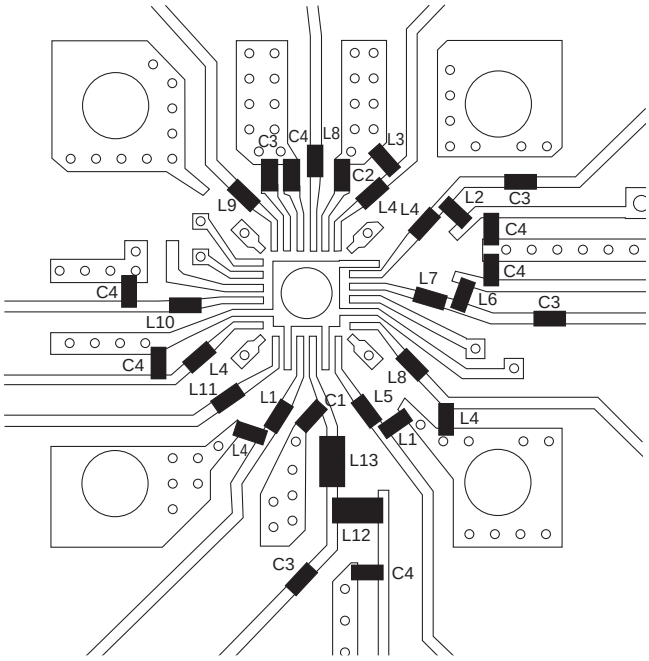
Input IP3



Recommended Evaluation Board



Enlarged Diagram of External Circuit Block

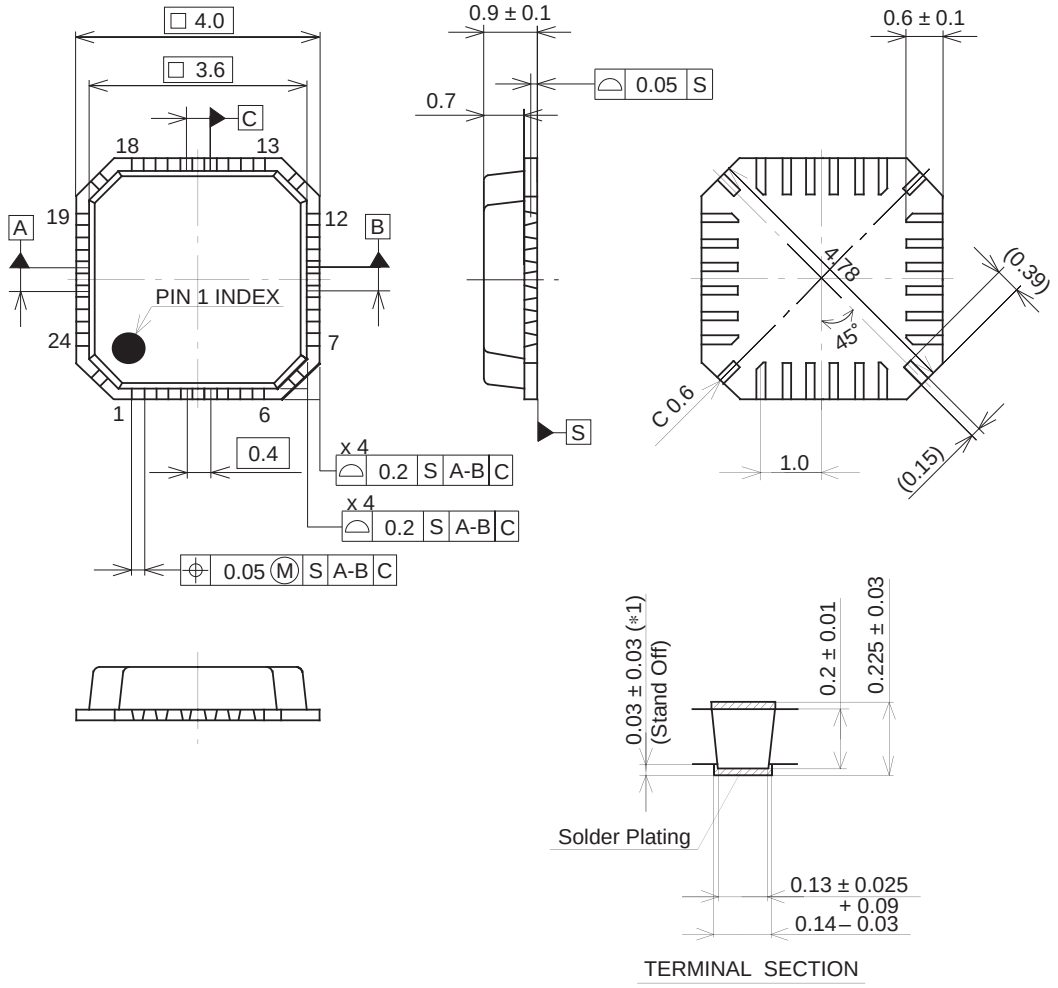


L1 = 2.7nH
L2 = 3.9nH
L3 = 5.6nH
L4 = 6.8nH
L5 = 8.2nH
L6 = 10nH
L7 = 15nH
L8 = 22nH
L9 = 27nH
L10 = 33nH
L11 = 39nH
L12 = 82nH
L13 = 120nH

C1 = 6pF
C2 = 22pF
C3 = 100pF
C4 = 1nF

Package Outline Unit: mm

24PIN VQFN(PLASTIC)



PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.04g

SONY CODE	VQFN-24P-03
EIAJ CODE	————
JEDEC CODE	————

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER PLATING	Sn-Bi Bi:1-4wt%
LEAD TREATMENT THICKNESS	5-18µm